

IRFPS35N50LPbF

SMPS MOSFET

HEXFET® Power MOSFET

Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications
- Lead-Free

V_{DS}	$R_{DS(on)}$ typ.	T_{rr} typ.	I_D
500V	0.125 Ω	170ns	34A

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	34	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	22	
I_{DM}	Pulsed Drain Current ①	140	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	450	W
	Linear Derating Factor	3.6	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	15	V/ns
T_J	Operating Junction and	-55 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lb•in)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	34	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 34\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	170	250	ns	$T_J = 25^\circ\text{C}$, $I_F = 34\text{A}$
		—	220	330		$T_J = 125^\circ\text{C}$, $di/dt = 100\text{A}/\mu\text{s}$ ④
Q_{rr}	Reverse Recovery Charge	—	670	1010	nC	$T_J = 25^\circ\text{C}$, $I_S = 34\text{A}$, $V_{GS} = 0\text{V}$ ④
		—	1500	2200		$T_J = 125^\circ\text{C}$, $di/dt = 100\text{A}/\mu\text{s}$ ④
I_{RRM}	Reverse Recovery Current	—	8.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.125	0.145	Ω	$V_{GS} = 10V, I_D = 20A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
R_G	Internal Gate Resistance	—	1.1	—	Ω	$f = 1MHz$, open drain

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	18	—	—	S	$V_{DS} = 50V, I_D = 20A$
Q_g	Total Gate Charge	—	—	230	nC	$I_D = 34A$
Q_{gs}	Gate-to-Source Charge	—	—	65	nC	$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	110	nC	$V_{GS} = 10V$, See Fig. 7 & 15 ④
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	100	—		$I_D = 34A$
$t_{d(off)}$	Turn-Off Delay Time	—	42	—		$R_G = 1.2\Omega$
t_f	Fall Time	—	42	—		$V_{GS} = 10V$, See Fig. 10a & 10b ④
C_{iss}	Input Capacitance	—	5580	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	590	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	58	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	7290	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	160	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	320	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	220	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ④	—	560	mJ
I_{AR}	Avalanche Current ①	—	34	A
E_{AR}	Repetitive Avalanche Energy ①	—	45	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.28	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	40	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.97mH$, $R_G = 25\Omega$, $I_{AS} = 34A$ (See Figure 13)
- ③ $I_{SD} \leq 34A$, $di/dt \leq 765A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ R_{θ} is measured at T_J approximately 90°C

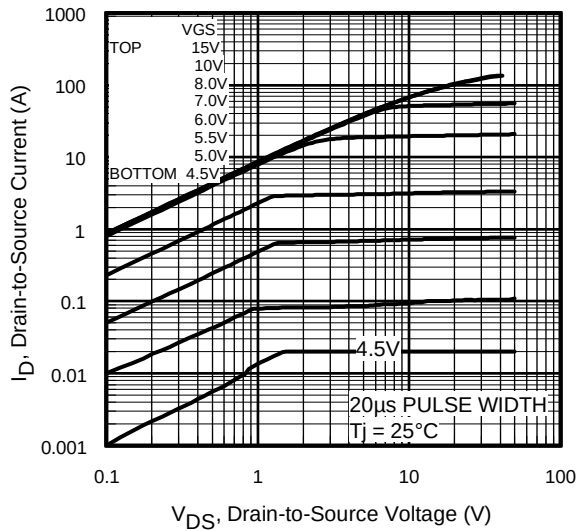


Fig 1. Typical Output Characteristics

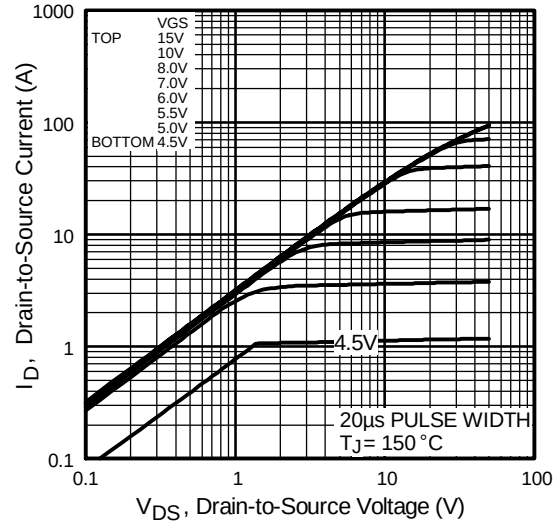


Fig 2. Typical Output Characteristics

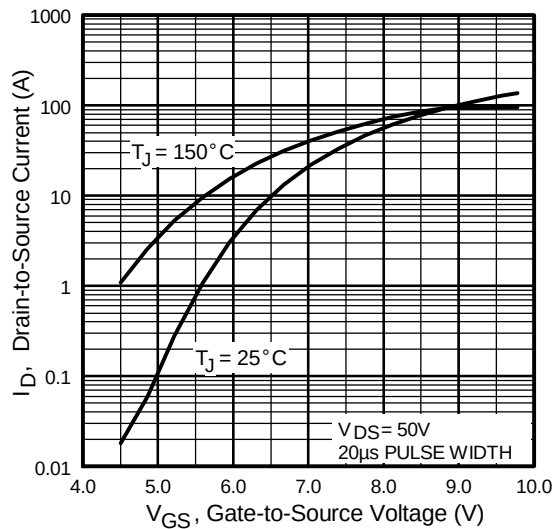


Fig 3. Typical Transfer Characteristics

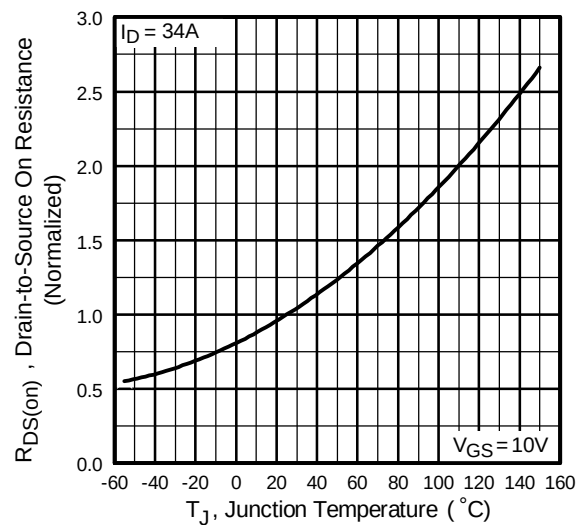


Fig 4. Normalized On-Resistance Vs. Temperature

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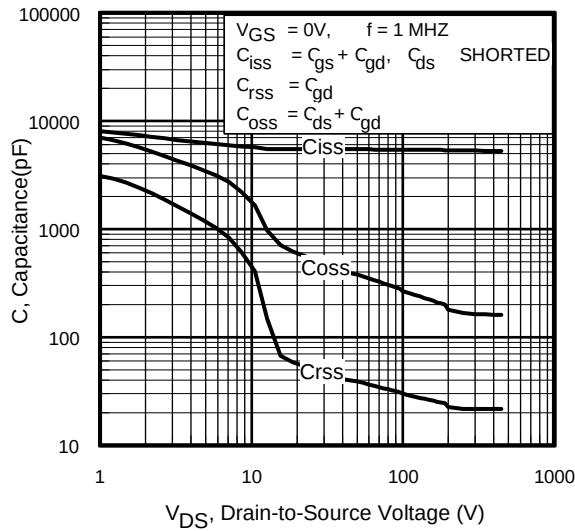


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

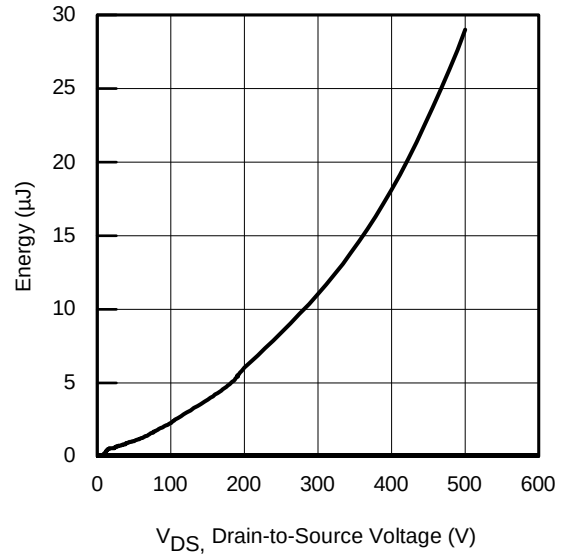


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

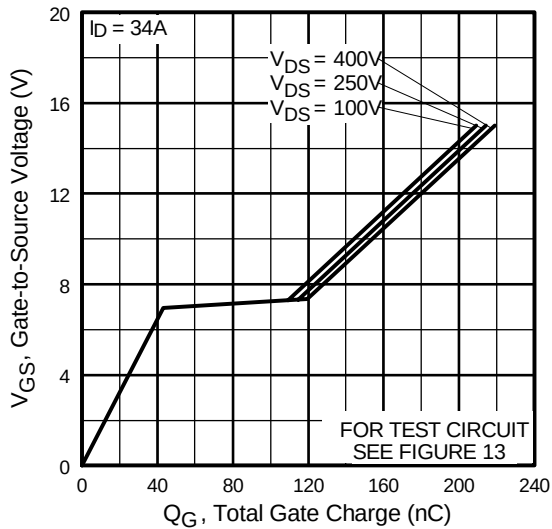


Fig 7. Typical Gate Charge Vs. Gate-to-Source Voltage

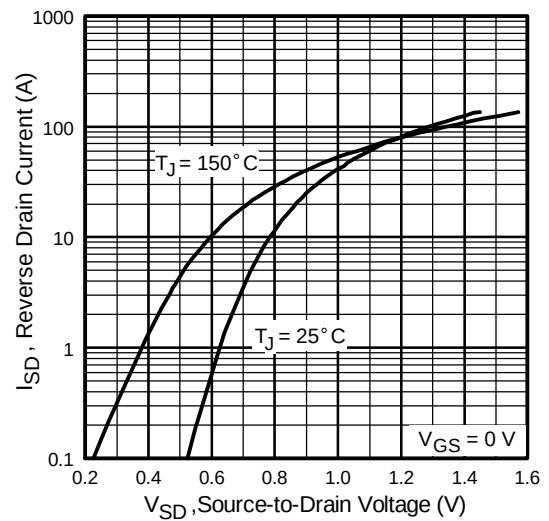


Fig 8. Typical Source-Drain Diode Forward Voltage

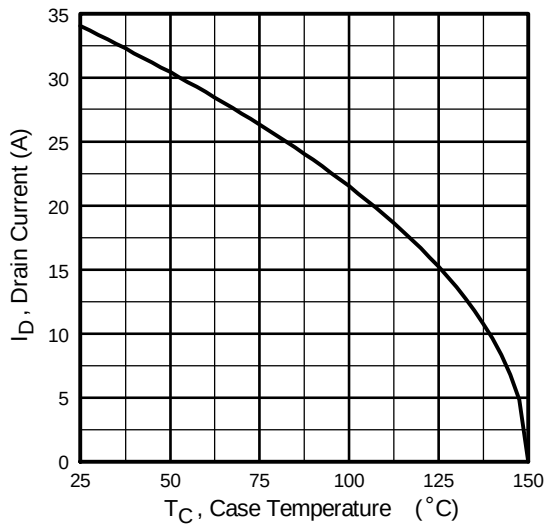


Fig 9. Maximum Drain Current Vs. Case Temperature

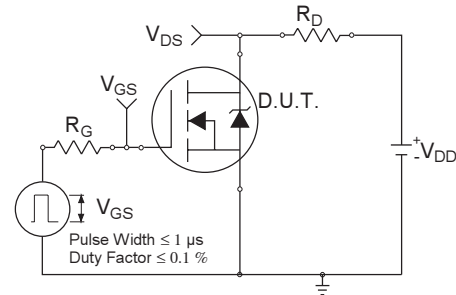


Fig 10a. Switching Time Test Circuit

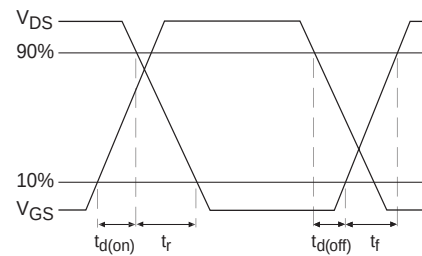


Fig 10b. Switching Time Waveforms

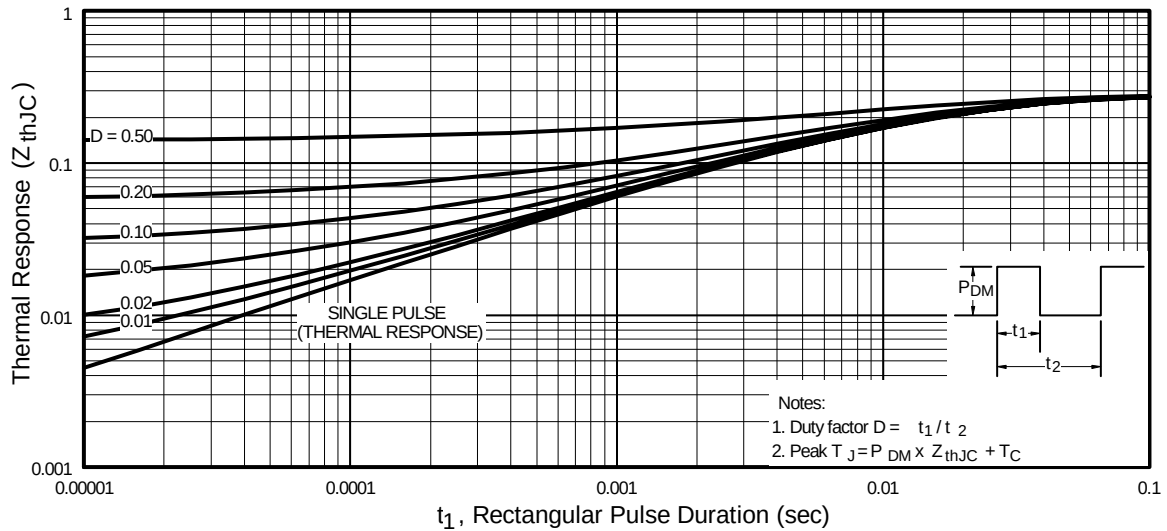


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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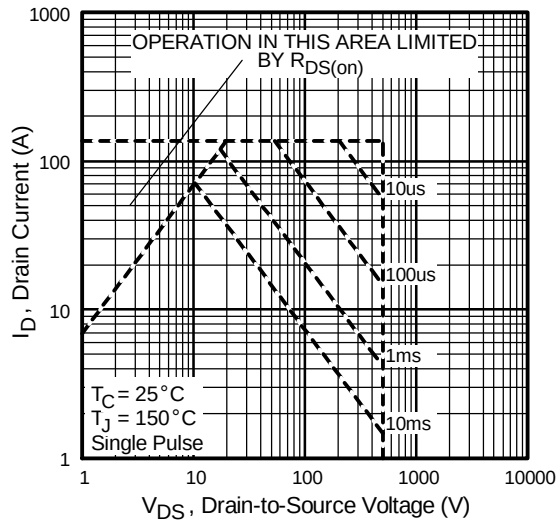


Fig 12. Maximum Safe Operating Area

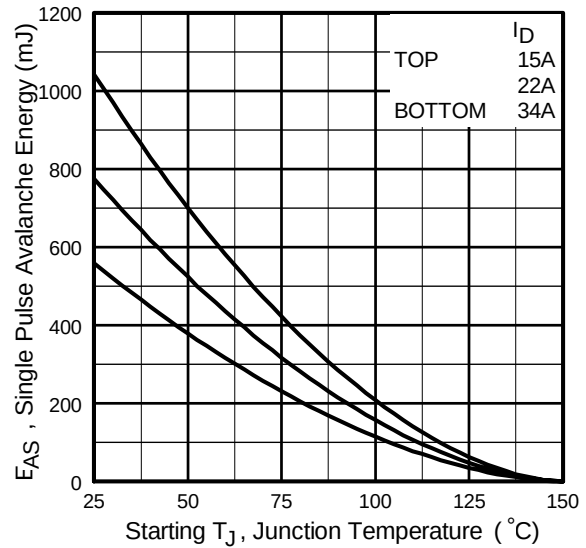


Fig 13. Maximum Avalanche Energy Vs. Drain Current

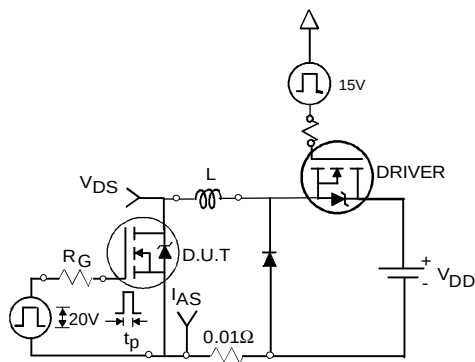


Fig 14a. Unclamped Inductive Test Circuit

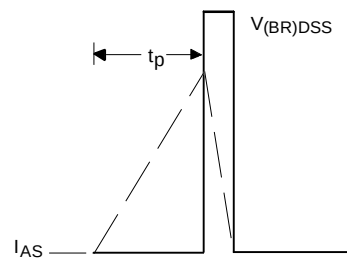


Fig 14b. Unclamped Inductive Waveforms

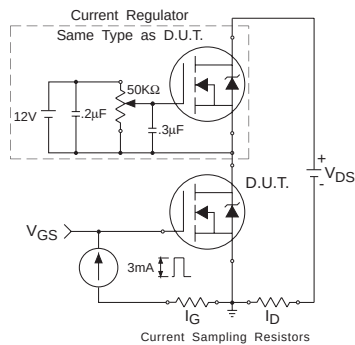


Fig 15a. Gate Charge Test Circuit

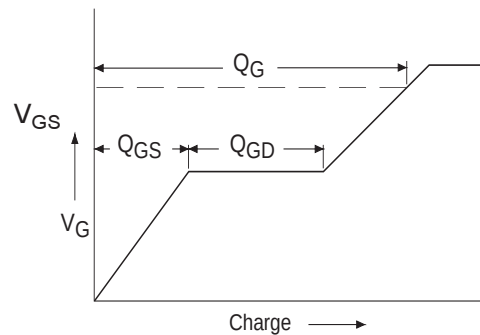
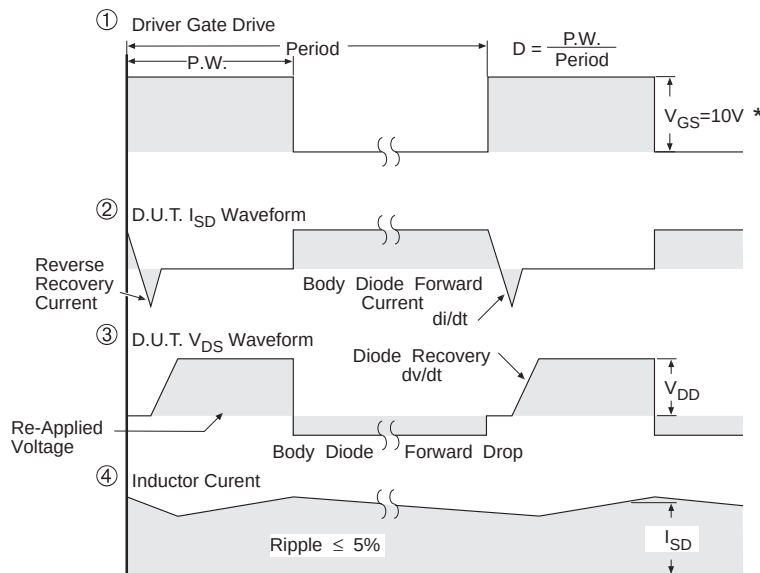
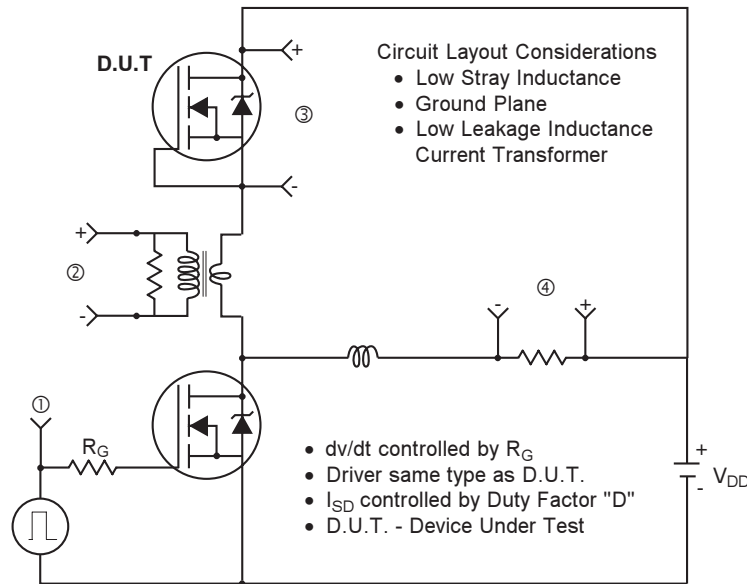


Fig 15b. Basic Gate Charge Waveform
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Peak Diode Recovery dv/dt Test Circuit

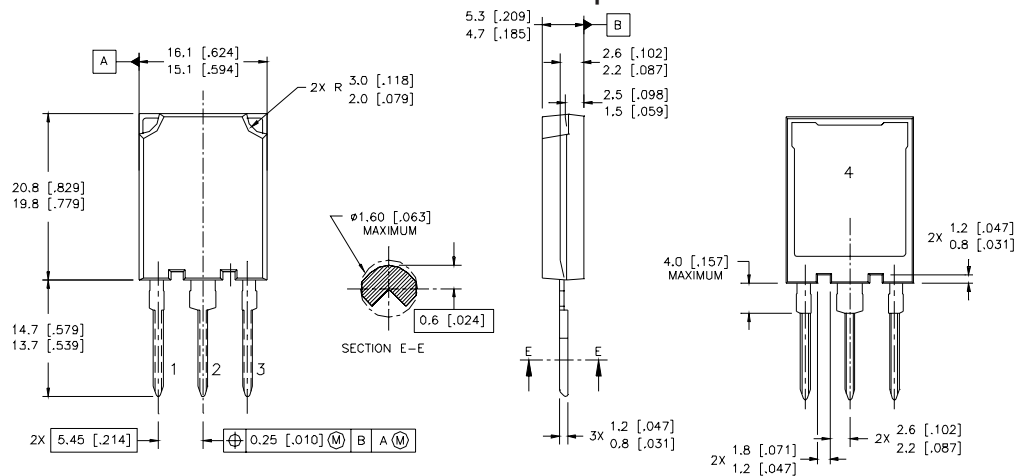


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

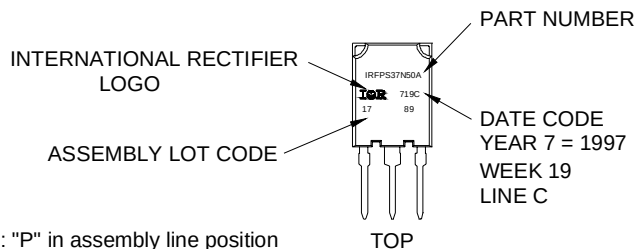
Case Outline and Dimensions — Super-247

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Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position indicates "Lead-Free"

Super TO-247™ package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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