# High Performance Step-Down DC-DC Converter With Dynamically Adjustable Output Voltage

## FEATURES

- 2-MHz PWM Operation
- Integrated MOSFET Switches
- 2.6-V to 6.0-V Input Voltage Range
- Minimal Number of External Components
- Up to 96% conversion efficiency
- 600-mA Load Capability
- 100% Duty Cycle Allows Low Dropout
- Integrated Compensation Circuit
- Over-Current Protection
- Shutdown Current < 2 μA
- Thermal Shutdown
- Integrated UVLO
- 10-Pin MSOP and Space Saving MLP33 Packaging
- DAC Input for Dynamic Output Voltage Adjustment
- Synchronizable to13-MHz Clock
- User Selectable PWM, PSM, or AUTO Mode
- PSM Frequency ≥20 kHz for Inaudible Harmonics

## APPLICATIONS

- W-CDMA Cell Phone
- PDAs/Palmtop PCs
- LCD Modules
- Portable Image Scanners
- GPS Receivers
- Smart Phones
- MP3 Players
- 3G Cell Phone
- Digital Cameras

## DESCRIPTION

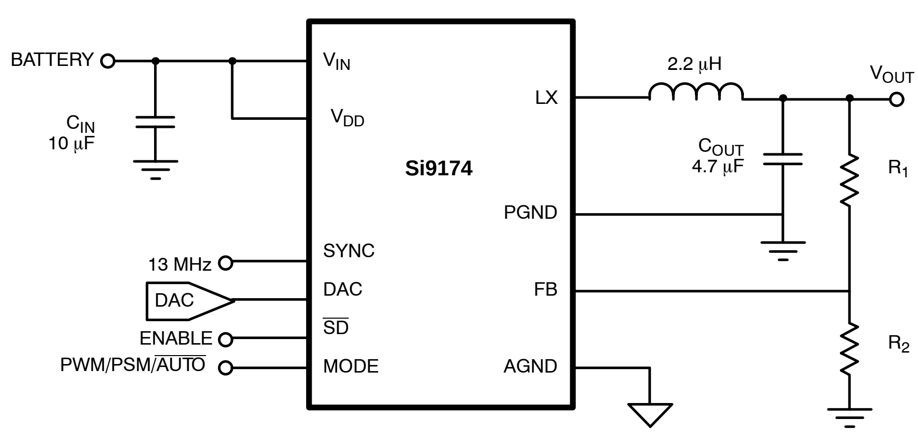
The Si9174 is a high efficiency 600-mA step down converter with internal low on resistance power MOSFET switch and synchronous rectifier transistors. It is designed to convert one cell LiIon battery or three cell alkaline battery voltages to a dynamically adjustable dc output. The voltage on the DAC pin controls the output voltage. The output voltage is adjustable between 0.4 V and the input voltage $V_{IN}$ less a small dropout voltage and settles in <30 μs.

In order to insure efficient conversion throughout the entire load range, PWM (pulse width modulation), PSM (pulse skipping mode) or Auto mode can be selected. In PWM mode, 2-MHz switching permits use of small external inductor and capacitor sizes allowing *one of the smallest solutions*. To minimize system noise, the switching frequency can be synchronized to an external 13-MHz clock.

PSM mode provides increased efficiency at light loads. In PSM mode the oscillator frequency is kept above 20 kHz to avoid audio band interference. When operating in Auto mode, the converter automatically selects operating in either PWM or PSM mode according to load current demand.

The Si9174 is available in the10-pin MSOP and the even smaller MLP33 package and is specified to operate over the industrial temperature range of –40°C to 85°C. The Si9174 packaged in the MLP33 package is available in both standard and lead (Pb)-free.

## TYPICAL APPLICATIONS CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to AGND = 0 V
$V_{IN}$, $V_{DD}$ .......... 6.2 V
Lx, $\overline{SD}$, MODE, FB, DAC, SYNC .......... –0.3 to 6.2 V
(or to $V_{DD}$ + 0.3 V whichever is less)
GND .......... –0.3 to +0.3 V
ESD Rating .......... 2 kV
Storage Temperature .......... –65 to 125°C
Operating Junction Temperature .......... 150°C
Power Dissipation (Package)[a]
10-pin MSOP[b] .......... 481 mW
10-pin MLP33 .......... 915 mW

Thermal Impedance ($\Theta_{JA}$)
10-Pin MSOP .......... 135°C/W
10-Pin MLP33 .......... 71°C/W
Peak Inductor Current .......... 1.8 A

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.4 mW/°C above 85°C.
c. Derate 14 mW/°C above 85°C.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING RANGE

$V_{IN}$ Range .......... 2.6 V to 5.5 V
$C_{IN}$ .......... 10 µF Ceramic
$C_{OUT}$ .......... 4.7 µF Ceramic
Inductor .......... 2.2 µH
Operating Load Current PWM Mode .......... 0 to 600 mA
Operating Load Current PSM Mode .......... 0 to 150 mA

## SPECIFICATIONS

| Parameter | Mode[f] | Symbol | Test Conditions Unless Specified: −40°C to 85°C, $V_{IN} = V_{DD}$, $V_{DAC}$ = 1.215 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 4.7 µF, L = 2.2 µH, 2.6 V ≤ $V_{IN}$ ≤ 5.5 V, $R_1$ = 11.3 kΩ, $R_2$ = 20 kΩ | | Limits Min[a] | Typ[b] | Max[a] | Unit |
|---|---|---|---|---|---|---|---|---|
| **Under Voltage Lockout (UVLO)** | | | | | | | | |
| Under Voltage Lockout (turn-on) | | | $V_{IN}$ rising | | 2.3 | | 2.5 | V |
| Hysteresis | | | | | | 0.1 | | V |
| **Shutdown ($\overline{SD}$)** | | | | | | | | |
| Logic HIGH | | $V_{SDH}$ | | | 1.6 | | | V |
| Logic LOW | | $V_{SDL}$ | | | | | 0.4 | V |
| Delay to Output[c] | | $t_{en}$ | Settle Within ±2% accuracy $\overline{SD}$ rising $t_r$ < 1 µs | $R_L$ = 3.3 Ω | | | 100 | µs |
| | | | | $R_L$ = 51 Ω | | 100 | | µs |
| Pull Down | | $I_{SD}$ | Input at $V_{IN}$ | | | | | µA |
| **Mode Selection Tri-Level Logic (MODE)** | | | | | | | | |
| MODE Pin HIGH | PWM | | | | $V_{IN}$ −0.4 | $V_{IN}$ | | V |
| MODE Pin LOW | Auto | | | | | | 0.4 | V |
| Mode Pin Input Current | | | MODE = GND | | | −5 | | µA |
| | | | MODE = $V_{IN}$ | | | 5 | | µA |
| **Oscillator** | | | | | | | | |
| Frequency | | $f_{OSC}$ | | | 1.6 | 2 | 2.4 | MHz |
| **External Clock Synchronization (SYNC)** | | | | | | | | |
| Frequency | | | SYNC Input = 500 $mV_{p-p}$ | | | 13 | | MHz |
| Ac Coupled Sinewave | | | Frequency = 13 MHz | | 0.2 | | 0.8 | $V_{p-p}$ |
| **Error Amplifier (FB, DAC Pin)** | | | | | | | | |
| FB Voltage Accuracy | | | | | $V_{DAC}$ −20 | | $V_{DAC}$ +20 | mV |
| DAC Input Voltage Range | | | $V_{IN}$ > 2.6, $V_{IN} - V_{DAC}$ > 0.5 V | | 0.28 | | 2.45 | V |
| Input Bias Current FB, DAC | | $I_{FBDAC}$ | $V_{FB}$ = 1.25 V | | −1 | 0.01 | 1 | µA |

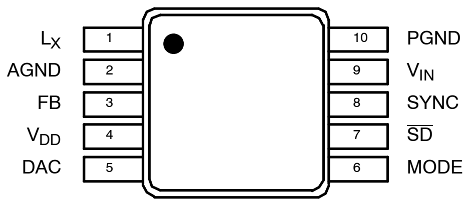
## SPECIFICATIONS

| Parameter | Mode[f] | Symbol | Test Conditions Unless Specified: −40°C to 85°C, $V_{IN}$ = $V_{DD}$, $V_{DAC}$ = 1.215 V, $C_{IN}$ = 10 μF, $C_{OUT}$ = 4.7 μF, L = 2.2 μH, 2.6 V ≤ $V_{IN}$ ≤ 5.5 V, $R_1$ = 11.3 kΩ, $R_2$ = 20 kΩ | | Limits Min[a] | Typ[b] | Max[a] | Unit |
|---|---|---|---|---|---|---|---|---|
| **Converter Operation** | | | | | | | | |
| Maximum Output Current | PWM | $I_{LOAD}$ | $V_{IN}$ = 3.6 V | | 600 | | | mA |
| Maximum Output Current | PSM | $I_{LOAD}$ | $V_{IN}$ = 3.6 V | | | | 150 | mA |
| Dropout Voltage[e] | | $V_{DD}$ | $V_{IN}$ = 2.6 V, $I_{OUT}$ = 600 mA | | | 190 | 300 | mV |
| Closed Loop Bandwidth | | BW | | | | 300 | | kHz |
| Load Regulation[c] | PWM | | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.9 V @ 25°C | $I_{OUT}$ = 30 mA to 600 mA | | 0.5 | | % |
| | PSM | | | $I_{OUT}$ = 30 mA to 75 mA | | 0.25 | | |
| Line Regulation | PWM | | $V_{OUT}$ = 3.0 V, $V_{IN}$ = 3.5 V to 5.5 V | | | ± 0.1 | | %/V |
| | PSM | | | | | ± 0.1 | | |
| PWM/PSM Switch Threshold Current | | $I_{AUpk}$ | | | | 200 | | mA |
| Maximum Inductor Peak Current Limit | | $I_{Lpk}$ | | | | 1500 | | |
| Maximum NMOS Transistor Current Sink | PWM | | Negative Transition on $V_{DAC}$ | | | 1500 | | |
| On Resistance | P-Channel | $r_{DS(on)}$ | $V_{IN}$ = 3.6 V | | | 250 | | mΩ |
| | N-Channel | | | | | 250 | | |
| Output Ripple Voltage | PWM | | 0.05 Ω $C_{OUT(ESR)}$ | $I_{OUT}$ = 600 mA | | 60 | | $mV_{p-p}$ |
| | PSM | | | $I_{OUT}$ = 30 mA | | 80 | | |
| Efficiency | PWM | | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 3.3 V | $I_{OUT}$ = 600 mA | | 90 | | % |
| | PSM | | | $I_{OUT}$ = 30 mA | | 80 | | |
| Frequency | PSM | | $I_{OUT}$ ≥ 30 mA | | 20 | | | kHz |
| **Supply Current** | | | | | | | | |
| Input Supply Current | PWM | $I_{SUPPLY}$ ($V_{DD}$ & $V_{IN}$) | $I_{OUT}$ = 0 mA, $V_{IN}$ = 3.6 V (not switching, FB = GND) | | | 500 | 800 | μA |
| | PSM | | | | | 400 | | |
| Shutdown Supply Current | | $I_{SD}$ | $\overline{SD}$ = Low | | | | 2 | |
| **Thermal Shutdown** | | | | | | | | |
| Thermal Shutdown Temperature[c] | | $T_{J(S/D)}$ | | | | 165 | | °C |
| Thermal Hysteresis[c] | | | | | | 20 | | |

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
c. Guaranteed by design.
d. Settling times, $t_s$, apply after $t_{en}$.
e. Bypass is a device mode of operation, in which, the device is in 100% duty cycle. Bypass operation is possible in either PWM or PSM.
f. Operating modes are controlled with the MODE pin where Auto mode = MODE = LOW, PWM Mode = MODE = HIGH, and PSM mode = MODE = OPEN.

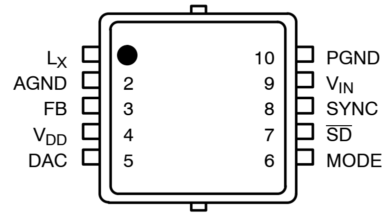
## PIN CONFIGURATION

**MSOP-10**




Top View

**MLP33**




Top View

## PIN DESCRIPTION

| Pin Number | Name | Function |
|---|---|---|
| 1 | $L_X$ | Inductor connection |
| 2 | AGND | Low power analog ground |
| 3 | FB | Output voltage feedback |
| 4 | $V_{DD}$ | Input supply voltage for the analog circuit. |
| 5 | DAC | Voltage from external DAC to adjust output voltage. |
| 6 | MODE | Used to select switching mode of the buck converter<br>PWM/PSM Pin Logic:<br>**MODE Pin** — **Operating Mode**<br>$V_{IN}$ — PWM<br>Open — PSM<br>GND — AUTO |
| 7 | $\overline{SD}$ | Logic low disables IC and reduces quiescent current to below 2 μA |
| 8 | SYNC | Converter switching frequency can be synchronized to $^1/_6$ of the clock frequency at this pin. |
| 9 | $V_{IN}$ | Input supply voltage |
| 10 | PGND | Low impedance power ground |

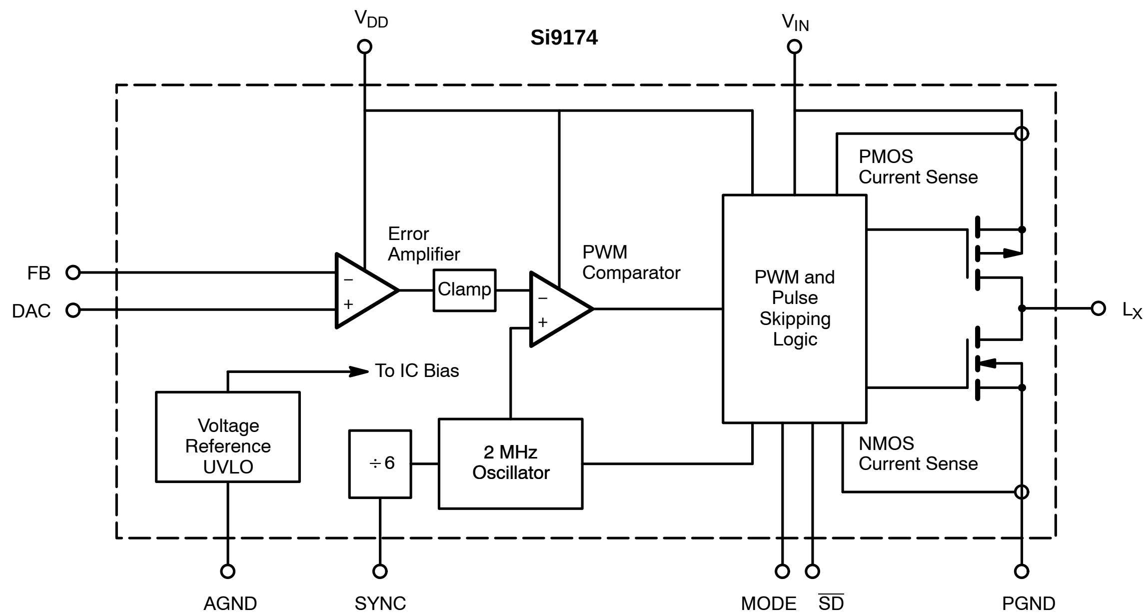
## ORDERING INFORMATION

| MSOP-10 | | | MLP33 | | | |
|---|---|---|---|---|---|---|
| Standard Part Number | Marking | Temperature | Standard Part Number | Lead (Pb)-Free Part Number | Marking | Temperature |
| Si9174DH-T1 | 9174 | –40 to 85°C | Si9174DM-T1 | Si9174DM-T1—E3 | 9174 | –40 to 85°C |

Additional voltage options are available.

| Eval Kit | Temperature Range | Board |
|---|---|---|
| Si9174DB | –40 to 85°C | Surface Mount |

## FUNCTIONAL BLOCK DIAGRAM




## DETAIL DESCRIPTION

### General

The Si9174 is a high efficiency synchronous dc-dc converter that is ideally suited for lithium ion battery or three cell alkaline applications, as well as step-down of 3.3-V or 5.0-V supplies. It is design to provide power to the power amplifier in WCDMA cell phones, but can utilized in any applications requiring a dynamically adjustable 600-mA power supply. The major blocks of the Si9174 are shown in the Functional Block Diagram. The 0.25-Ω internal MOSFETs switching at a frequency of 2-MHz minimize PC board space while providing high conversion efficiency and performance. The high frequency error-amplifier with built-in loop compensation minimizes external components and provides rapid output settling times of <30 μs. Sensing of the inductor current for control is accomplished internally without power wasting resistors. The switching frequency can be synchronized to an external 13-MHz clock signal.

### Start-Up

When voltage is applied to $V_{IN}$ and $V_{DD}$, the under-voltage lockout (UVLO) circuit prevents the oscillator and control circuitry from turning on until the voltage on the exceeds 2.4 V. With a typical UVLO hysteresis of 0.1 V, the converter operates continuously until the voltage on $V_{IN}$ drops below 2.3 V, whereupon the converter shuts down. This hysteresis prevents false start-stop cycling as the input voltage approaches the UVLO switching threshold. Start-up is always accomplished in PWM mode to ensure start-up under all load conditions. Switching to other modes of operation occurs according to the state of the MODE pin and the load current. The start-up sequence occurs after $\overline{SD}$ switches from LOW to HIGH with $V_{IN}$ applied, or after $V_{IN}$ rises above the UVLO threshold and $\overline{SD}$ is a logic HIGH.

### Mode Control (MODE)

The MODE pin allows the user to control the mode of operation or to enable the Si9174 to automatically optimize the mode of operation according to load current. There are three different modes of operation as controlled by the MODE pin. Switching waveforms are shown in the Typical Switching Waveform sections, page 9.

### PWM Mode (MODE pin = HIGH)

With the MODE pin in the logic HIGH condition, the Si9174 operates as a 2-MHz fixed frequency voltage mode converter. A NMOS synchronous rectification MOSFET transistor provides very high conversion efficiency for large load currents by minimizing the conduction losses. PWM mode provides low output ripple, fast transient response, and switching frequency synchronization. Output load currents can range from 0 to 600 mA.

The error amplifier and comparator control the duty cycle of the PMOS MOSFET to continuously force the DAC pin and FB pin voltages to be equal. As the input-to-output voltage difference drops, the duty cycle of the PMOS MOSFET can reach 100% to allow system designers to extract the maximum stored energy from the battery. The dropout voltage is 190 mV at 600 mA.

During each cycle, the PMOS switch current is limited to a maximum of 1.5 A (typical) thereby protecting the IC while continuing to force maximum current into the load. Similarly, the NMOS switch is internally limited to a maximum of 1.5 A (typical) during negative output voltage transients.

**Pulse Skipping Mode (MODE pin = OPEN)**

By leaving the MODE pin open-circuit, the converter runs in pulse skipping mode (PSM). In PSM mode the oscillator continues to operate, but switching only occurs if the FB pin voltage is below the DAC voltage at the start of each clock cycle. Clock cycles are skipped thereby reducing the switching frequency to well below 100 kHz and minimizing switching losses for improved efficiency at loads under 150 mA. Although PSM mode switching frequency varies with line and load conditions, the minimum PSM frequency will be kept above 20 kHz for load currents of 30 mA or more to prevent switching noise from reaching the audio frequency range.

Each time the PMOS switch is turned on, the inductor current is allowed to reach 300 mA. Once achieved, the PMOS switch is turned off and the NMOS switch is turned on in the normal manner. However, unlike PWM mode, the NMOS switch, turns off as the switch current approaches zero current to maximize efficiency. The PMOS switch remains on continuously (100% duty cycle) when the input-voltage-to-output-voltage difference is low enabling maximum possible energy extraction from the battery.

PSM mode is recommend for load currents of 150 mA or less.

**Auto Mode**

When the MODE pin grounded, the converter is set to Auto mode. Switching between PWM mode and PSM modes takes place automatically without an external control signal. For heavy load operation, the converter will operate in PWM mode to achieve maximum efficiency. When delivering light load currents, the converter operates in PSM mode to conserve power. The switchover threshold between the two modes is determined by the peak inductor current, which is 300 mA nominal. There is hysteresis in the switchover threshold to provide smooth operation. Thus, the mode PSM-to-PWM mode switchover current for increasing load currents is higher than that of PWM-to-PSM mode switchover for decreasing load currents.

**Oscillator Synchronization (SYNC)**

The internal oscillator provides for a fixed 2-MHz switching frequency. In order to minimize system noise, the oscillator of the Si9174 can be synchronized to an external clock, typically an ac-coupled 13-MHz sine wave. An on-chip divide-by-six circuit sets the converter switching frequency to 2.167 MHz in this mode. The frequency lock range of the synchronization circuitry is typically 20%. If synchronization is not required, the SYNC pin must be tied to GND permitting the internal oscillator to oscillate at 2 MHz.

**Dynamic Output Voltage Control (DAC)**

The Si9174 is designed to dynamically adjust the output voltage according to the voltage present on the DAC pin. The output voltage is regulated to the same voltage the DAC pin through the resistor divider. For $V_{DAC}$ within the voltage range of 0.28 – 2.45 V, $V_{OUT}$ is proportional to $V_{DAC}$ according to the following relationship:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{DAC}$$

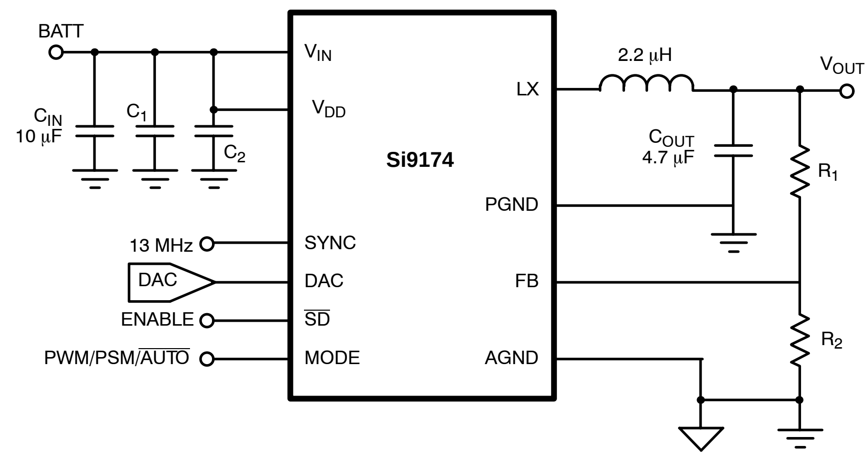
**Converter Shutdown ($\overline{SD}$ pin)**

With logic LOW level on the $\overline{SD}$ pin, the Si9174 is shutdown. Shutdown reduces current consumption to less than 2-µA by shutting off all of the internal circuits. Both the PMOS and NMOS transistors are turned off. A logic HIGH enables the IC to start up as described in “Start-up” section.

**Thermal Shutdown**

The Si9174 includes thermal shutdown circuitry, which turns off the regulator when the junction temperature exceeds 165°C. Once the junction temperature drops below 145°C, the regulator is enabled. If the condition causing the over temperature, the Si9174 begins thermal cycling, turning the regulator on and off in response to junction temperature. Restart from a thermal shutdown condition is the same as described in the “Start-up” section.

## APPLICATIONS CIRCUIT




$C_{IN}$ = 10 µF, Ceramic, Murata GRM42-2X5R106K16
$C_1$, $C_2$ = 0.01 µF, Vishay VJ0603Y 104KXXAT
$C_{OUT}$ = 4.7 µF, Ceramic, Murata GRM42-6X5R475K16
$R_1$ = 8.2 kΩ, Vishay CRCW06031132F
$R_2$ = 20 kΩ, Vishay CRCW06032002F
$L_1$ = 2.2 µH, Toko A914BYW-2R2M

## TYPICAL CHARACTERISTICS

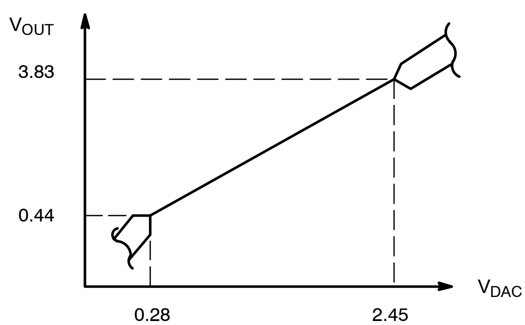
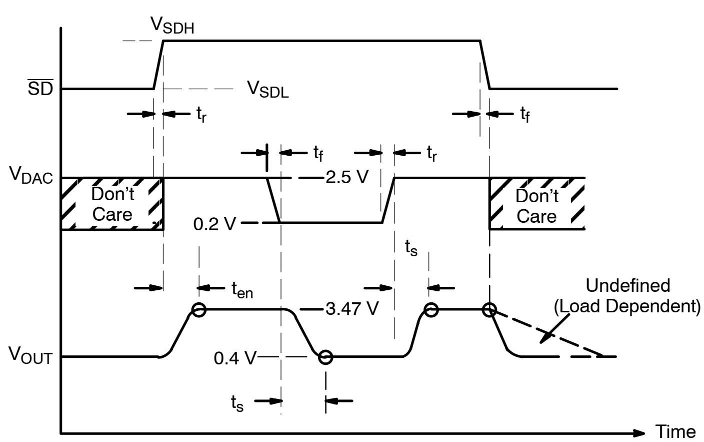


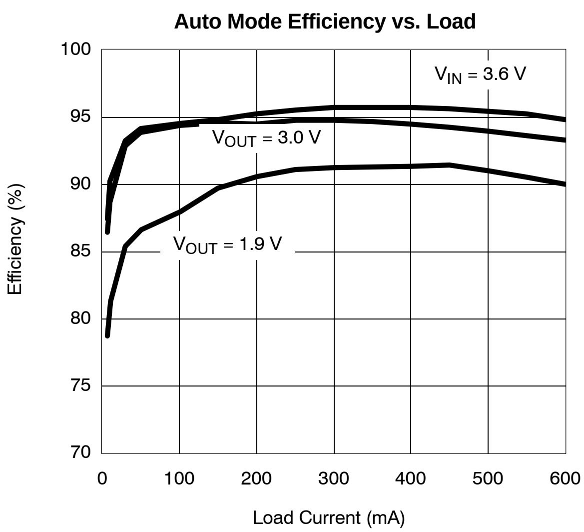

**Figure 1.** $V_{OUT}$-vs. $V_{DAC}$ Characteristics ($V_{IN}$ = 5 V)

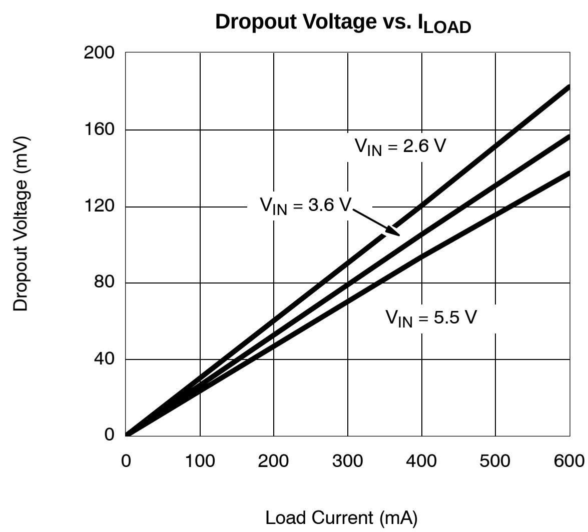


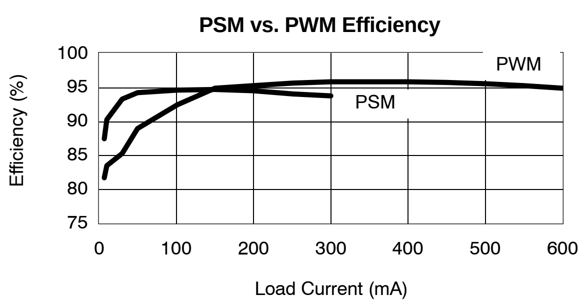

○ Indicates $V_{OUT}$ settles to ±2% of the final value.

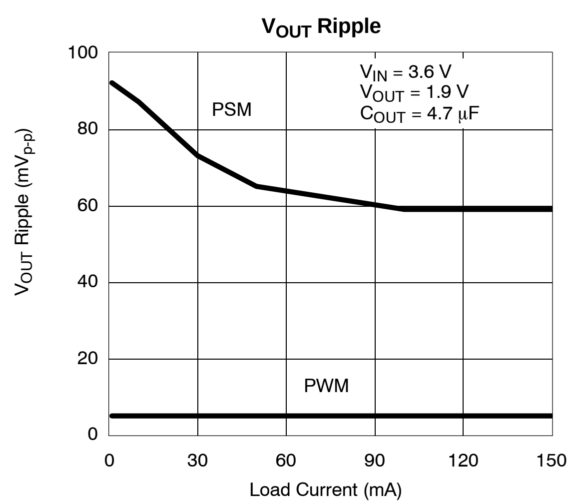
**Figure 2.** PWM Mode $V_{OUT}$ Settling

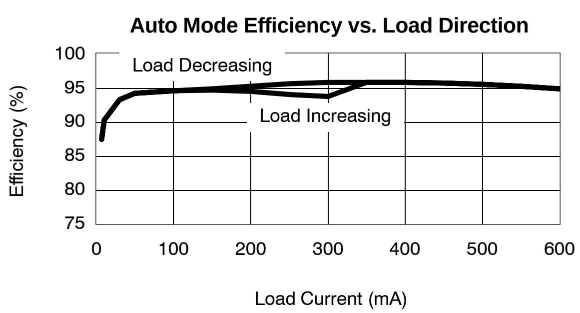
## TYPICAL CHARACTERISTICS



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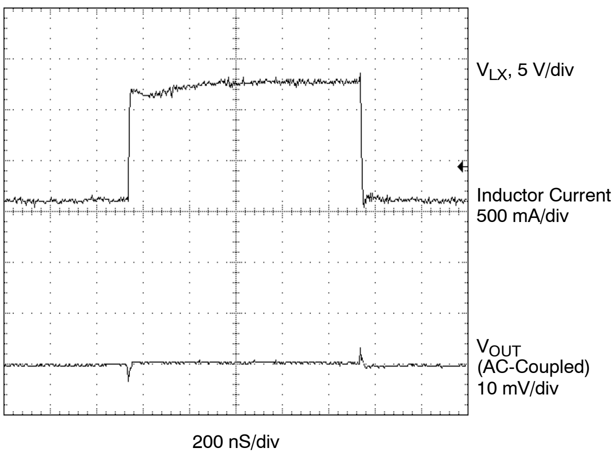
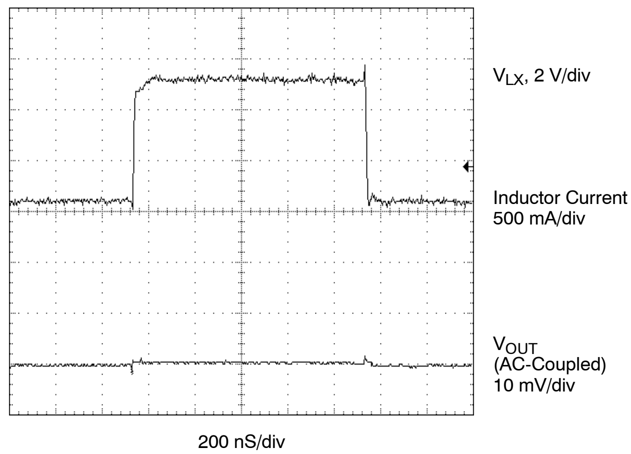
## TYPICAL SWITCHING WAVEFORMS ($V_{IN}$ = 3.6 V, $V_{OUT}$ = 3.0 V)

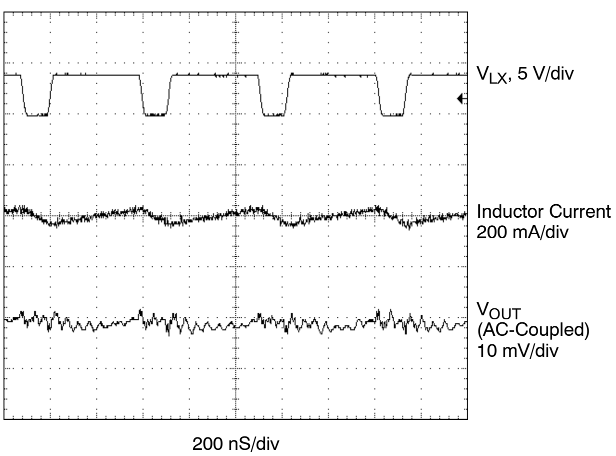
PWM mode Heavy-Load Switching Waveforms,
$I_{OUT}$ = 600 mA, MODE = HIGH



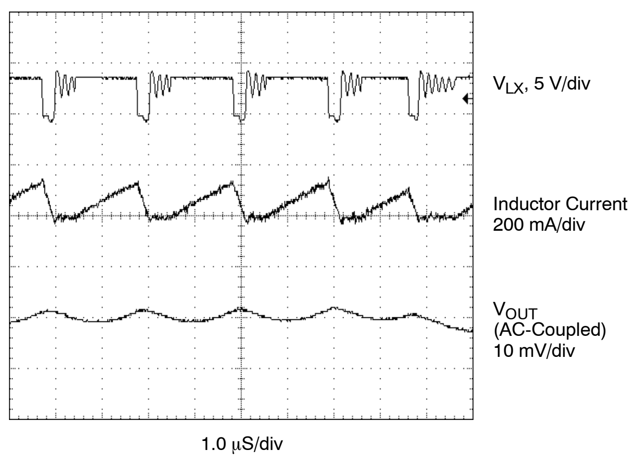

PWM Mode Medium-Load Switching Waveforms,
$I_{OUT}$ = 300 mA, MODE = HIGH



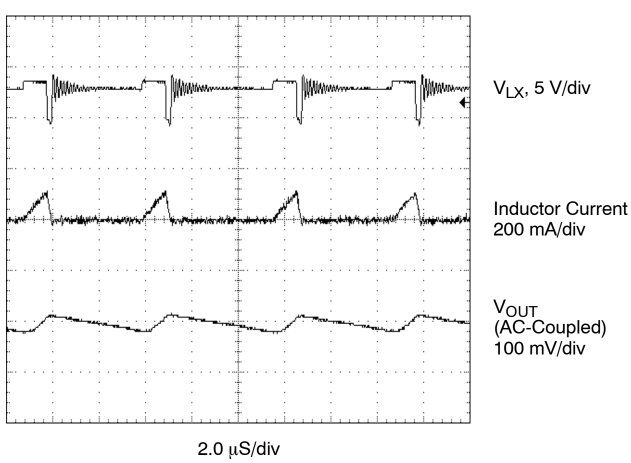

PWM Mode Light-Load Switching Waveforms,
$I_{OUT}$ = 0 mA, MODE = HIGH




PSM Mode Light-Load Switching Waveforms,
$I_{OUT}$ = 150 mA, MODE = OPEN

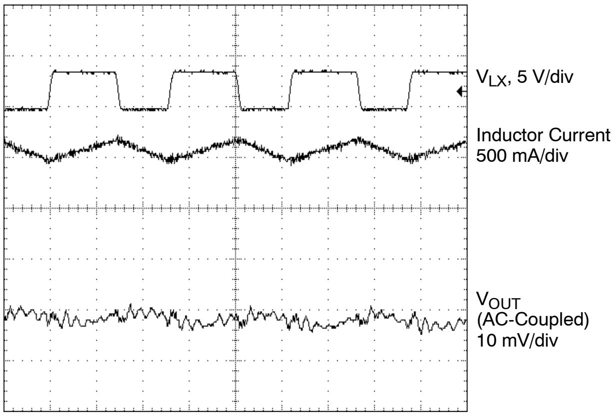



PSM Mode Light-Load Switching Waveforms,
$I_{OUT}$ = 30 mA, MODE = OPEN



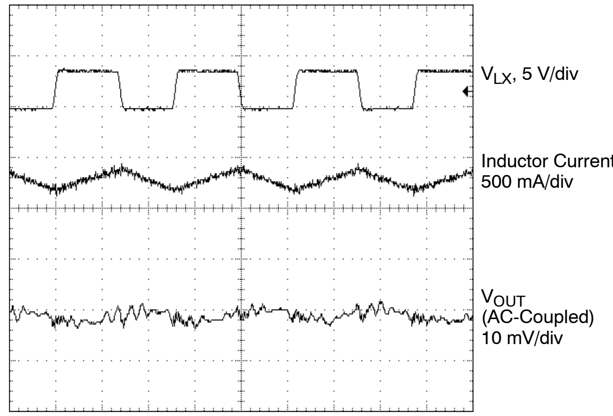
## TYPICAL WAVEFORMS ($V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.9 V)

PWM Mode Heavy-Load Switching Waveforms, $I_{OUT}$ = 600 mA, MODE = HIGH



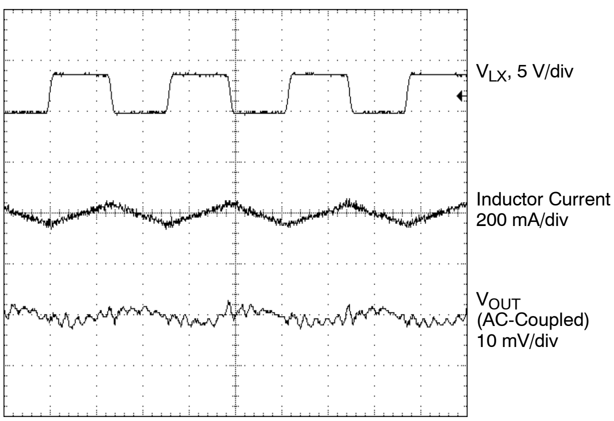

200 nS/div

PWM Mode Medium-Load Switching Waveforms, $I_{OUT}$ = 300 mA, MODE = HIGH



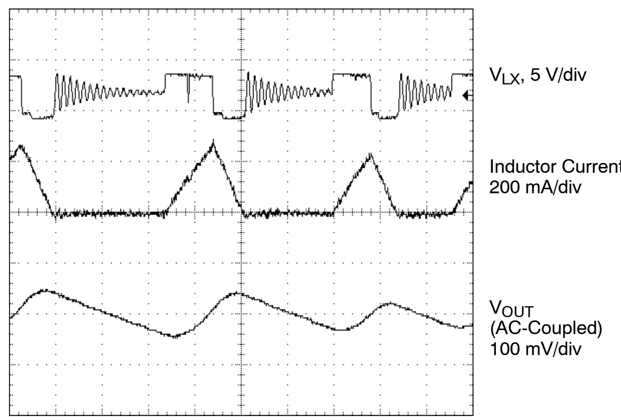

200 nS/div

PWM Mode Light-Load Switching Waveforms, $I_{OUT}$ = 0 mA, MODE = HIGH



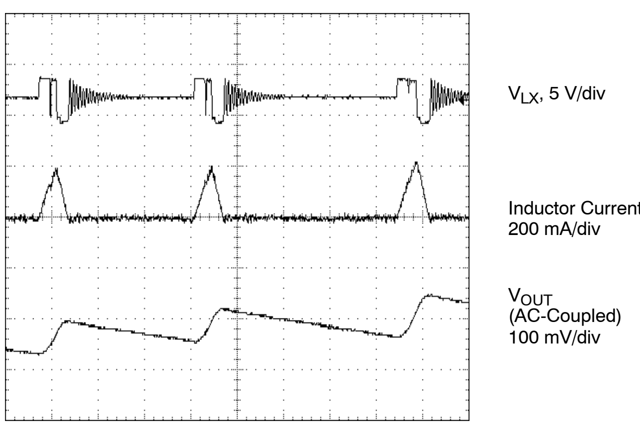

200 nS/div

PSM Mode Light-Load Switching Waveforms, $I_{OUT}$ = 150 mA, MODE = OPEN




1.0 µS/div

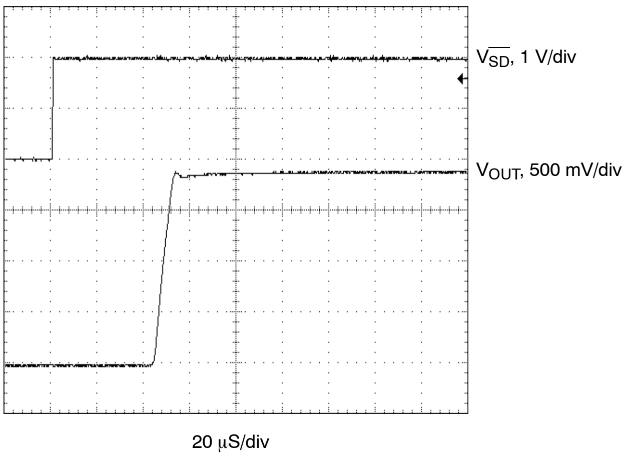
PSM Mode Light-Load Switching Waveforms, $I_{OUT}$ = 30 mA, MODE = OPEN



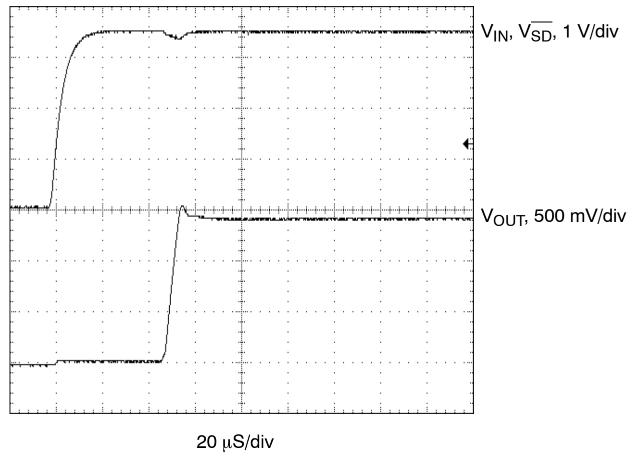

2.0 µS/div

## TYPICAL START-UP AND SHUTDOWN TRANSIENT WAVEFORMS ($V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.9 V)

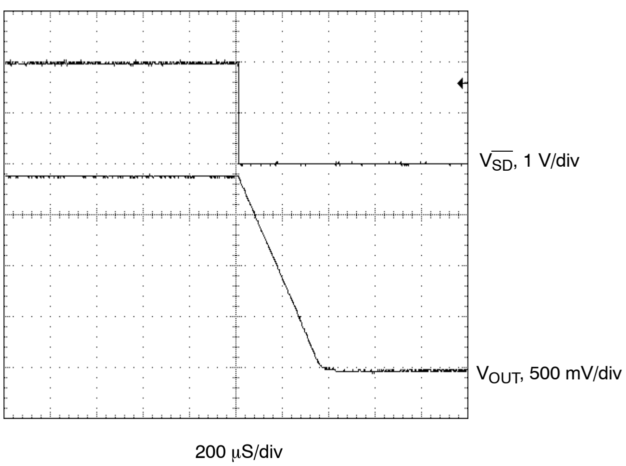
Start-Up, $R_{LOAD}$ = 4 Ω



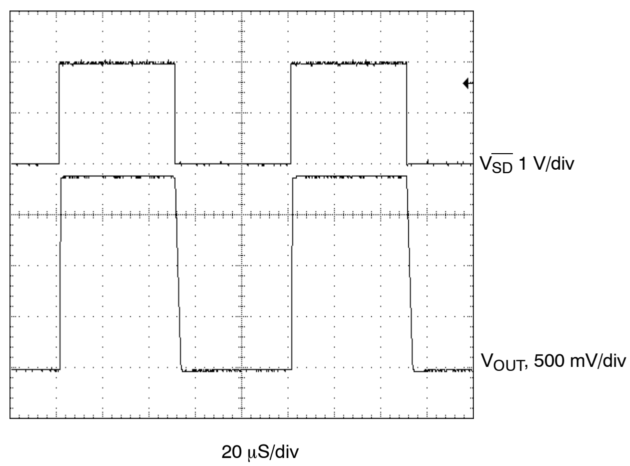

Start-Up, $V_{IN}$ = $V_{\overline{SD}}$ = 3.6 V, $R_{LOAD}$ = 4 Ω




Shutdown, $R_{LOAD}$ = 4 Ω

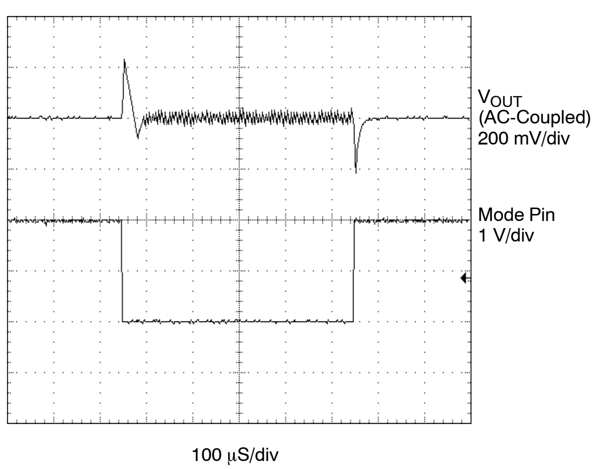



Enable Switching, $R_{LOAD}$ = 4 Ω



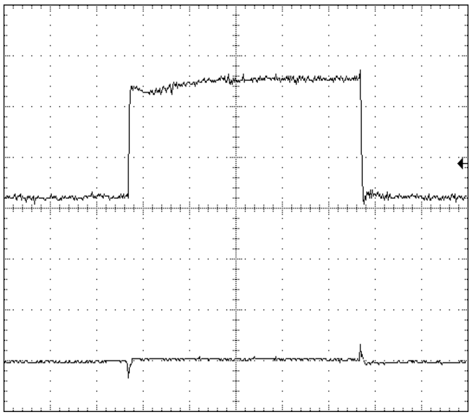

## TYPICAL MODE SWITCH TRANSIENT WAVEFORM

Output Transient At Mode Switch, $I_{LOAD}$ = 30 mA



## TYPICAL LOAD TRANSIENT WAVEFORMS ($V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.9 V)

Load Transient, Auto Mode, $I_{LOAD}$ = 30 to 500 mA, MODE = LOW

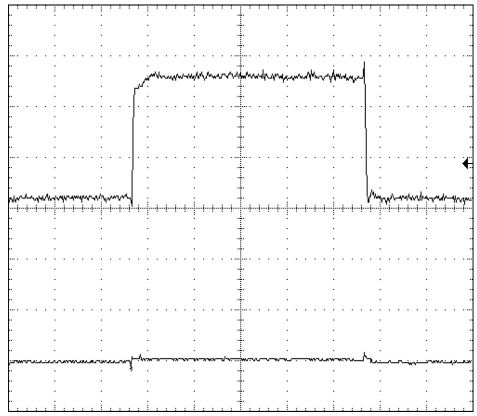


$I_{LOAD}$, 200 mA /div

$V_{OUT}$ (AC-Coupled) 50 V/div

10 µS/div

Load Transient, PWM Mode, $I_{LOAD}$ = 30 to 500 mA, L = 2.2 µH, MODE= HIGH

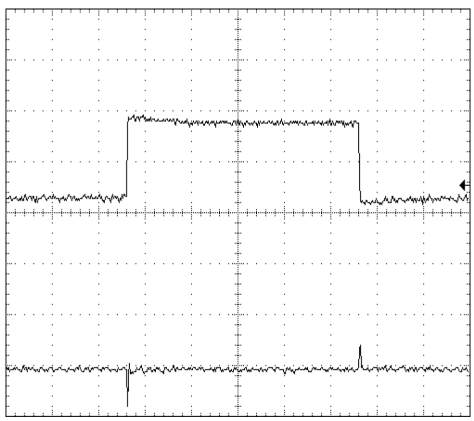


$I_{LOAD}$, 200 mA /div

$V_{OUT}$ (AC-Coupled) 50 mV/div

10 µS/div

Load Transient (PSM Mode), $I_{LOAD}$ = 30 to 150 mA, L = 2.2 µH



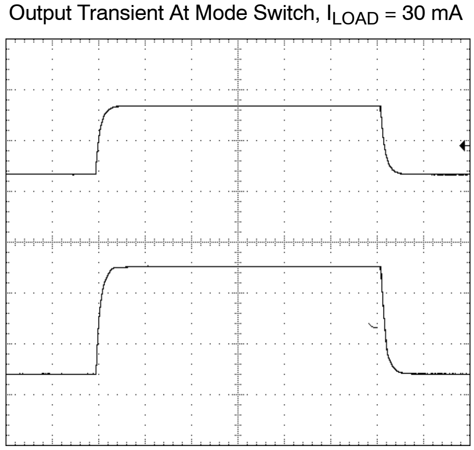
$I_{LOAD}$, 200 mA /div

$V_{OUT}$ (AC-Coupled) 50 mV/div

100 µS/div

## TYPICAL DAC INPUT RESPONSE WAVEFORM

Output Transient At Mode Switch, $I_{LOAD}$ = 30 mA



$V_{DAC}$, 1 V/div

$V_{OUT}$, 1 V/div

100 µS/div

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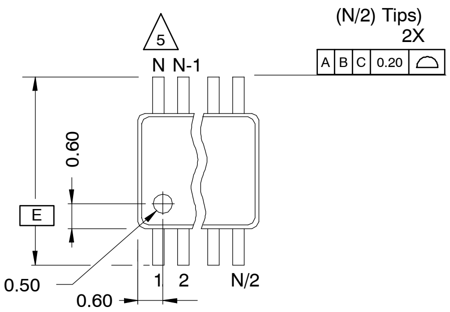
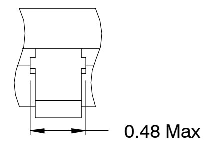
## MSOP: 10-LEADS (POWER IC ONLY)

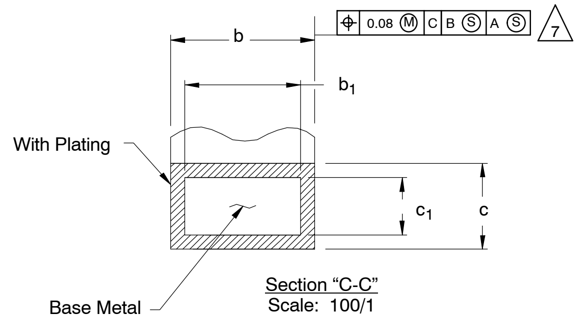
**JEDEC Part Number: MO-187, (Variation AA and BA)**



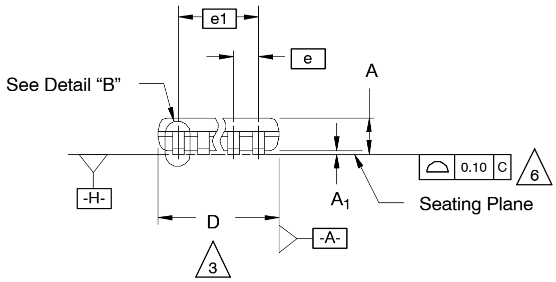

Top View



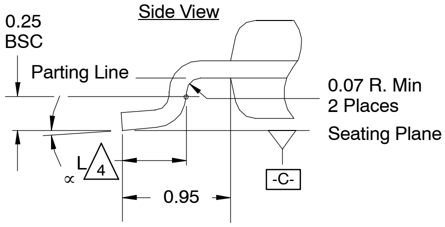

Detail "B"
(Scale: 30/1)
Dambar Protrusion



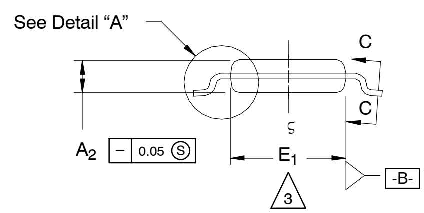

Section "C-C"
Scale: 100/1
(See Note 8)




Side View




Detail "A"
(Scale: 30/1)




End View

NOTES:

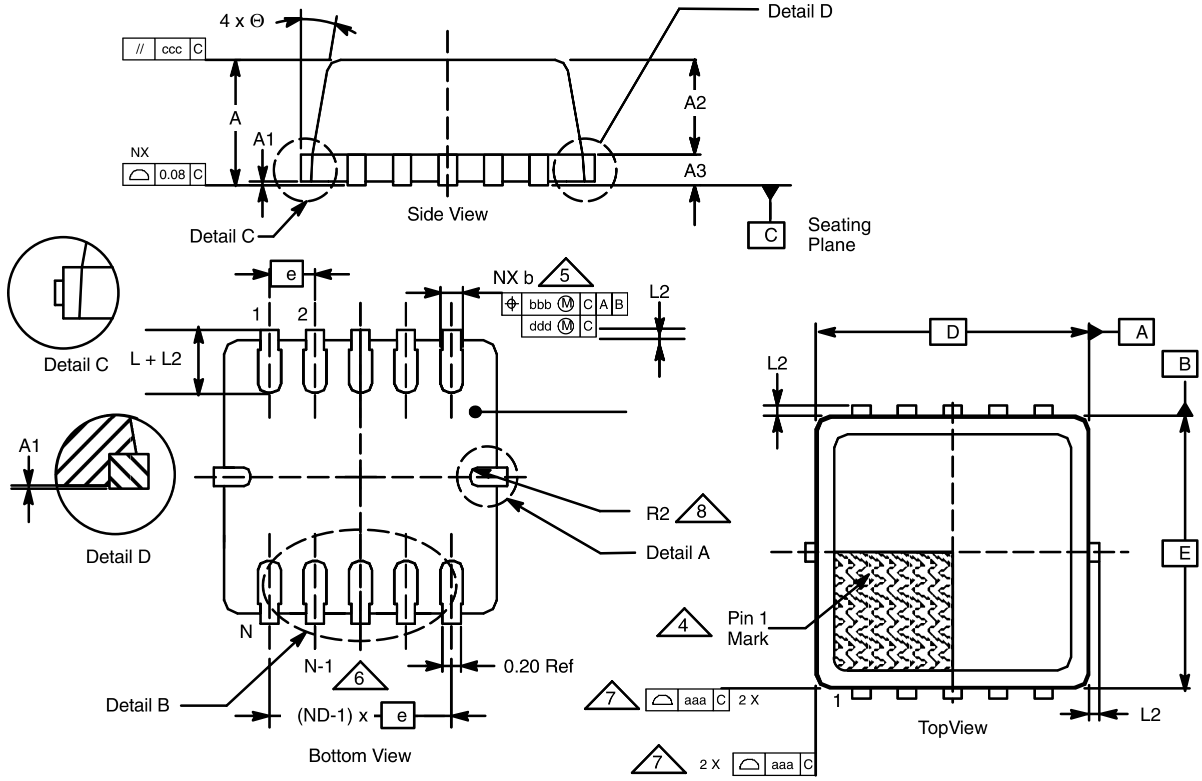
1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "$E_1$" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

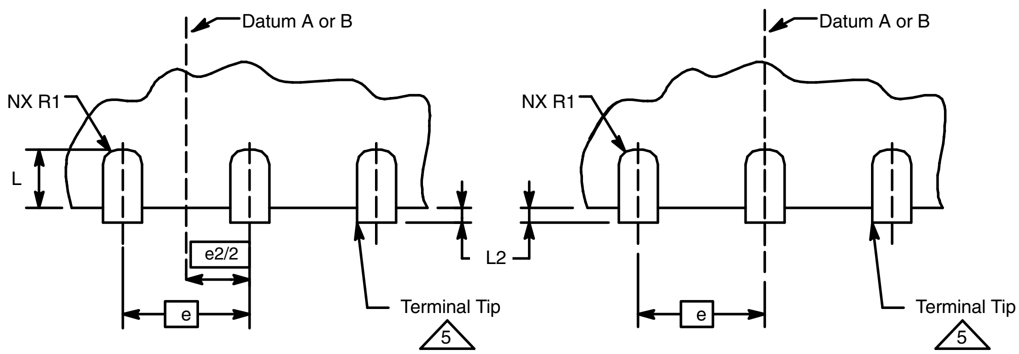
**N = 10L**

| Dim | MILLIMETERS | | | Note |
|---|---|---|---|---|
| | Min | Nom | Max | |
| A | – | – | 1.10 | |
| $A_1$ | 0.05 | 0.10 | 0.15 | |
| $A_2$ | 0.75 | 0.85 | 0.95 | |
| b | 0.17 | – | 0.27 | 8 |
| $b_1$ | 0.17 | 0.20 | 0.23 | 8 |
| c | 0.13 | – | 0.23 | |
| $c_1$ | 0.13 | 0.15 | 0.18 | |
| D | | 3.00 BSC | | 3 |
| E | | 4.90 BSC | | |
| $E_1$ | 2.90 | 3.00 | 3.10 | 3 |
| e | | 0.50 BSC | | |
| $e_1$ | | 2.00 BSC | | |
| L | 0.40 | 0.55 | 0.70 | 4 |
| N | | 10 | | 5 |
| ∝ | 0° | 4° | 6° | |
| ECN: S-40082—Rev. A, 02-Feb-04<br>DWG: 5922 | | | | |

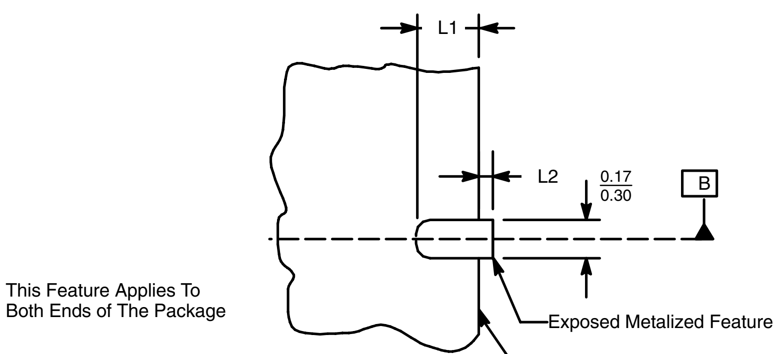
## MLP33-10 (POWER IC ONLY)

**JEDEC Part Number: Outline is consistent with JEDEC MO229-VEED-2**




Detail B




Detail A

### MLP33-10 (POWER IC ONLY)

**N = 10 PITCH: 0.50 mm, BODY SIZE: 3.00 x 3.00**

| Dim | MILLIMETERS* | | | INCHES | | | Notes |
|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max | |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 | 1, 2 |
| A1 | 0 | 0.025 | 0.05 | 0 | 0.001 | 0.002 | 1, 2 |
| A2 | 0.65 | 0.70 | 0.75 | 0.026 | 0.028 | 0.030 | 1, 2 |
| A3 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 | 1, 2 |
| aaa | – | 0.10 | – | – | 0.004 | – | 1, 2 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 | 5, 11 |
| bbb | – | 0.10 | – | – | 0.004 | – | 1, 2 |
| ccc | – | 0.10 | – | – | 0.004 | – | 1, 2 |
| D | 3.00 BSC | | | 0.118 BSC | | | 1, 2 |
| ddd | – | 0.05 | – | | 0.002 | | 1, 2 |
| E | 3.00 BSC | | | 0.118 BSC | | | 1, 2 |
| e | – | 0.5 | – | – | 0.002 | – | |
| e2 | 1.10 | 1.20 | 1.30 | 0.043 | 0.047 | 0.051 | 1, 2, 9 |
| L | 0.45 | 0,58 | 0.65 | 0.018 | 0.023 | 0.026 | 1, 2 |
| L1 | 0.20 | 0.29 | 0.45 | 0.008 | 0.012 | 0.018 | 1, 2 |
| L2 | – | – | 0.125 | – | – | 0.005 | 5, 11 |
| N | 10 | | | 10 | | | 3 |
| ND | 5 | | | 5 | | | 6 |
| R1 Ref | – | 0.100 | – | – | | – | 5, 11 |
| R2 Ref | – | 0.075 | – | – | 0.003 | – | 1, 2 |
| Θ | 0° | 10° | 12° | 0° | 10° | 12° | 1, 2 |

* Use millimeters as the primary measurement.

ECN: S-52448—Rev. B, 28-Nov-05
DWG: 5924

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be a molded, marked, or metallized feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.20 mm from the terminal tip.
6. ND refers to the maximum number of terminals on the D side.
7. Profile tolerance (aaa) will be applicable only to the plastic body and not to the metallized features (such as the terminal tips and tie bars.) Metallized features may protrude a maximum of L2 from the plastic body profile.
8. The corner will be sharp unless otherwise specified with radius dimensions.
9. Package outline is consistent with JEDEC M0229-VEED-2.

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