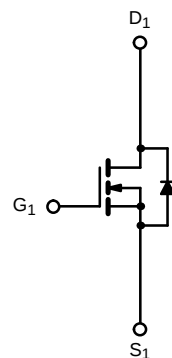
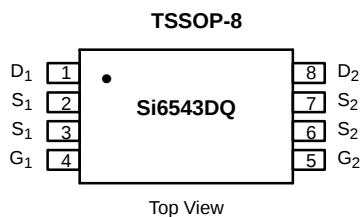


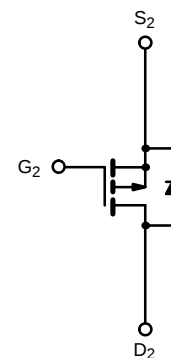


Dual N- and P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ $V_{GS} = 10$ V	± 3.9
		0.095 @ $V_{GS} = 4.5$ V	± 3.1
P-Channel	-30	0.085 @ $V_{GS} = -10$ V	± 2.5
		0.19 @ $V_{GS} = -4.5$ V	± 1.8



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter			Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage			V _{DS}	30	−30	V
Gate-Source Voltage			V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150 °C) ^a		T _A = 25 °C	I _D	± 3.9	± 2.5	A
		T _A = 70 °C		± 3.1	± 2.1	
Pulsed Drain Current			I _{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a			I _S	1.25	−1.25	
Maximum Power Dissipation ^a		T _A = 25 °C	P _D	1.0		W
		T _A = 70 °C		0.64		
Operating Junction and Storage Temperature Range			T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0			V
		V _{DS} = V _{GS} , I _D = −250 μA	P-Ch	−1.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	N-Ch P-Ch			±100 ±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch			1	μA
		V _{DS} = −30 V, V _{GS} = 0 V	P-Ch			−1	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			25	
		V _{DS} = −30 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			−25	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	15			A
		V _{DS} ≥ −5 V, V _{GS} = −10 V	P-Ch	−15			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 3.9 A	N-Ch		0.043	0.065	Ω
		V _{GS} = −10 V, I _D = 2.5 A	P-Ch		0.066	0.085	
		V _{GS} = 4.5 V, I _D = 3.1 A	N-Ch		0.075	0.095	
		V _{GS} = −4.5 V, I _D = 1.8 A	P-Ch		0.125	0.19	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 3.9 A	N-Ch		7		S
		V _{DS} = −15 V, I _D = −2.5 A	P-Ch		5		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V
		I _S = −1.25 A, V _{GS} = 0 V	P-Ch		0.8	−1.2	
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 3.9 A P-Channel V _{DS} = −10 V, V _{GS} = −10 V, I _D = −2.5 A	N-Ch P-Ch		9.8 8.7	15 15	nC
Gate-Source Charge	Q _{gs}		N-Ch P-Ch		2.1 1.9		
Gate-Drain Charge	Q _{gd}		N-Ch P-Ch		1.6 1.3		
Turn-On Delay Time	t _{d(on)}		N-Ch P-Ch		9 7	15 15	
Rise Time	t _r	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = −10 V, R _L = 10 Ω I _D ≅ −1 A, V _{GEN} = −10 V, R _G = 6 Ω	N-Ch P-Ch		6 9	18 18	ns
Turn-Off Delay Time	t _{d(off)}		N-Ch P-Ch		18 14	27 27	
Fall Time	t _f		N-Ch P-Ch		6 8	15 15	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.25 A, di/dt = 100 A/μs I _F = −1.25 A, di/dt = 100 A/μs	N-Ch P-Ch		48 46	

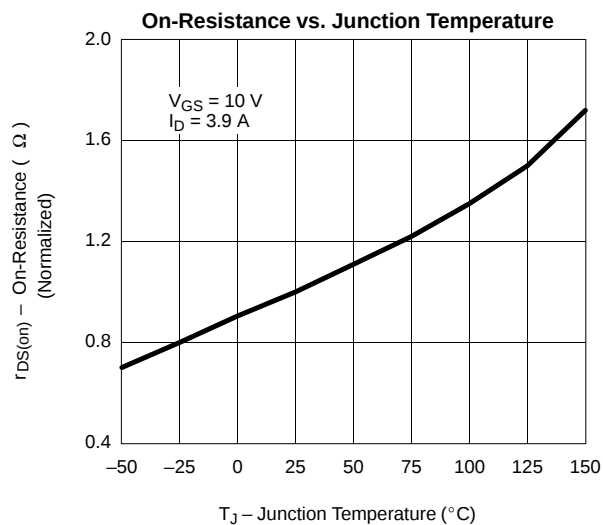
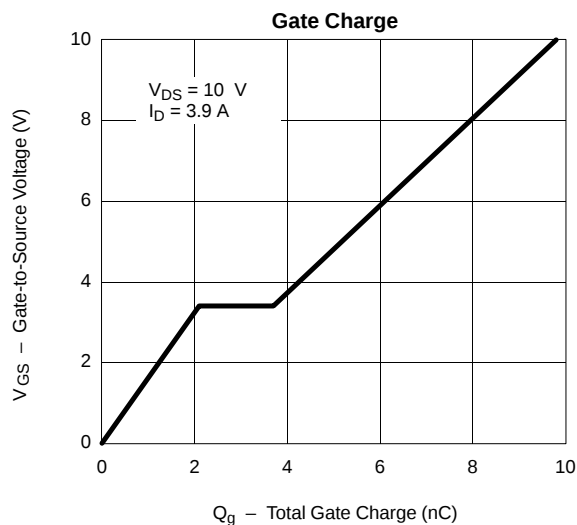
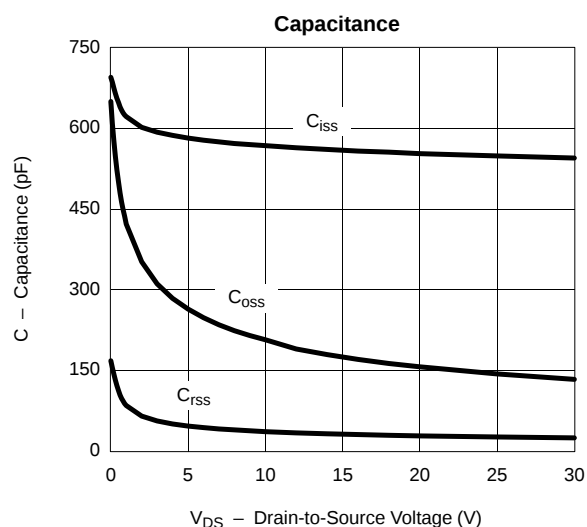
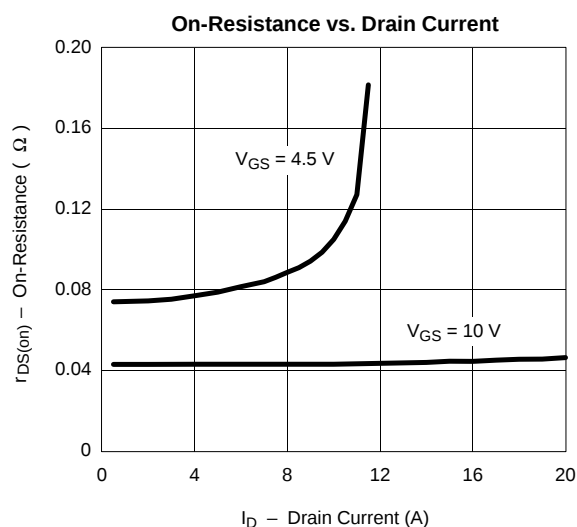
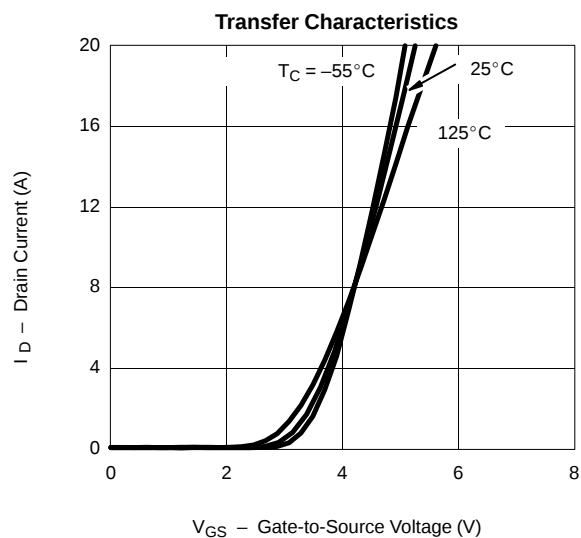
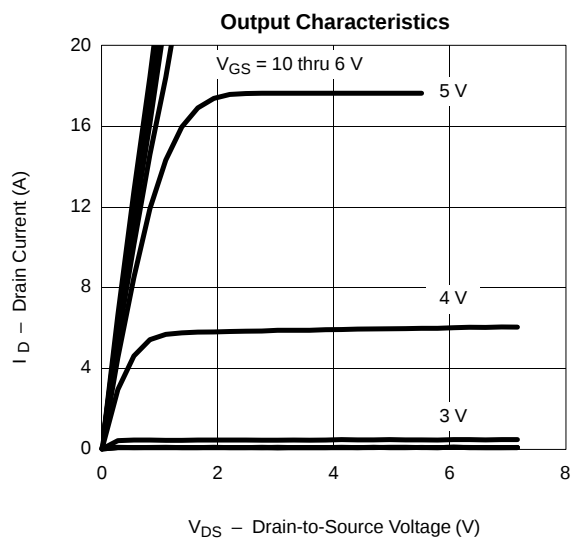
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.



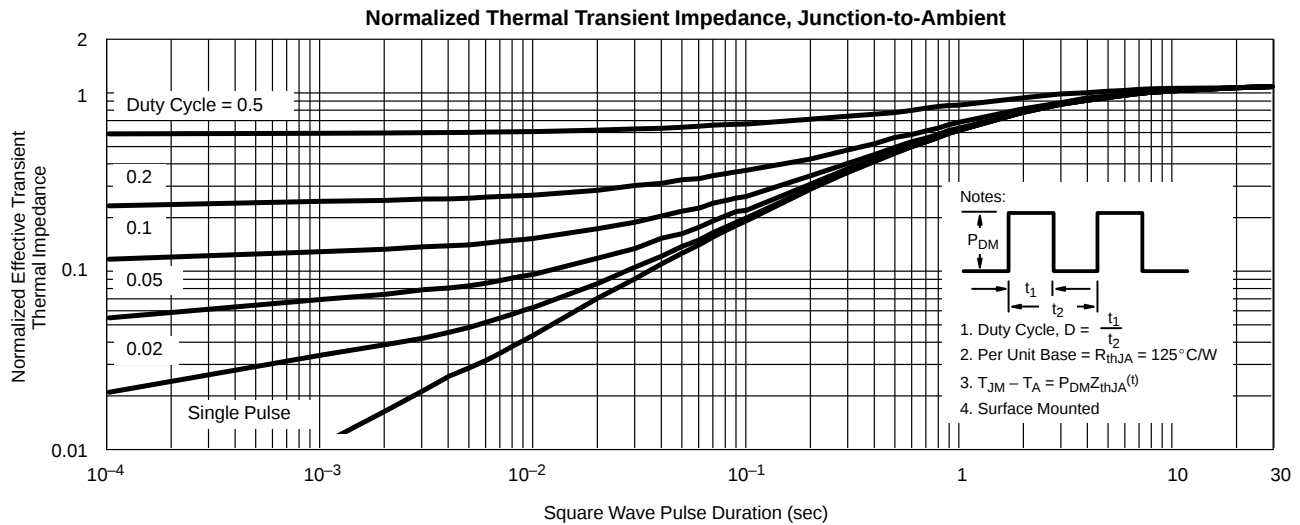
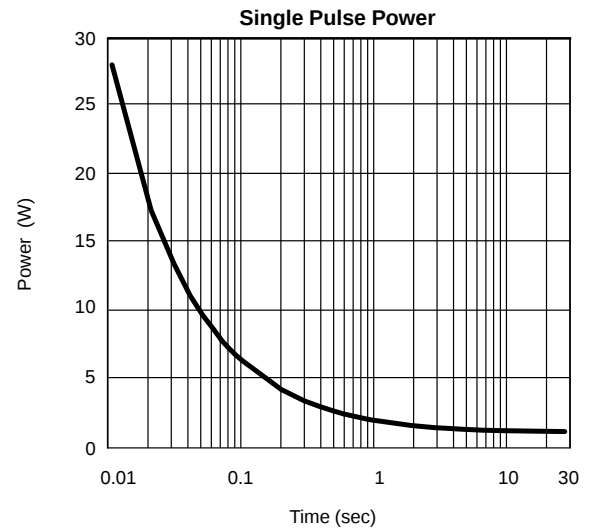
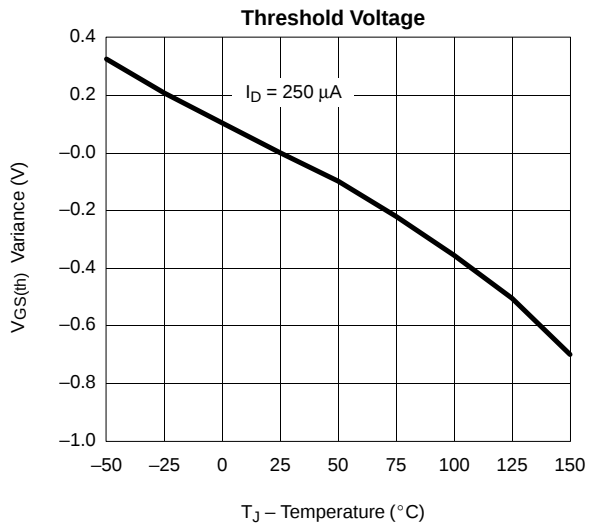
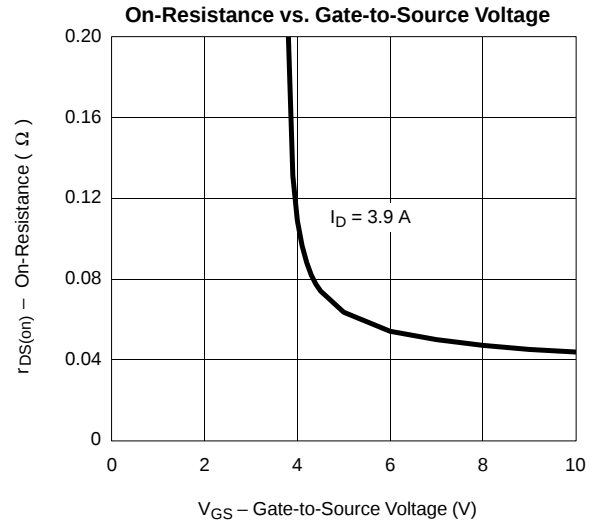
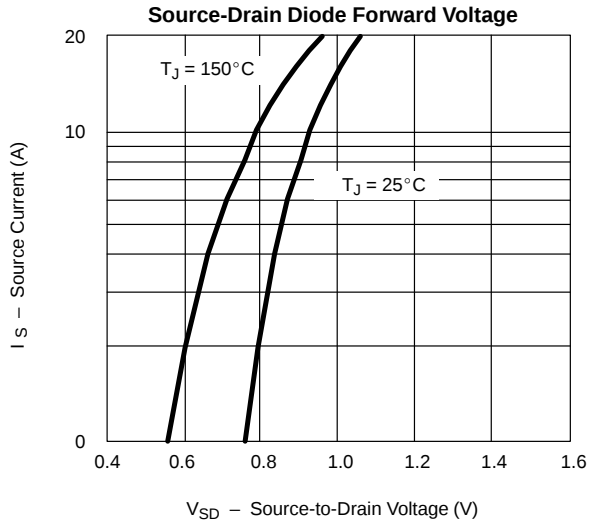
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

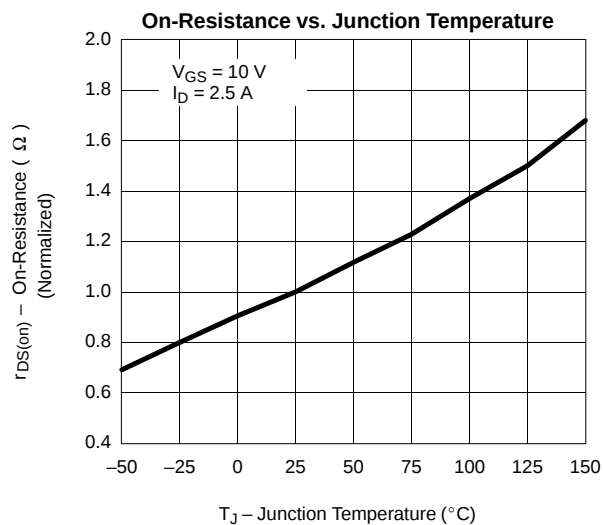
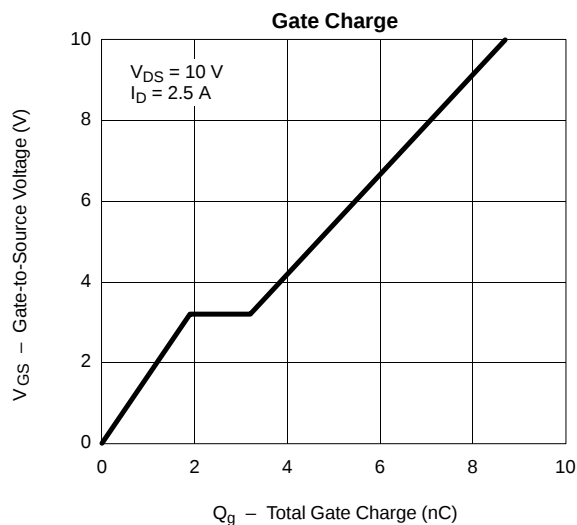
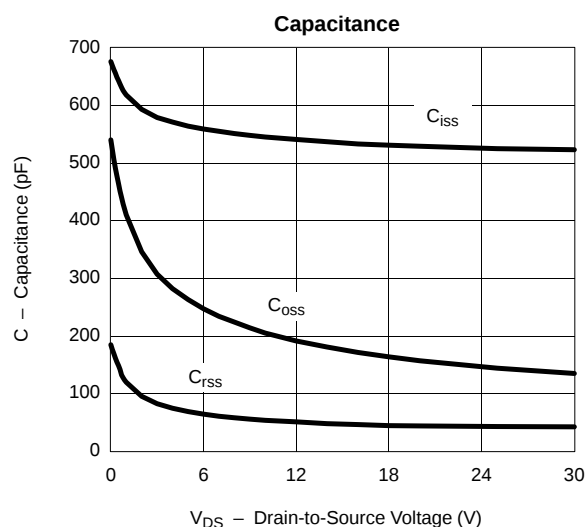
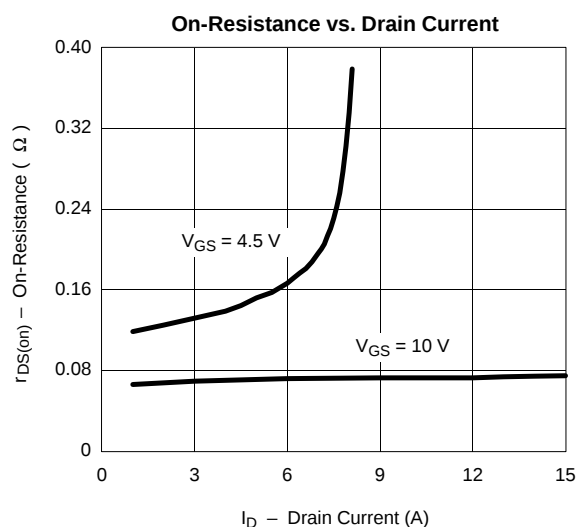
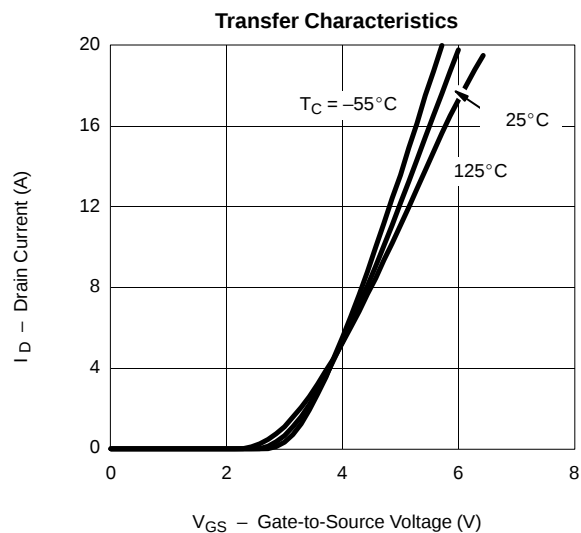
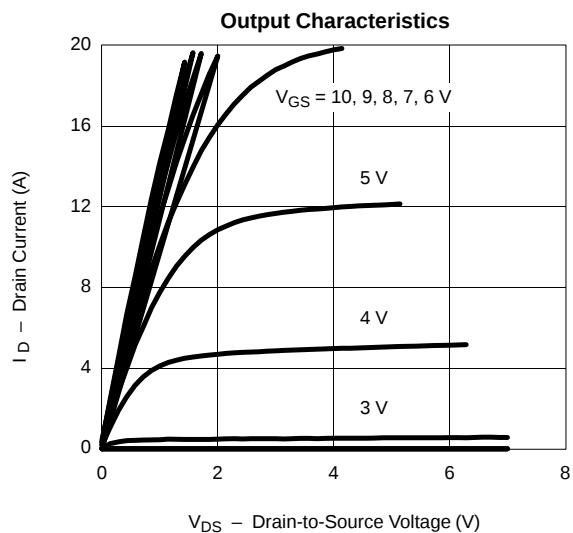
N-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL

