

# 4V Drive Nch MOS FET

## 2SK2094

### ●Structure

Silicon N-channel MOS FET

### ●Features

- 1) Low On-resistance.
- 2) Fast switching speed.
- 3) Wide SOA (safe operating area).
- 4) 4V drive.
- 5) Drive circuits can be simple.
- 6) Parallel use is easy.

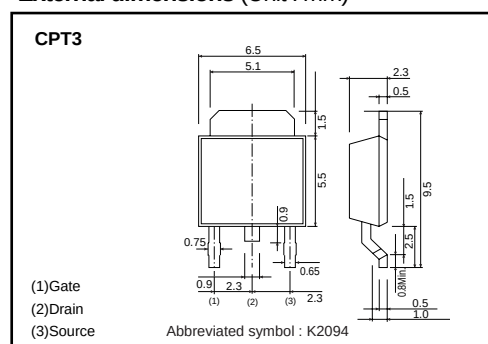
### ●Applications

Switching

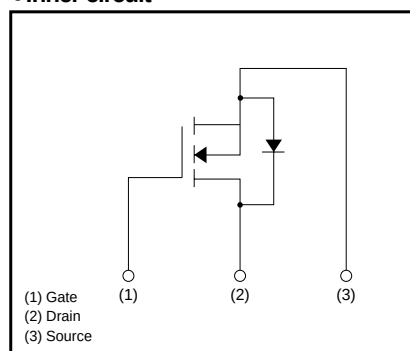
### ●Packaging specifications

|         |                              |        |
|---------|------------------------------|--------|
| Type    | Package                      | Taping |
|         | Code                         | TL     |
|         | Basic ordering unit (pieces) | 2500   |
| 2SK2094 |                              | ○      |

### ●External dimensions (Unit : mm)



### ●Inner circuit



### ●Absolute maximum ratings (Ta=25°C)

| Parameter                         |            | Symbol      | Limits      | Unit |
|-----------------------------------|------------|-------------|-------------|------|
| Drain-source voltage              |            | $V_{DS}$    | 60          | V    |
| Gate-source voltage               |            | $V_{GS}$    | $\pm 20$    | V    |
| Drain current                     | Continuous | $I_D$       | 2           | A    |
|                                   | Pulsed     | $I_{DP}^*$  | 8           | A    |
| Reverse drain current             | Continuous | $I_{DR}$    | 2           | A    |
|                                   | Pulsed     | $I_{DRP}^*$ | 8           | A    |
| Total power dissipation (Tc=25°C) |            | $P_D$       | 10          | W    |
| Channel temperature               |            | $T_{ch}$    | 150         | °C   |
| Storage temperature               |            | $T_{stg}$   | -55 to +150 | °C   |

\*  $P_w \leq 300\mu s$ , Duty cycle  $\leq 2\%$

## Transistors

## ●Electrical characteristics (Ta=25°C)

| Parameter                               | Symbol        | Min. | Typ. | Max.      | Unit     | Test Conditions                                     |
|-----------------------------------------|---------------|------|------|-----------|----------|-----------------------------------------------------|
| Gate-source leakage                     | $I_{GSS}$     | –    | –    | $\pm 100$ | nA       | $V_{GS} = \pm 20V$ , $V_{DS} = 0V$                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | 60   | –    | –         | V        | $I_D = 1mA$ , $V_{GS} = 0V$                         |
| Zero gate voltage drain current         | $I_{DSS}$     | –    | –    | 100       | $\mu A$  | $V_{DS} = 60V$ , $V_{GS} = 0V$                      |
| Gate threshold voltage                  | $V_{GS(th)}$  | 1.0  | –    | 2.5       | V        | $V_{DS} = 10V$ , $I_D = 1mA$                        |
| Static drain-source on-state resistance | $R_{DS(on)}$  | –    | 0.3  | 0.35      | $\Omega$ | $I_D = 1A$ , $V_{GS} = 10V$                         |
|                                         |               | –    | 0.4  | 0.5       |          | $I_D = 1A$ , $V_{GS} = 4V$                          |
| Forward transfer admittance             | $ Y_{fs} $    | 1.0  | –    | –         | S        | $V_{DS} = 10V$ , $I_D = 1A$                         |
| Input capacitance                       | $C_{iss}$     | –    | 400  | –         | pF       | $V_{DS} = 10V$                                      |
| Output capacitance                      | $C_{oss}$     | –    | 150  | –         | pF       | $V_{GS} = 0V$                                       |
| Reverse transfer capacitance            | $C_{rss}$     | –    | 50   | –         | pF       | $f = 1MHz$                                          |
| Turn-on delay time                      | $t_{d(on)}$   | –    | 10   | –         | ns       | $I_D = 1A$ , $V_{DD} = 30V$                         |
| Rise time                               | $t_r$         | –    | 20   | –         | ns       | $V_{GS} = 10V$                                      |
| Turn-off delay time                     | $t_{d(off)}$  | –    | 100  | –         | ns       | $R_L = 30\Omega$                                    |
| Fall time                               | $t_f$         | –    | 40   | –         | ns       | $R_G = 10\Omega$                                    |
| Reverse recovery time (Body Diode)      | $t_{rr}$      | –    | 100  | –         | ns       | $I_{DR} = 2A$ , $V_{GS} = 0V$ , $di/dt = 50A/\mu s$ |

## Transistors

## ●Electrical characteristics curve

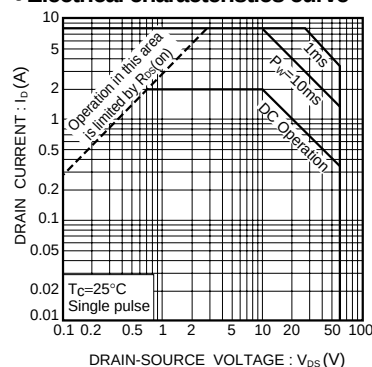


Fig.1 Maximum Safe Operating Area

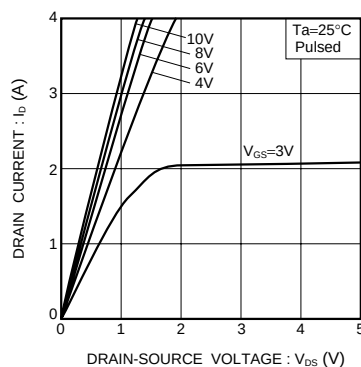


Fig.2 Typical Output Characteristics

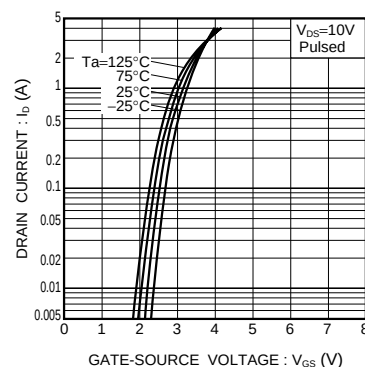


Fig.3 Typical Transfer Characteristics

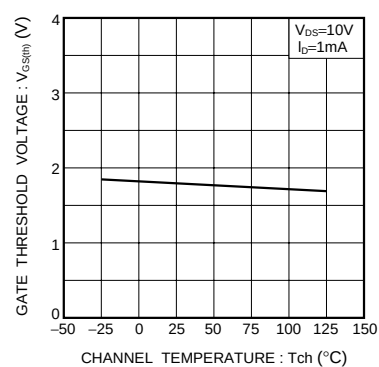


Fig.4 Gate Threshold Voltage vs. Channel Temperature

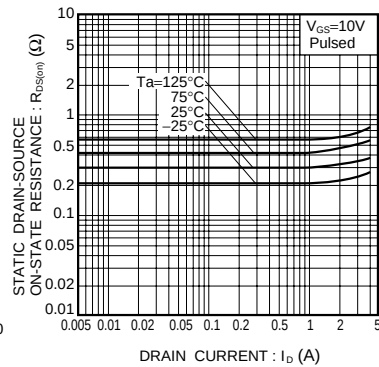


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (I)

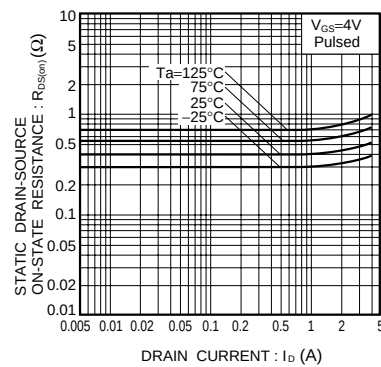


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (II)

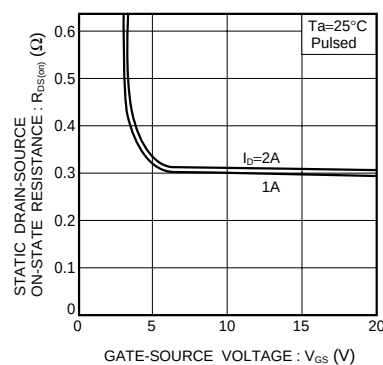


Fig.7 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

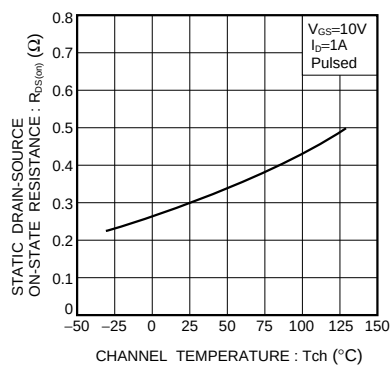


Fig.8 Static Drain-Source On-State Resistance vs. Channel Temperature

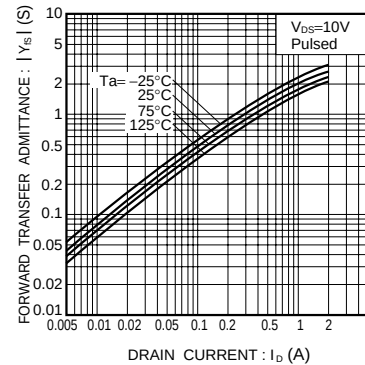


Fig.9 Forward Transfer Admittance vs. Drain Current

## Transistors

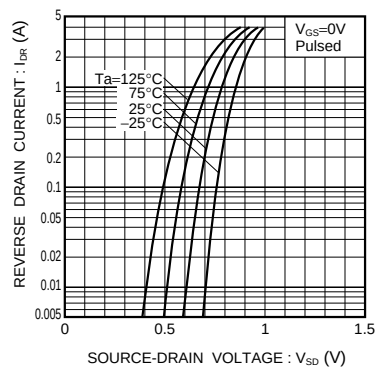


Fig.10 Reverse Drain Current vs. Source-Drain Voltage (I)

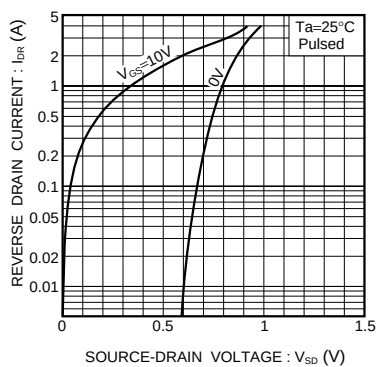


Fig.11 Reverse Drain Current vs. Source-Drain Voltage (II)

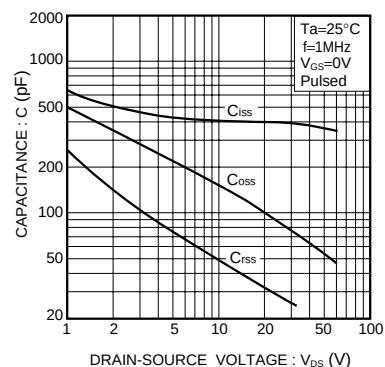


Fig.12 Typical Capacitance vs. Drain-Source Voltage

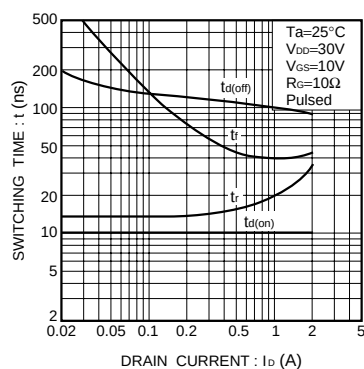


Fig.13 Switching characteristics (See Figure. 15 and 16 for the measurement circuit and resultant waveforms)

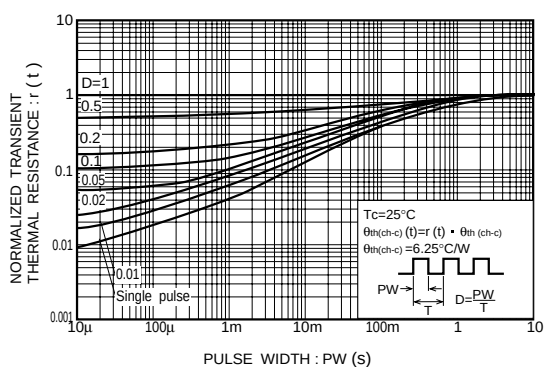


Fig.14 Normalized Transient Thermal Resistance vs. Pulse Width

## ● Switching characteristics measurement circuit

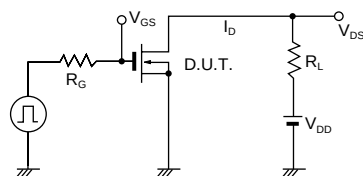


Fig.15 Switching Time Test Circuit

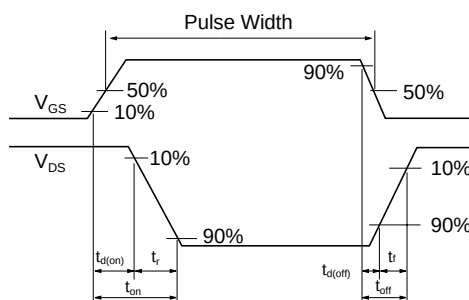


Fig.16 Switching Time Waveforms

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