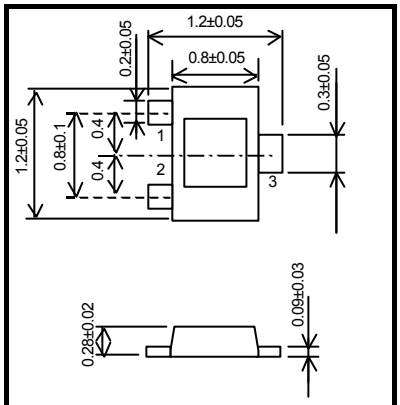
TOSHIBA Field Effect Transistor Silicon N Channel Junction Type

# 2SK3582TV

For ECM

- Application for Ultra-compact ECM

Unit: mm




1.Drain
2.Source
3.Gate

VESM2

| | |
|---|---|
| JEDEC | - |
| JEITA | - |
| TOSHIBA | 2-1H1A |

Weight: 0.8mg (typ.)

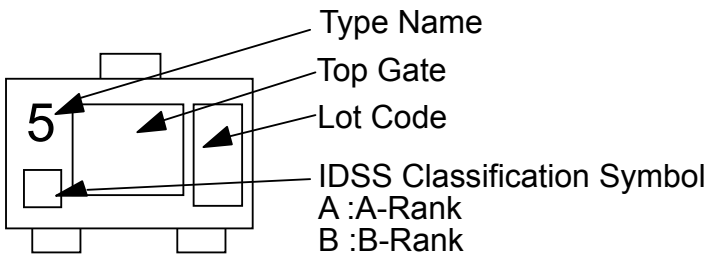
## Absolute Maximum Ratings (Ta=25°C)

| Characteristic | Symbol | Rating | Unit |
|---|---|---|---|
| Gate-Drain voltage | $V_{GDO}$ | -20 | V |
| Gate Current | $I_G$ | 10 | mA |
| Drain power dissipation (Ta = 25°C) | $P_D$ | 100 | mW |
| Junction Temperature | $T_j$ | 125 | °C |
| Storage temperature range | $T_{stg}$ | −55~125 | °C |

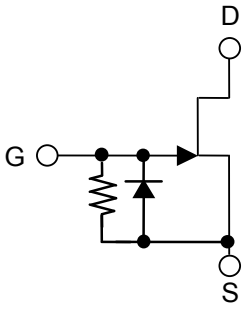
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

IDSS CLASSIFICATION
A-Rank 80 to 200 μA
B-Rank 170 to 300μA

## Marking




## Equivalent Circuit




## Precaution

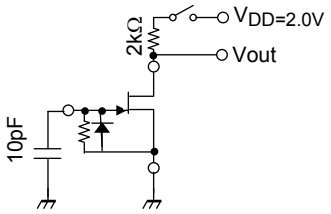
There is a metal plate on the top of package, which has the same electrical potential as the Gate terminal. Don’t use it as a terminal.

## Electrical Characteristics (Ta=25°C)

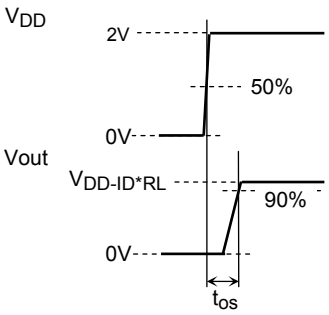
| Characteristic | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Drain Current | $I_{DSS}$ | $V_{DS}$ = 2 V, $V_{GS}$ = 0 | 80 | — | 300 | μA |
| Drain Current | $I_D$ | $V_{DD}$ = 2 V, RL= 2kΩ,Cg = 10pF | — | — | 340 | μA |
| Gate-Source Cut-off Voltage | $V_{GS(OFF)}$ | $V_{DS}$ = 2 V, $I_D$ = 1μA | -0.1 | — | -0.65 | V |
| Forward transfer admittance | $\|Y_{fs}\|$ | $V_{DS}$ = 2 V,$V_{GS}$ = 0V | 0.55 | 1.0 | — | mS |
| Gate-Drain Voltage | $V_{(BR)GDO}$ | IG=-10μA | -20 | — | — | V |
| Input capacitance | $C_{iss}$ | $V_{DS}$ = 2 V, $V_{GS}$ = 0, f = 1 MHz | — | 3.6 | — | pF |
| Voltage Gain | Gv | $V_{DD}$ = 2V, RL= 2kΩ,Cg = 10pF, f = 1kHz,vin=100mV | -5.0 | 0 | +2.0 | dB |
| Delta Voltage Gain | DGv(f) | $V_{DD}$ = 2V, RL= 2kΩ,Cg = 10pF,f = 1kHz to 100Hz,vin=100mV | — | 0 | -1.0 | dB |
| Delta Voltage Gain | DGv(V) | $V_{DD}$ = 2V to 1.5V, RL= 2kΩ,Cg = 10pF,f = 1kHz, vin=100mV | — | -1.0 | -3.0 | dB |
| Noise Voltage | VN | $V_{DD}$ = 2V, RL= 1kΩ,Cg = 10pF,Gv=80dB, A-Curve Filter | — | — | 50 | mV |
| Total Harmonic Distortion | THD | $V_{DD}$ = 2V, RL= 2kΩ,Cg = 10pF, f = 1kHz, vin=50mV | — | 1.0 | — | % |
| Time Output Stability | tos | $V_{DD}$ = 2V, RL= 2kΩ,Cg = 10pF | — | 100 | 200 | ms |

## Time Output Stability Test Method

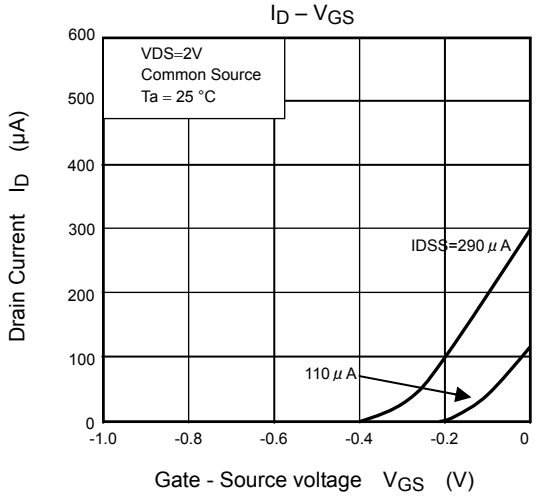
a) TEST CIRCUIT



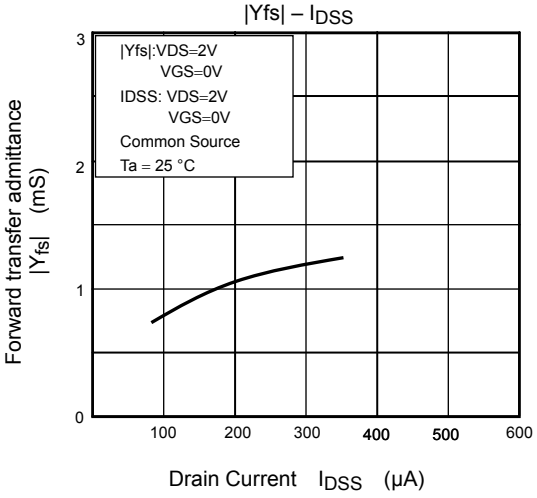

b) TEST SIGNAL



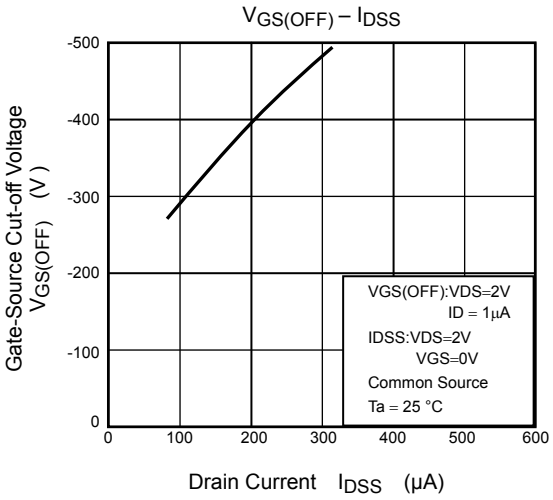
$I_D - V_{GS}$



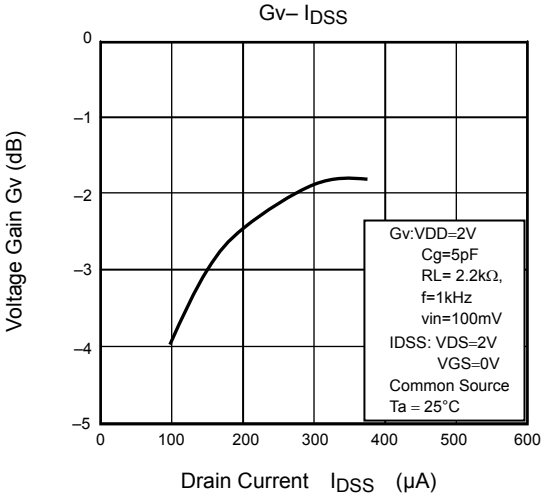

$|Yfs| - I_{DSS}$



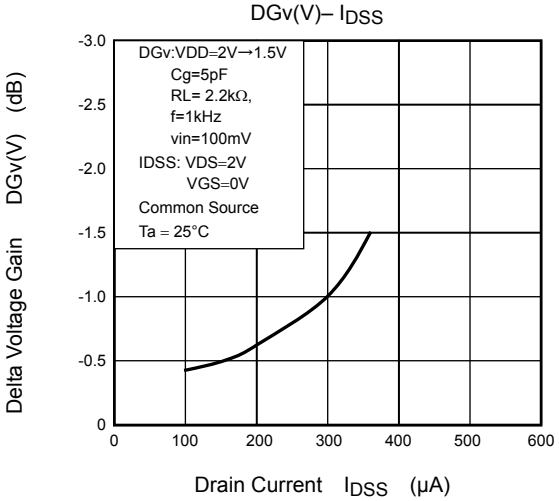

$V_{GS(OFF)} - I_{DSS}$



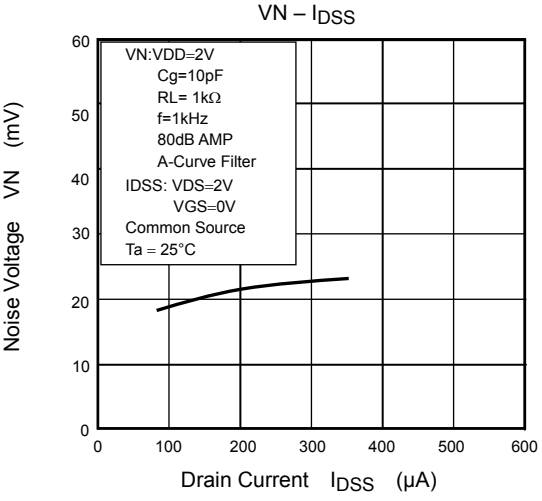

$Gv - I_{DSS}$

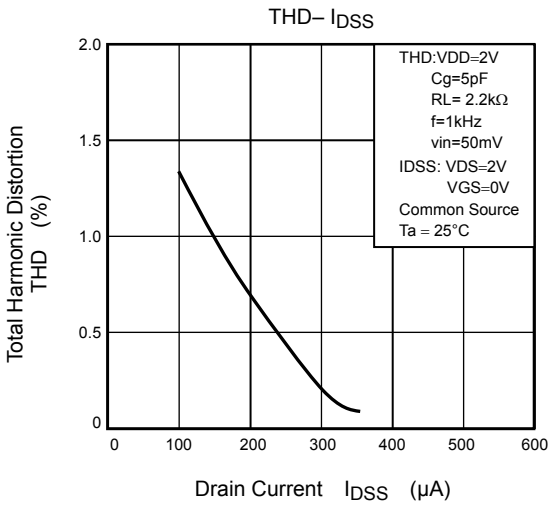


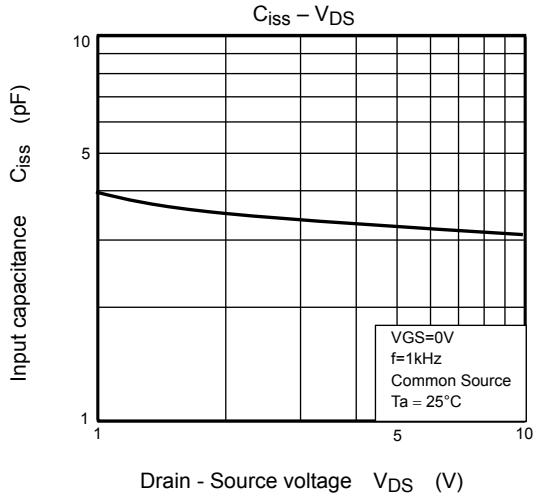

$DGv(V) - I_{DSS}$




$VN - I_{DSS}$




THD– IDSS
Total Harmonic Distortion THD (%)
2.0
1.5
1.0
0.5
0
0
100
200
300
400
500
600
THD:VDD=2V
Cg=5pF
RL= 2.2kΩ
f=1kHz
vin=50mV
IDSS: VDS=2V
VGS=0V
Common Source
Ta = 25°C
Drain Current IDSS (μA)


Ciss – VDS
Input capacitance Ciss (pF)
10
5
1
1
5
10
VGS=0V
f=1kHz
Common Source
Ta = 25°C
Drain - Source voltage VDS (V)

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20070701-EN GENERAL

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