NEC

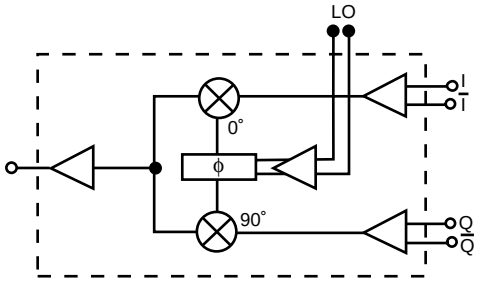
SILICON MMIC QUADRATURE MODULATOR

UPC8105GR

FEATURES

- **WIDE SUPPLY VOLTAGE RANGE:** 2.7 ~ 5.5 V
- **BROADBAND OPERATION:**
  MOD_{OUT} = 100 - 400 MHz, I/Q = DC to 10 MHz
- **INTERNAL 90° PHASE SHIFTER**
- **POWER SAVE FUNCTION**
- **LOW POWER CONSUMPTION:** 16 mA Typ. @ 3 V
- **SMALL SSOP 16 PACKAGE**
- **TAPE AND REEL PACKAGING AVAILABLE**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The UPC8105GR Silicon MMIC I/Q Modulator is manufactured using the NESAT III MMIC process. The NESAT III process produces transistors with f_T approaching 20 GHz. The device was designed for use in Digital Mobile Communications circuits such as 900 MHz Digital Cordless and Cellular Phones, WLAN and PCN/PCS Handset Transmitters.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, $V_{PS} \geq$ 1.8 V)

PART NUMBER PACKAGE OUTLINE				UPC8105GR S16 (SSOP 16)		
SYMBOLS	**PARAMETERS AND CONDITIONS**		**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Total Circuit Current (no signal) $V_{PS} \geq$ 1.8 V $V_{PS} \leq$ 1.0 V		mA μA	10	16 0.1	21 5
P_{MOD}	Output Power - Modulator	$V_{I/Q}$ = 1.5 V (DC) + 500 mVp-p (AC)	dBm	-21	-16.5	-12
LO_{LEAK}	Local Oscillator Leakage		dBc		-40	-30
ImR	Image Rejection		dBc		-40	-30
$IM3_{I/Q}$	I/Q 3rd Order Intermodulation Distortion		dBc		-50	
RL_{IN}	I/Q LO Input Return Loss		dB		20	
$Z_{I/Q}$	Input Impedance I and Q Port		kΩ		20	
T_{PS}(RISE)	Power Save Rise Time $V_{PS} \leq$ 1.0 V to $V_{PS} \geq$ 1.8V		μS		2	5
T_{PS} (FALL)	Power Save Fall Time $V_{PS} \geq$1.8 V to $V_{PS} \leq$1.0 V		μS		2	5

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	6.0
V_{PS}	Enable Voltage for Power Save	V	6.0
P_D	Power Dissipation[2]	mW	530
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-65 to +150

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50x50x1.6 mm double copper clad epoxy glass PWB (T_A = 85°C).

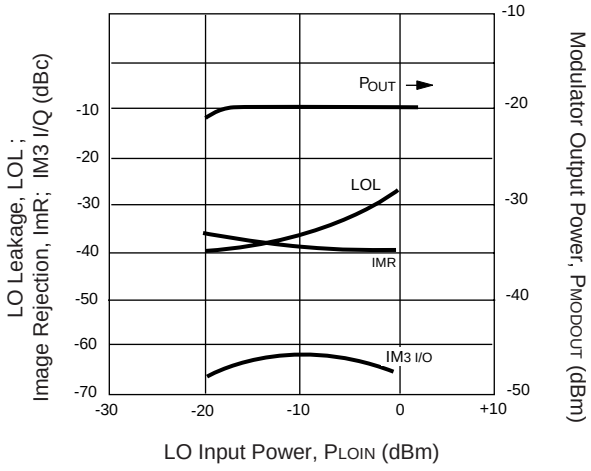
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	5.5
T_{OP}	Operating Temperature	°C	-40	+25	+85
f_{MODOUT}	Modulator Output Frequency	MHz	100		400
f_{LOIN}	LO1 Input Frequency[1]	MHz	100		400
$f_{I/QIN}$	I/Q Input Frequency[2]	MHz	DC		10

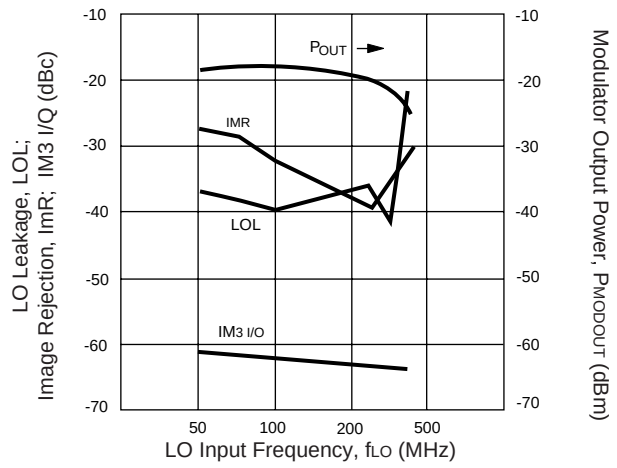
Notes:
1. P_{LOIN} = -10 dBm.
2. $P_{I/QIN}$ = 600 mVp-p max.

TYPICAL PERFORMANCE CURVES (T_A = 25°C, V_{CC} = V_{PS} = 3 V, I/Q DC Offset = $\overline{I}/\overline{Q}$ DC Offset = 1.5 V, I/Q Input Signal = 500 mVp-p (Single-ended), P_{LOIN} = -10 dBm unless otherwise specified)

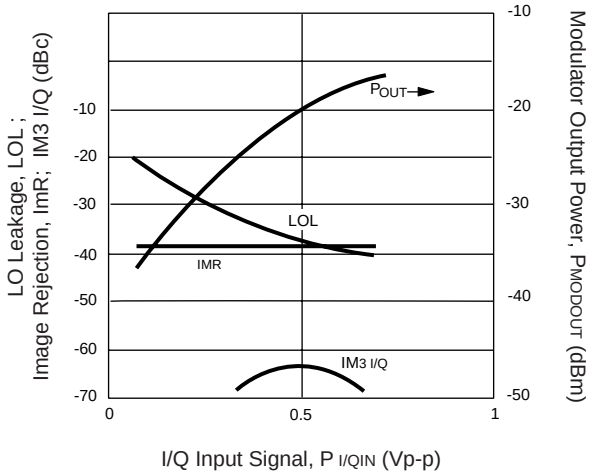
MODULATOR
OUTPUT POWER, LO LEAKAGE , IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs.LO INPUT POWER



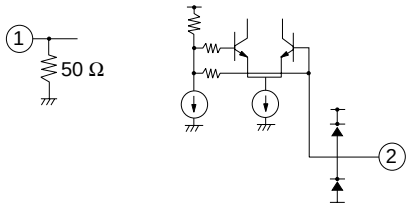
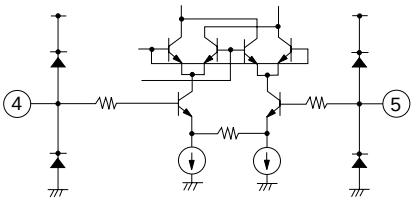
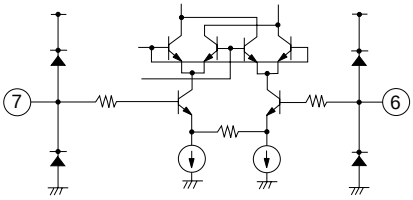
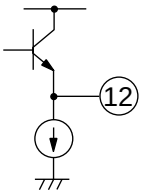
MODULATOR
OUTPUT POWER, LO LEAKAGE , IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. LO INPUT FREQUENCY



MODULATOR
OUTPUT POWER, LO LEAKAGE , IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. I/Q INPUT SIGNAL



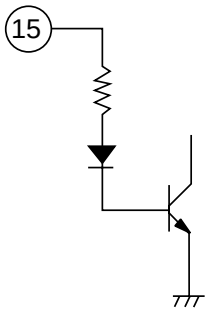
PIN FUNCTIONS

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage</th><th>Pin Voltage</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>1</td><td>LO_{IN}</td><td>—</td><td>0</td><td>LO input for the phase shifter. This input impedance is internally matched to 50 Ω.</td><td rowspan="2"> 
</td></tr>
<tr><td>2</td><td>$\overline{LO_{IN}}$ (Bypass)</td><td>—</td><td></td><td>Bypass of the LO input.This pin is grounded through an internal capacitor. For a single-ended design this pin should be left open.</td></tr>
<tr><td>3
8</td><td>GND</td><td></td><td></td><td>Connect to ground with minimum inductance. Track length should be kept as short as possible.</td><td></td></tr>
<tr><td>4</td><td>I</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for I signal. This input impedance is larger than 20 kΩ. The relationship between the amplitude and the DC bias of the input signal are as follows: *1
<table>
<tr><th>$V_{CC/2}$ (V)</th><th>Amp. (mVp-p)</th></tr>
<tr><td>≥1.35</td><td>400</td></tr>
<tr><td>≥1.5</td><td>600</td></tr>
<tr><td>≥1.75</td><td>1000</td></tr>
</table></td><td rowspan="2"> 
</td></tr>
<tr><td>5</td><td>$\overline{I}$</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for I signal. This input impedance is larger than 20 kΩ. $V_{CC/2}$ biased DC signal should be input.</td></tr>
<tr><td>6</td><td>$\overline{Q}$</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for Q signal. This input impedance is larger than 20 kΩ. $V_{CC/2}$ biased DC signal should be input.</td><td rowspan="2"> 
</td></tr>
<tr><td>7</td><td>Q</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for Q signal. This input impedance is larger than 20 kΩ. The relationship between the amplitude and the DC bias of the input signal are as follows:
<table>
<tr><th>$V_{CC/2}$ (V)</th><th>Amp. (mVp-p)</th></tr>
<tr><td>≥1.35</td><td>400</td></tr>
<tr><td>≥1.5</td><td>600</td></tr>
<tr><td>≥1.75</td><td>1000</td></tr>
</table></td></tr>
<tr><td>12</td><td>MOD_{OUT}</td><td>—</td><td></td><td>Output from the modulator. This is emitter follower output. Connect approx. 15 Ω in series to match to 50 Ω.</td><td> 
</td></tr>
</table>

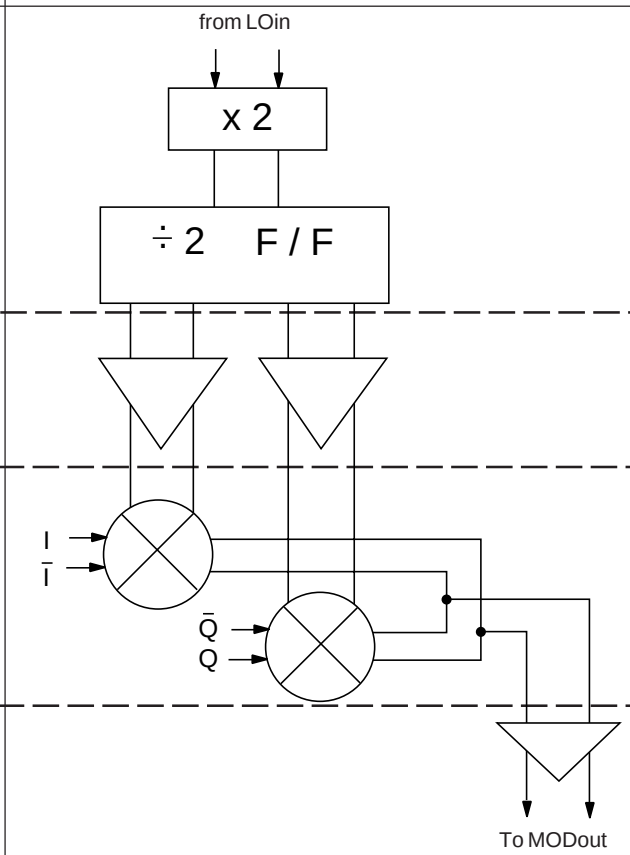
*1: In case I/Q input signals are single ended. I/Q signal inputs can be used either single-ended or differentially with proper terminations.

*2: $V_{CC/2}$ DC bias must be supplied to I, $\overline{I}$, Q, $\overline{Q}$.

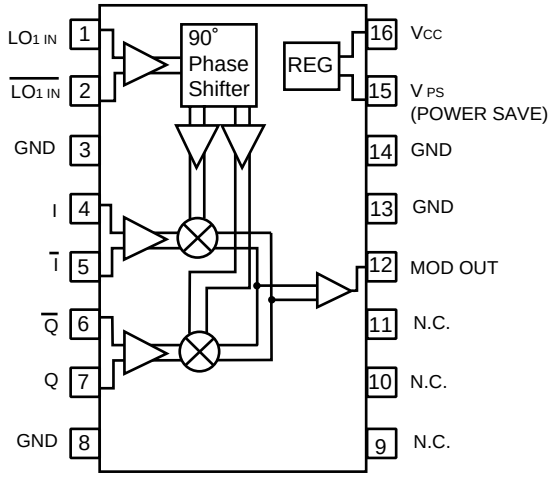
PIN FUNCTIONS

Pin No.	Symbol	Supply Voltage	Pin Voltage	Description	Equivalent Circuit
13 14	GND	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
15	V_{PS} (Power Save)	V_{PS}		Power save control pin can control the On/Sleep state with bias as follows: V_{PS} (V) / STATE 1.8~5.5 / ON 0~1.0 / SLEEP	
16	V_{CC}	2.7~5.5	—	Supply voltage pin for the modulator. An internal regulator helps keep the device stable against temperature or V_{CC} variation.	

MODULATOR INTERNAL FUNCTIONS

Block	Function/Operation	Block Diagram
90° Phase Shifter	Input signal from LO is sent to a T-type flip-flop through a frequency doubler. The output signal from the T-type F/F is changed to the same frequency as LO input with a quadrature phase shift of 0°, 90°, 180°, or 270°. These circuits provide self phase correction for proper quadrature signals.	
Buffer Amplifier	Buffer amplifiers for each phase signal are sent to each mixer.	
Mixer	Each signal from the buffer amps is quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to provide excellent image rejection.	
Adder	Output signal from each mixer is added and sent through a final amplifier stage to pin 16 for further off-chip filtering if necessary.	

INTERNAL BLOCK DIAGRAM



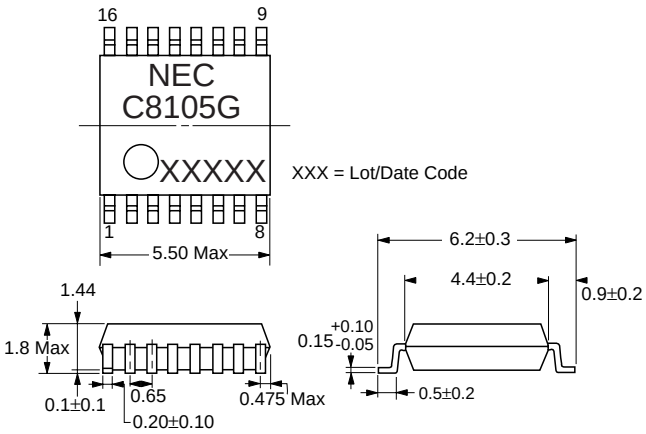
ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC8105GR-E1	2500/Reel

Note: Embossed Tape, 12 mm wide.

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE SSOP 16



LEAD CONNECTIONS

1. $\overline{LO_{IN}}$	9. N.C.
2. LO_{IN}	10. N.C.
3. GND	11. N.C.
4. I Input	12. MOD_{OUT}
5. $\overline{I}$ Input	13. GND
6. $\overline{Q}$ Input	14. GND
7. Q Input	15. V_{PS} (Power Save)
8. GND	16. V_{CC}

All dimensions are typical unless specified otherwise.

APPLICATION CIRCUIT