

N-CHANNEL POWER MOS FET ARRAY FOR SWITCHING

μ PA1550 is a N-channel vertical power MOS FET and this switching device is available for direct drive by output of 5 V power supply IC.

This device features low on-resistance and excellent switching characteristic, and is ideal for control of devices such as mortars, solenoid, or ramp.

FEATURES

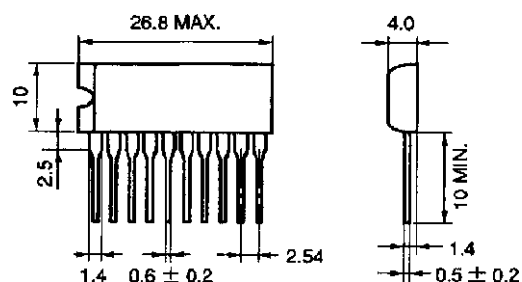
- Gate drive available at logic level ($V_{GS} = 4$ V)
- High current capacity and low on-resistance
 $I_{D(pulse)} = \pm 20$ A
 $R_{DS(on)} = 0.09 \Omega$ TYP. @ $V_{GS} = 10$ V
 $R_{DS(on)} = 0.11 \Omega$ TYP. @ $V_{GS} = 4$ V
- Easy to mount the printing board due to 2.54 mm (0.1 inch) interval of lead pins
- Small dimension and no electrode exposure except lead pins enable the high density mounting.

ORDERING INFORMATION

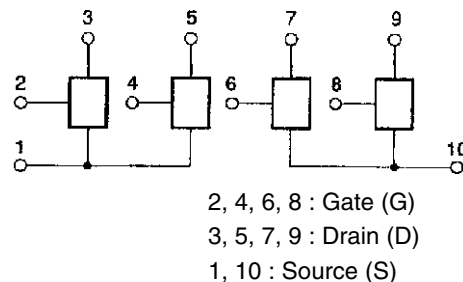
Part Number	Package	Quality
μ PA1550H	10-pin SIP	Standard

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

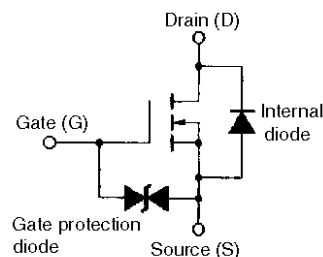
PACKAGE DRAWING (UNIT: mm)



ELECTRODE CONNECTION



INTERNAL EQUIVALENT CIRCUIT



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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

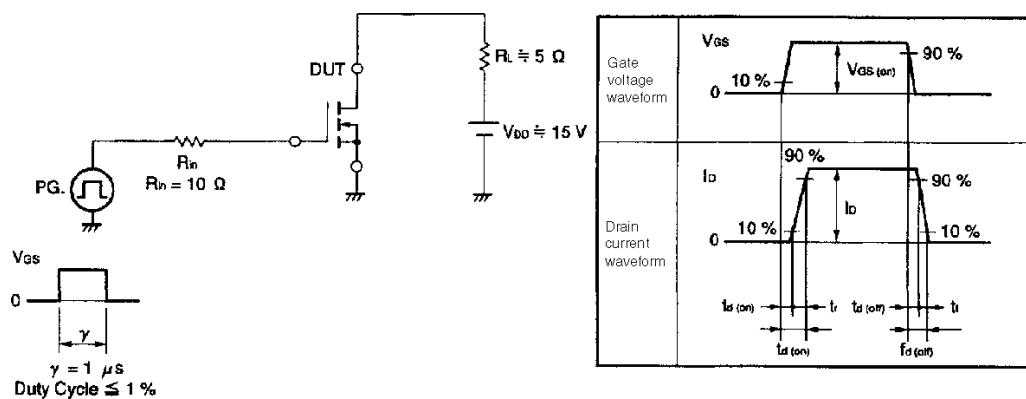
Parameter	Symbol	Conditions	Ratings	Unit
Drain to source voltage	V _{DSS}	V _{GS} = 0	30	V
Gate to source voltage	V _{GSS}	V _{DS} = 0	±20	V
Drain current (DC)	I _{D(DC)}	T _C = 25°C	±5	A/unit
Drain current (pulse)	I _{D(pulse)}	PW ≤ 10 μs duty cycle ≤ 1 %	±20	A/unit
Total power dissipation	P _{T1} *	T _C = 25°C	3.5	W
Total power dissipation	P _{T2} *	T _a = 25°C	28	W
Channel temperature	T _{ch}		150	°C
Storage temperature	T _{stg}		-55 to +150	°C

* When all 4 elements are ON.

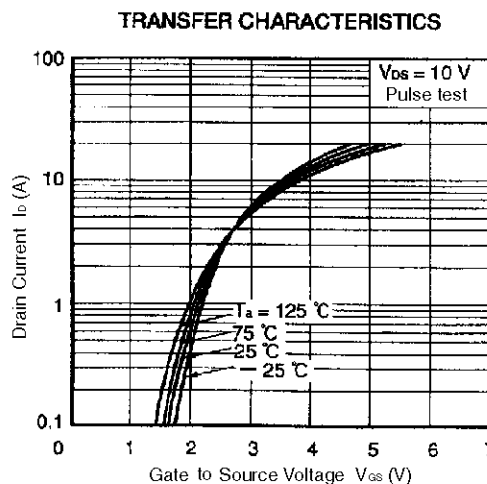
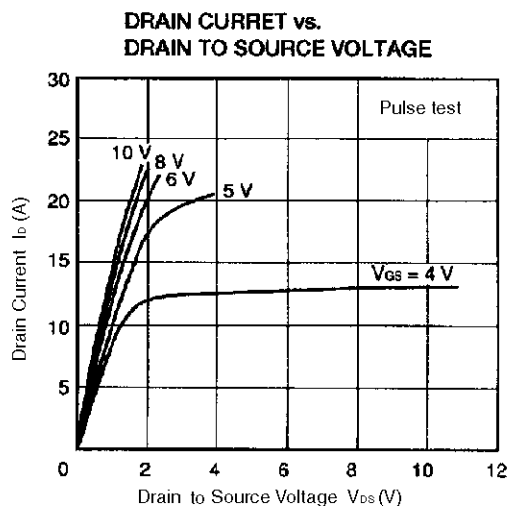
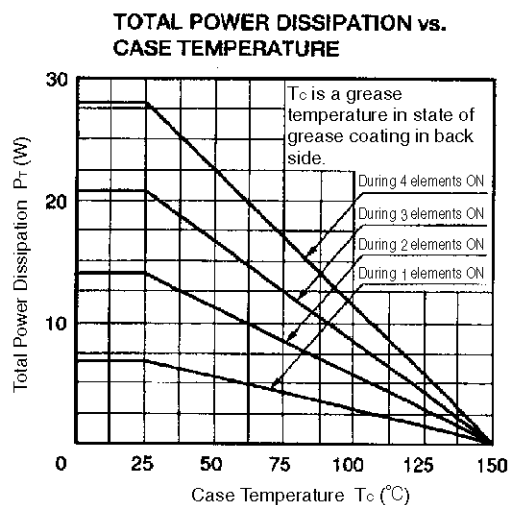
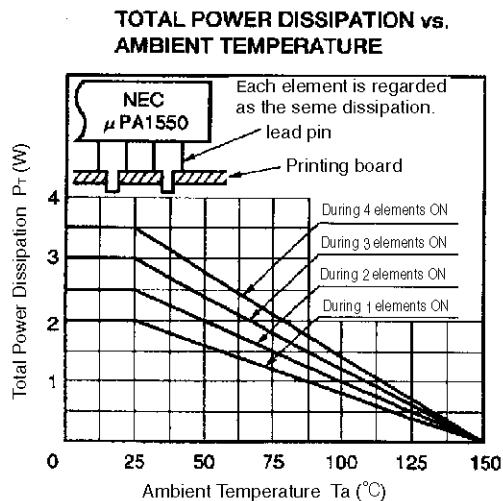
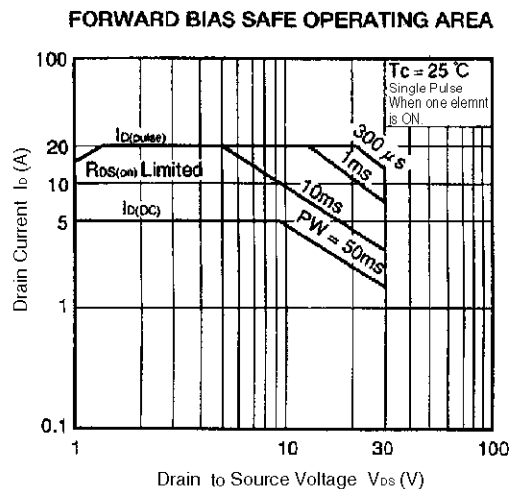
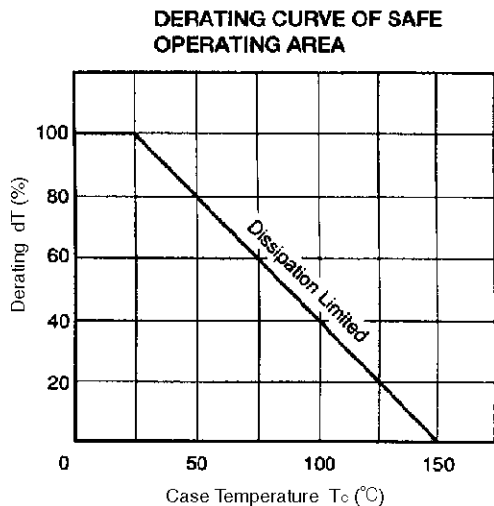
ELECTRICAL CHARACTERISTICS (VCC = 5V, Ta = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain cutoff current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate leakage current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate cutoff voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	0.8		2.5	V
Forward transfer admittance	y _{ts}	V _{DS} = 10 V, I _D = 3 A	4.0	5.0		S
Drain to source on-state resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 3 A		90	100	mΩ
Drain to source on-state resistance	R _{DS(on)2}	V _{GS} = 4 V, I _D = 3 A		110	150	mΩ
Input capacitance	C _{iss}	V _{DS} = 10 V		900		pF
Output capacitance	C _{oss}	V _{GS} = 0 V		400		pF
Return capacitance	C _{rss}	f = 1 MHz		100		pF
Turn-on delay time	t _{d(on)}	I _D = 3 A V _{GS(on)} = 10 V		10		ns
Rise time	t _r	V _{DD} = 5 Ω		40		ns
Turn-off delay time	t _{d(off)}	R _L = 5 Ω, R _{in} = 10 Ω		110		ns
Fall time	t _f	Refer to the test circuit.		30		ns

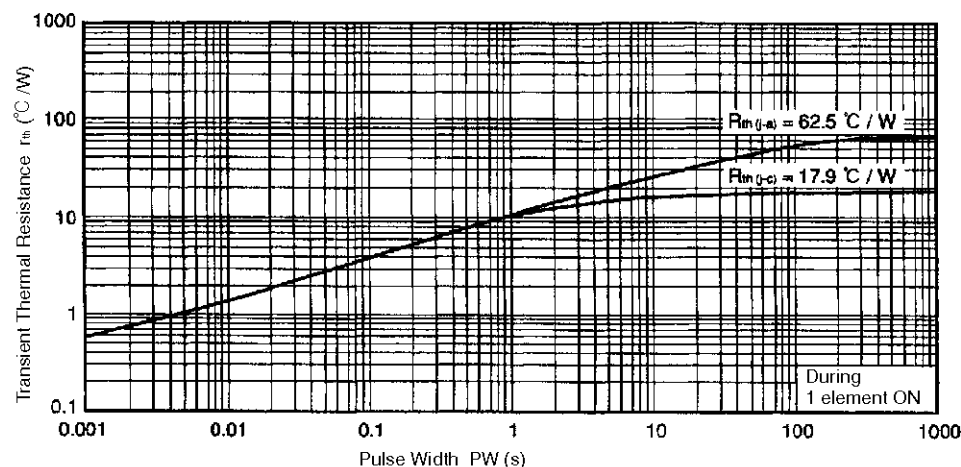
TEST CIRCUIT DIAGRAM: SWITCHING TIME



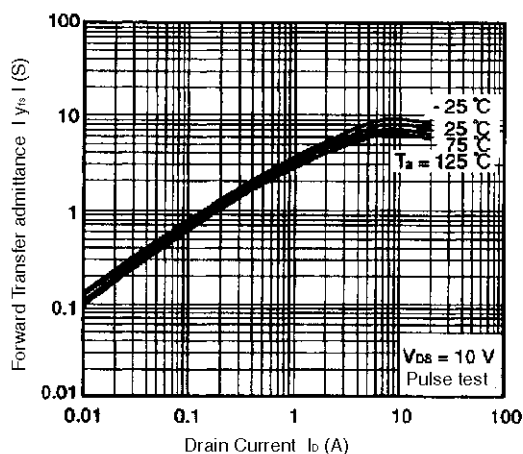
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



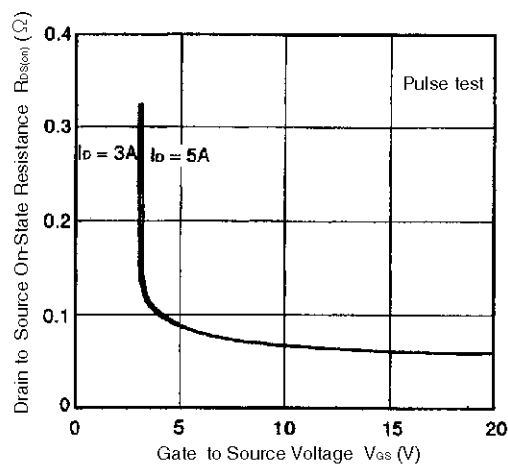
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



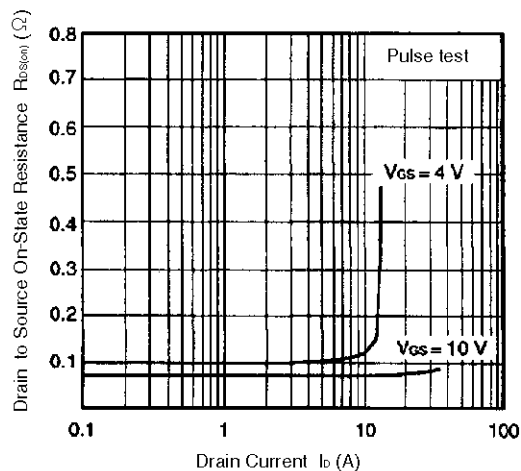
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



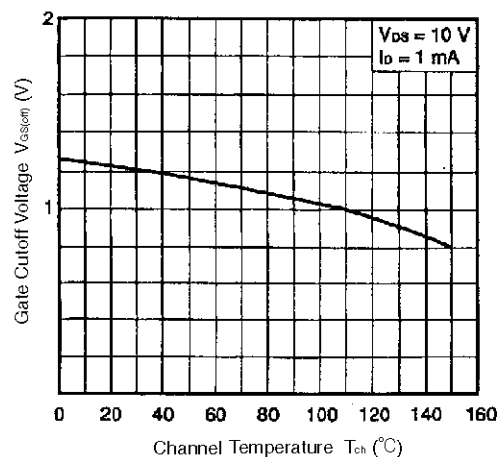
DRAIN TO SOURCE ON STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



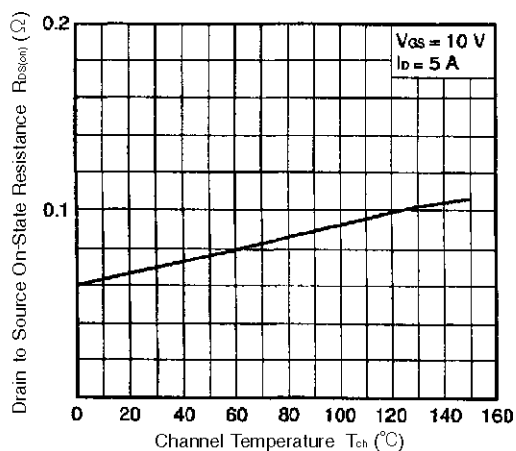
DRAIN TO SOURCE ON STATE RESISTANCE vs. DRAIN CURRENT



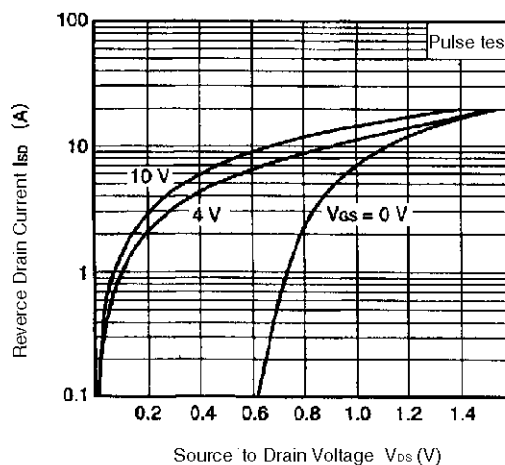
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



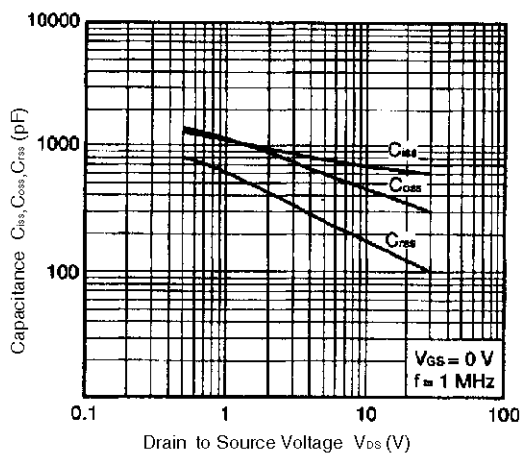
**DRAIN TO SOURCE ON - STATE RESISTANCE
vs. CHANNEL TEMPERATURE**



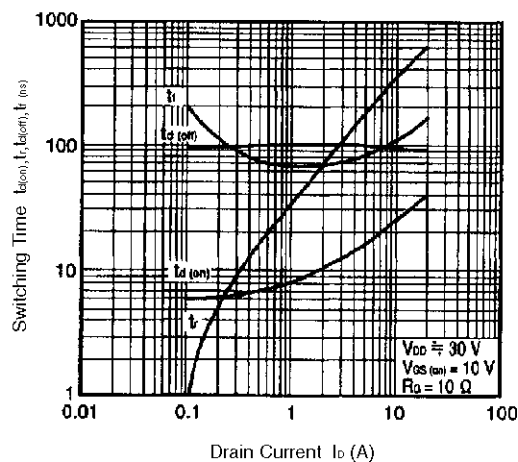
BODY DIODE FORWARD VOLTAGE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS



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