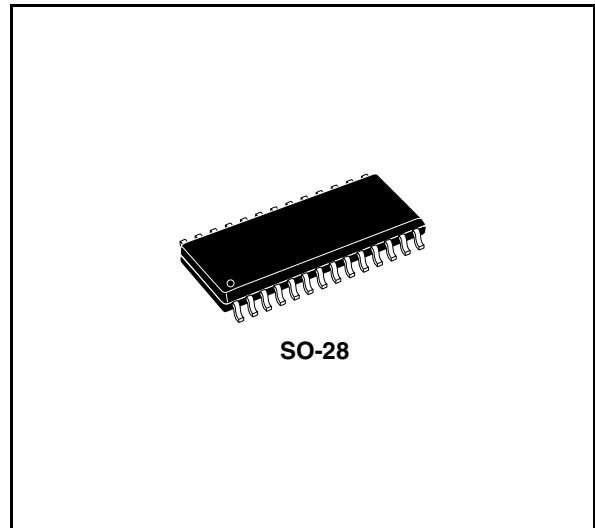


Digitally controlled audio processor

Features

- Input multiplexer
 - Three stereo and one mono inputs
 - Selectable input gain for optimal adaptation to different sources
- Volume control in 0.3db steps including gain up to 20dB
- Zero crossing mute and direct mute
- Pause detector with programmable threshold
- Soft mute controlled by software or hardware PIN
- Bass and treble control
- Four speaker attenuators
 - Four independent speakers control in 1.25dB steps for balance and fader facilities
 - Independent mute function
- All functions programmable via serial I²C bus



instead of standard bipolar multipliers, very low distortion and very low noise are obtained. Several new features like softmute, zero-crossing mute and pause detector are implemented.

The Soft Mute function can be activated in two ways, either via the serial bus (bit D0, Mute Byte), or directly on pin 22 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

Description

The TDA7348 is an upgrade of the TDA7318 audioprocessor.

Thanks to the used BIPOLAR/CMOS technology, very low distortion, low noise and DC-stepping are obtained. Due to a highly linear signal processing, using CMOS-switching techniques

Order codes

Part number	Package	Packing
TDA7348D	SO-28	Tube
TDA7348D013TR	SO-28	Tape and reel
E-TDA7348D ⁽¹⁾	SO-28	Tube
E-TDA7348D013TR ⁽¹⁾	SO-28	Tape and reel

1. This device is Pb-free Ecopack , see [Chapter 5](#) Package information.

Contents

1	Block diagram and PIN connections	5
2	Electrical characteristics	6
3	I²C BUS interface	10
3.1	Data validity	10
3.2	Start and stop conditions	10
3.3	Byte format	10
3.4	Acknowledge	10
3.5	Transmission without acknowledgement	10
4	Software specification	12
4.1	Interface protocol	12
4.2	Auto increment	12
4.3	Transmitted data	13
4.4	Data byte specification	13
5	Package information	18
6	Revision history	19

List of tables

Table 1.	Electrical characteristics	6
Table 2.	Absolute maximum ratings	8
Table 3.	Thermal data	8
Table 4.	Quick reference data	8
Table 5.	Subaddress (receive mode)	12
Table 6.	Send mode	13
Table 7.	Input Selector	13
Table 8.	Loudness	13
Table 9.	Mute	14
Table 10.	Speaker attenuators	15
Table 11.	Bass/Treble	15
Table 12.	Volume	17
Table 13.	Document revision history	19

List of figures

Figure 1. Block diagram 5

Figure 2. PIN connections 5

Figure 3. Data validity on the I²C BUS. 11

Figure 4. Timing diagram of I²C BUS 11

Figure 5. Acknowledge on the I²C BUS. 11

Figure 6. SO-28 mechanical, data and package dimensions 18



1 Block diagram and PIN connections

Figure 1. Block diagram

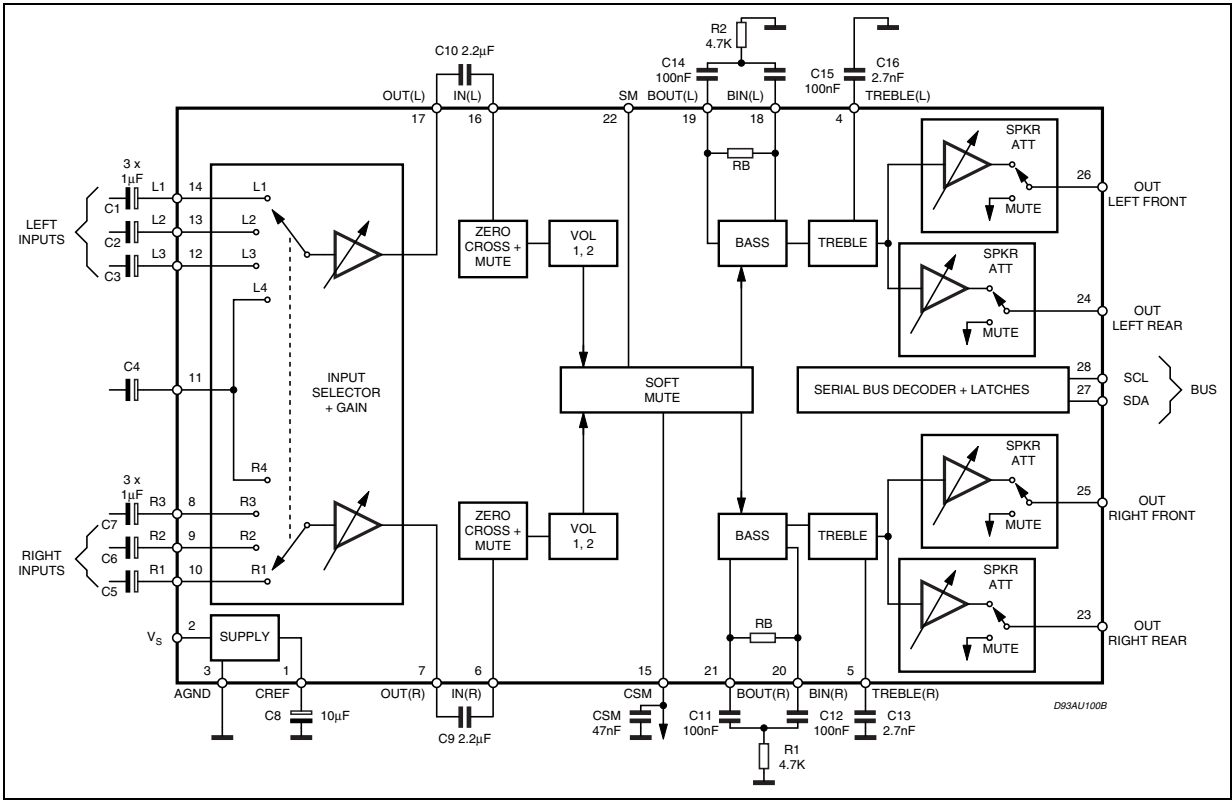
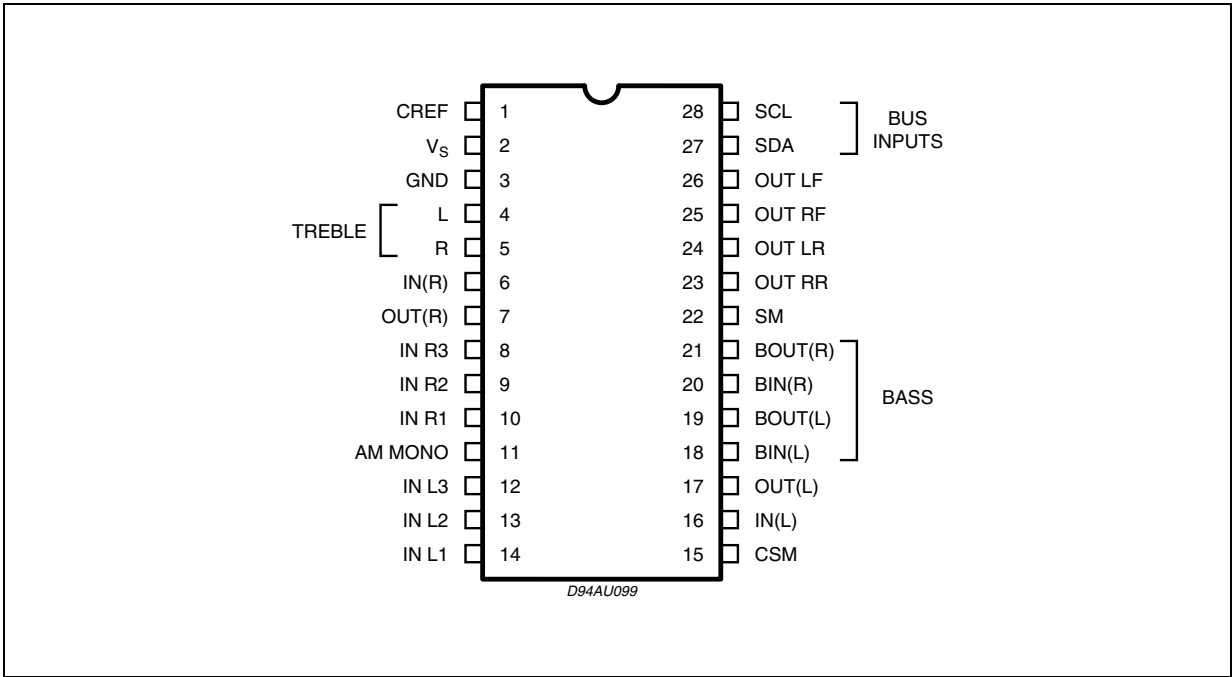


Figure 2. PIN connections



2 Electrical characteristics

Table 1. Electrical characteristics

$V_S = 9V$; $R_L = 10K\Omega$; $R_g = 50\Omega$; $T_{amb} = 25^\circ C$; all controls flat ($G = 0.3dB$ step $0dB$); $f = 1KHz$. Refer to the test circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input selector						
R _I	Input resistance		70	100	130	KΩ
V _{CL}	Clipping level	d ≤ 0.3%	2.1	2.6		V _{RMS}
S _I	Input separation		80	100		dB
R _L	Output load resistance		2			KΩ
G _{I MIN}	Minimum input gain		-0.75	0	0.75	dB
G _{I MAX}	Maximum input gain		10.25	11.25	12.25	dB
G _{step}	Step resolution		2.75	3.75	4.75	dB
e _N	Input noise	20Hz to 20 KHz unweighted		2.3		μV
V _{DC}	DC steps	Adiacent gain steps		1.5	10	mV
		G _{IMIN} to G _{IMAX}		3		mV
Volume control (1 + 2)						
R _I	Input resistance		35	50		KΩ
G _{MAX}	Maximum gain		18.75	20	21.25	dB
A _{MAX}	Maximum attenuation			78.45		dB
A _{STEPC}	Step resolution coarse attenuation		0.5	1.25	2.0	dB
A _{STEPF}	Step resolution fine attenuation		0.11	0.31	0.51	dB
E _A	Attenuation set error	G = 20 to -20dB	-1.25	0	1.25	dB
		G = -20 to -58dB	-3		2	dB
E _t	Tracking error				2	dB
V _{DC}	DC steps	Adiacent attenuation steps	-3	0	3	mV
		From 0dB to A _{MAX}		0.5	5	mV
Zero crossing mute						
V _{TH}	Zero crossing threshold	WIN = 11		20		mV
		WIN = 10		40		mV
		WIN = 01		80		mV
		WIN = 00		160		mV
A _{MUTE}	Mute attenuation		80	100		dB
V _{DC}	DC step	0dB to Mute		0	3	mV

Table 1. Electrical characteristics (continued)

$V_S = 9V$; $R_L = 10K\Omega$; $R_g = 50\Omega$; $T_{amb} = 25^\circ C$; all controls flat ($G = 0.3dB$ step $0dB$); $f = 1KHz$. Refer to the test circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Soft mute						
A_{MUTE}	Mute attenuation		45	60		dB
T_{DON}	ON delay time	$C_{CSM} = 22nF$; 0 to $-20dB$; $I = I_{MAX}$	0.7	1	1.7	ms
		$C_{CSM} = 22nF$; 0 to $-20dB$; $I = I_{MIN}$	20	35	55	ms
T_{DOFF}	OFF delay time	$V_{CSM} = 0V$; $I = I_{MAX}$	25	50	75	μA
		$V_{CSM} = 0V$; $I = I_{MIN}$		1		μA
V_{THSM}	Soft mute threshold		1.5	2.5	3.5	V
R_{INT}	Pull-up resistor (pin 22)		35	50	65	$K\Omega$
V_{SMH}	(pin 22) level high	Soft Mute active	3.5			V
V_{SML}	(pin 22) level low				1	V
Bass control						
B_{BOOST}	Max bass boost		15	18	20	dB
B_{CUT}	Max bass cut		-8.5	-10	-11.5	dB
A_{step}	Step resolution		1	2	3	dB
R_g	Internal feedback resistance		45	65	85	$K\Omega$
Treble control						
C_{RANGE}	Control range		± 13	± 14	± 15	dB
A_{step}	Step resolution		1	2	3	dB
Speaker attenuators						
C_{RANGE}	Control range		35	37.5	40	dB
A_{step}	Step resolution		0.5	1.25	2.0	dB
A_{MUTE}	Output mute attenuation	Data word = XXX11111	80	100		dB
E_A	Attenuation set error				1.25	dB
V_{DC}	DC steps	Adjacent attenuation steps		0	3	mV
Audio output						
V_{clip}	Clipping level	$d = 0.3\%$	2.1	2.6		V _{rms}
R_L	Output load resistance		2			$K\Omega$
R_O	Output impedance			30	100	W
V_{DC}	DC voltage level		3.5	3.8	4.1	V
General						
V_{CC}	Supply voltage		6	9	10.2	V

Table 1. Electrical characteristics (continued)

$V_S = 9V$; $R_L = 10K\Omega$; $R_g = 50\Omega$; $T_{amb} = 25^\circ C$; all controls flat ($G = 0.3dB$ step $0dB$); $f = 1KHz$. Refer to the test circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC}	Supply current		5	10	15	mA
PSRR	Power supply rejection ratio	$f = 1KHz$	60	80		dB
		$B = 20$ to $20kHz$ "A" weighted		65		dB
e_{NO}	Output noise	Output Muted ($B = 20$ to $20kHz$ flat)		2.5		μV
		All Gains $0dB$ ($B = 20$ to $20kHz$ flat)		5	15	μV
E_t	Total tracking error	$A_V = 0$ to $-20dB$		0	1	dB
		$A_V = -20$ to $-60dB$		0	2	dB
S/N	Signal to noise ratio	All Gains = $0dB$; $V_O = 1V_{rms}$		106		dB
S_C	Channel separation		80	100		dB
d	Distortion	$V_{in} = 1V$		0.01	0.08	%
Bus inputs						
V_{IL}	Input low voltage				1	V
V_{IN}	Input high voltage		3			V
I_{IN}	Input current	$V_{IN} = 0.4V$	-5		5	μA
V_O	Output voltage SDA acknowledge	$I_O = 1.6mA$		0.4	0.8	V

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature	-40 to 85	$^\circ C$
T_{stg}	Storage temperature range	-55 to 150	$^\circ C$

Table 3. Thermal data

Symbol	Parameter	SO28	Unit
$R_{th j-amb}$	Thermal Resistance Junction pins	65	$^\circ C/W$

Table 4. Quick reference data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply voltage	6	9	10.2	V
V_{CL}	Max. input signal handling	2.1	2.6		V_{rms}
THD	Total harmonic distortion $V = 1V_{rms}$ $f = 1KHz$		0.01	0.08	%
S/N	Signal to noise ratio		106		dB

Table 4. Quick reference data (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Sc	Channel separation f = 1KHz		100		dB
	Volume control	-78.45		20	dB
	Treble control 2dB step	-14		+14	dB
	Bass control 2dB step	-10		+18	dB
	Fader and balance control 1.25dB step	-38.75		0	dB
	Input gain 3.75dB step	0		11.25	dB
	Mute attenuation		100		dB

3 I²C BUS interface

Data transmission from microprocessor to the TDA7348 and vice-versa takes place through the 2 wires of the I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to the positive supply voltage must be externally connected).

3.1 Data validity

As shown in [Figure 3.](#), the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and stop conditions

As shown in [Figure 4.](#) a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

A STOP conditions must be sent before each START condition.

3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

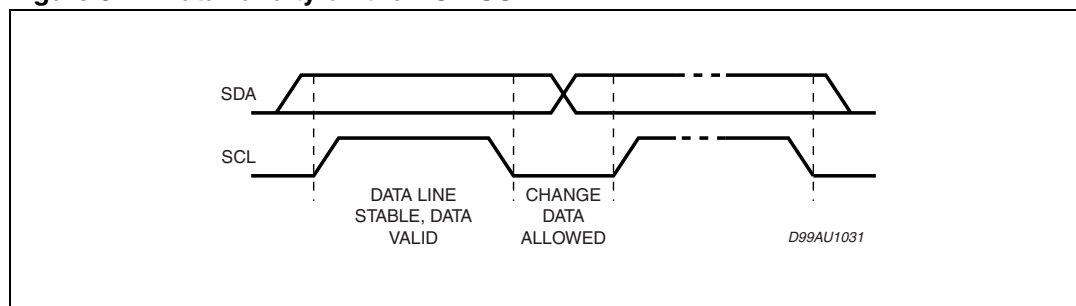
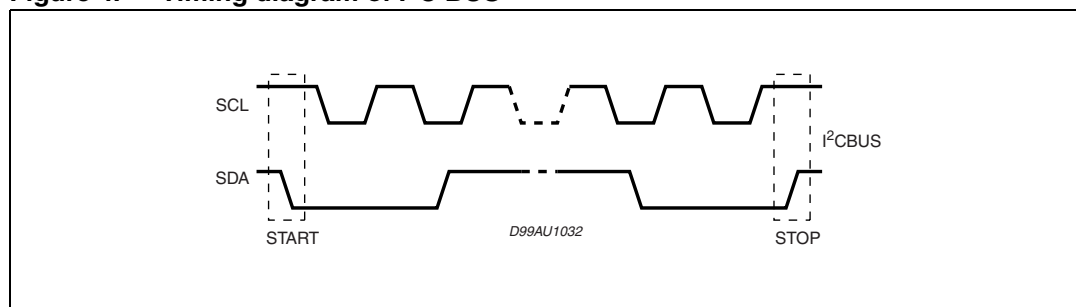
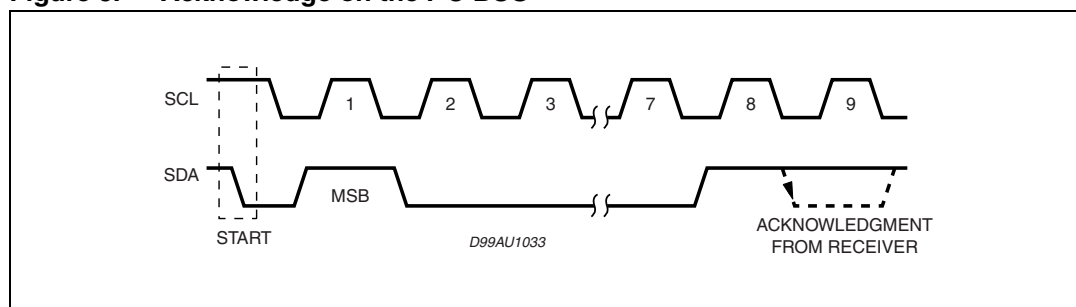
The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see [Figure 5.](#)). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without acknowledgement

The microprocessor can use a simpler transmission, if it avoids detection of the acknowledgement from the audio processor. It simply waits one clock pulse without checking the slave acknowledgment, and sends the new data.

This approach of course is less protected from errors, increases the possibility of interference, and decreases the immunity to noise.

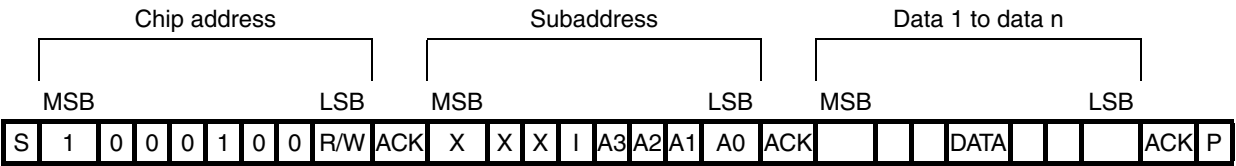
Figure 3. Data validity on the I²C BUS**Figure 4. Timing diagram of I²C BUS****Figure 5. Acknowledge on the I²C BUS**

4 Software specification

4.1 Interface protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, (the LSB bit determines read/write transmission)
- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

I = Auto Increment

X = Not used

Max clock speed 500kbits/s

4.2 Auto increment

If bit I in the subaddress byte is set to "1", the auto-increment of the subaddress is enabled

Table 5. Subaddress (receive mode)

MSB								LSB	Function
X	X	X	I	A3	A2	A1	A0		
				0	0	0	0		Input selector
				0	0	0	1		Loudness
				0	0	1	0		Volume
				0	0	1	1		Bass, Treble
				0	1	0	0		Speaker attenuator LF
				0	1	0	1		Speaker attenuator LR
				0	1	1	0		Speaker attenuator RF
				0	1	1	1		Speaker attenuator RR
				1	0	0	0		Mute

4.3 Transmitted data

Table 6. Send mode

MSB						LSB	
X	X	X	X	X	SM	ZM	X

ZM = Zero crossing muted (HIGH active)

SM = Soft mute activated (HIGH active)

X = Not used

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

4.4 Data byte specification

X = not relevant; set to "1" during testing

Table 7. Input Selector

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	1			0	0	0	not used
X	X	1			0	0	1	IN 2
X	X	1			0	1	0	IN 1
X	X	1			0	1	1	AM mono
X	X	1			1	0	0	not used
X	X	1			1	0	1	IN 3
X	X	1			1	1	0	not allowed
X	X	1			1	1	1	not allowed
X	X	1	0	0				11.25dB gain
X	X	1	0	1				7.5dB gain
X	X	1	1	0				3.75dB gain
X	X	1	1	1				0dB gain

For example to select the IN 2 input with a gain of 7.5dB the Data Byte is: X X 1 0 1 0 0 1

Table 8. Loudness

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	1	0	0	0	0	0dB
X	X	X	1	0	0	0	1	-1.25dB
X	X	X	1	0	0	1	0	-2.5dB

Table 8. Loudness (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	1	0	0	1	1	-3.75dB
X	X	X	1	0	1	0	0	-5dB
X	X	X	1	0	1	0	1	-6.25dB
X	X	X	1	0	1	1	0	-7.5dB
X	X	X	1	0	1	1	1	-8.75dB
X	X	X	1	1	0	0	0	-10dB
X	X	X	1	1	0	0	1	-11.25dB
X	X	X	1	1	0	1	0	-12.5dB
X	X	X	1	1	0	1	1	-13.75dB
X	X	X	1	1	1	0	0	-15dB
X	X	X	1	1	1	0	1	-16.25dB
X	X	X	1	1	1	1	0	-17.5dB
X	X	X	1	1	1	1	1	-18.75dB

For example to select -17.5dB attenuation, loudness OFF, the Data Byte is: X X X1 1 1 1 0

Table 9. Mute

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							1	Soft mute on
						0	1	Soft mute with fast slope (I = IMAX)
						1	1	Soft mute with slow slope (I = IMIN)
				1				Direct mute
			0		1			Zero crossing mute on
			0		0			Zero crossing mute off (delayed until next zerocrossing)
			1					Zero crossing mute and pause detector reset
	0	0						160mV ZC window threshold (WIN = 00)
	0	1						80mV ZC window threshold (WIN = 01)
	1	0						40mV ZC window threshold (WIN = 10)
	1	1						20mV ZC window threshold (WIN = 11)
0								Non-symmetrical Bass Cut
1								Symmetrical Bass Cut

An additional direct mute function is included in the speaker attenuators.

Note: Bass cut for very low frequencies should not be used at +16 & +18dB bass boost (DC gain)

Table 10. Speaker attenuators

MSB							LSB	Speaker attenuator LF, LR, RF, RR
D7	D6	D5	D4	D3	D2	D1	D0	
								1.25dB step
X	X	X			0	0	0	0dB
X	X	X			0	0	1	-1.25dB
X	X	X			0	1	0	-2.5dB
X	X	X			0	1	1	-3.75dB
X	X	X			1	0	0	-5dB
X	X	X			1	0	1	-6.25dB
X	X	X			1	1	0	-7.5dB
X	X	X			1	1	1	-8.75dB
								10dB step
X	X	X	0	0				0dB
X	X	X	0	1				-10dB
X	X	X	1	0				-20dB
X	X	X	1	1				-30dB
X	X	X	1	1	1	1	1	Speaker mute

For example an attenuation of 25dB on a selected output is given by: X X X1 0 1 0 0

Table 11. Bass/Treble

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble step
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB

Table 11. Bass/Treble (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB
								BASS STEPS
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					-0dB
1	1	1	1					-0dB
1	1	1	0					2dB
1	1	0	1					4dB
1	1	0	0					6dB
1	0	1	1					8dB
1	0	1	0					10dB
1	0	0	1					12dB
1	0	0	0					14dB
0	0	0	1					146B
0	0	0	0					18dB

For example 12dB Treble and -8dB Bass give the following DATA BYTE: 0 0 1 1 1 0 0 1

Table 12. Volume

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								0.31dB Fine attenuation steps
						0	0	0dB
						0	1	-0.31dB
						1	0	-0.62dB
						1	1	-0.94dB
								1.25dB Coarse attenuation steps
			0	0	0			0dB
			0	0	1			-1.25dB
			0	1	0			-2.5dB
			0	1	1			-3.75dB
			1	0	0			-5dB
			1	0	1			-6.25dB
			1	1	0			-7.5dB
			1	1	1			-8.75dB
								10dB Gain / attenuation steps
0	0	0						20dB
0	0	1						10dB
0	1	0						0dB
0	1	1						-10dB
1	0	0						-20dB
1	0	1						-30dB
1	1	0						-40dB
1	1	1						-50dB

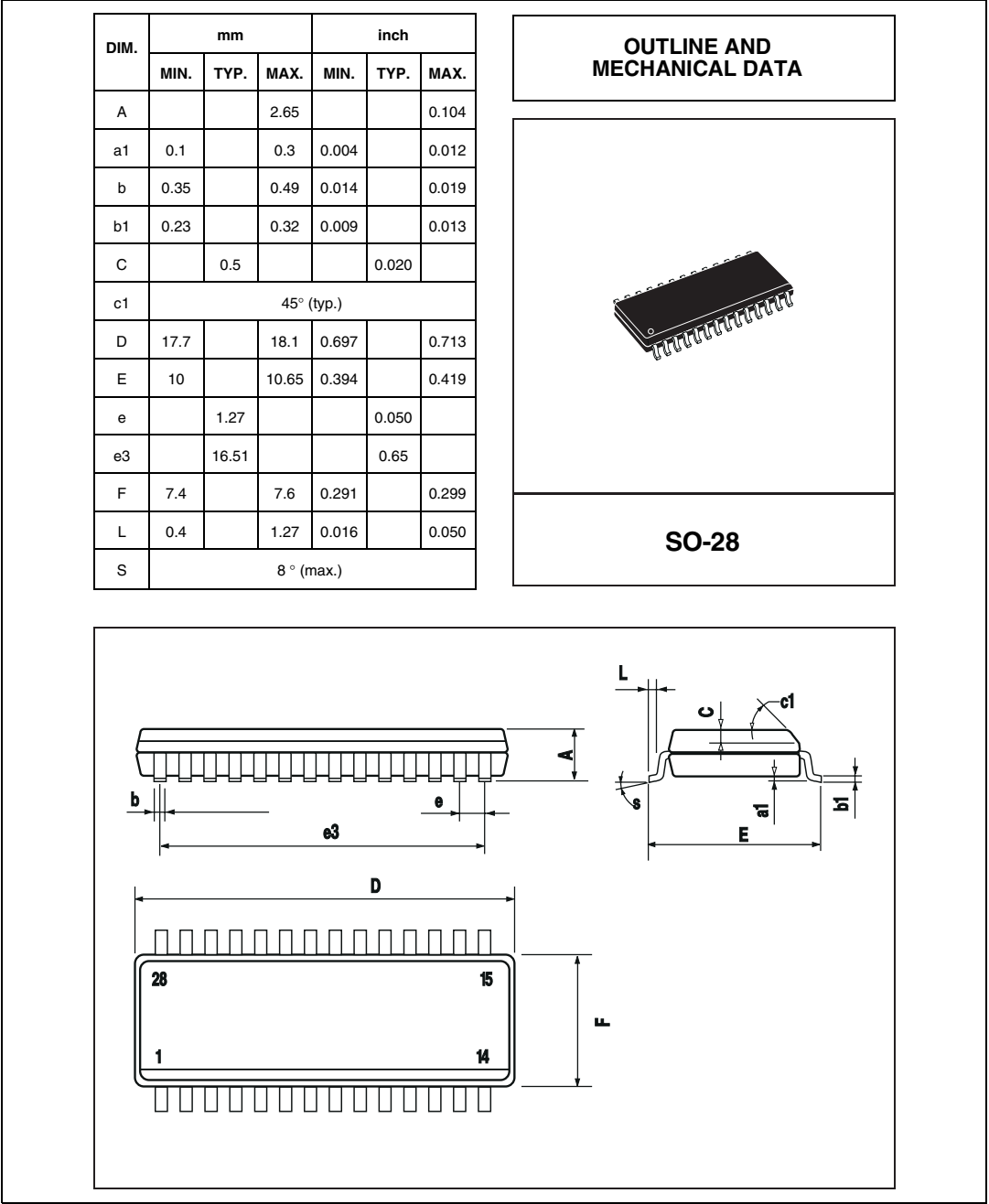
For example to select -47.81dB volume the data byte is: 1 1 0 1 1 0 0 1

Power on RESET: All bytes set to 1 1 1 1 1 1 1 0

5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. SO-28 mechanical, data and package dimensions



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
14-Jan-2004	1	Initial release.
21-Jun-2004	2	Technical migration from ST-PRESS to EDOCS DMS
26-Jan-2007	3	DIP28 package removed, block diagram changed, layout modified.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com