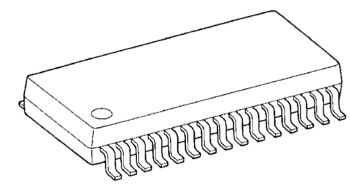
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TD62650FG,TD62651FG,TD62652FG

## 5V POWER SUPPLY & SUPPLY MONITORING + COMMUNICATIONS IC



SSOP30-P-375-1.00

Weight: 0.63 g (typ.)

The TD62650FG series covers products developed for use in microcomputer systems applicable to automatic vending machines. They produce an output voltage of 5 V ± 0.5 V without need for adjustment, through their accurate reference voltage and amplifier circuit.
The 5V section can reset the system by outputting reset signals at power−on, and also output a reset signal when the 5 V output voltage drops below the specified 92% (TD62650FG / 652FG) or 85% (TD62651FG) because of external disturbances or other problem.
It also incorporates a watchdog timer for self−diagnosing the system. When the system malfunctions, the IC generates reset pulses intermittently to prevent the system from running away.
The interface section incorporates three serial ports corresponding to the typical 24−V 4800 bps system in microcomputers.
The suffix (G) appended to the part number represents a Lead (Pb)-Free product.

## FEATURES

- Accurate output : 5V ± 0.25 V
- Output PNP Tr incorporated : Current capacity ; 300 mA (max)
- Power−on Reset timer incorporated
- Watchdog timer incorporated
- Small flat package sealing : SSOP30 pin (1 mm pitch)

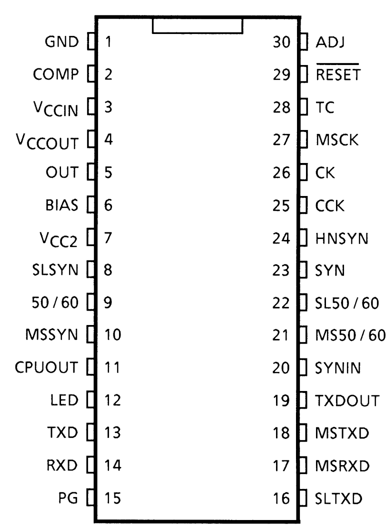
- Difference 1

| CHARACTERISTIC | TD62650 / 652FG | TD62651FG |
|---|---|---|
| Reset Detecting Voltage | 5V / 92% | 5V / 85% |

- Difference 2
  Time setting resistance 22 kΩ for power−on reset / watchdog timer, and PULL resistance of 4.7 kΩ for $\overline{\text{RESET}}$ pin.

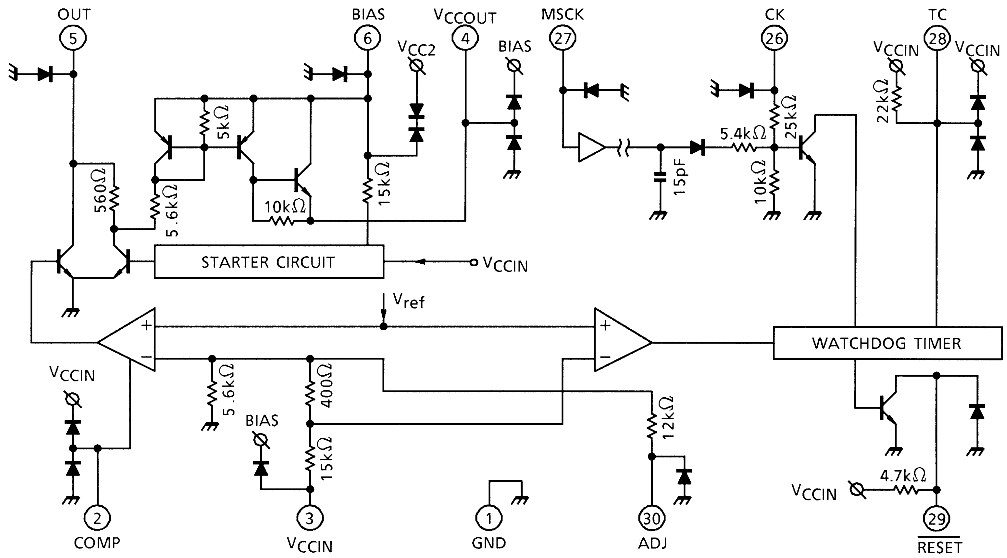
| TD62650FG | TD62651FG | TD62652FG |
|---|---|---|
| Built−in | None | None |

## PIN CONNECTION

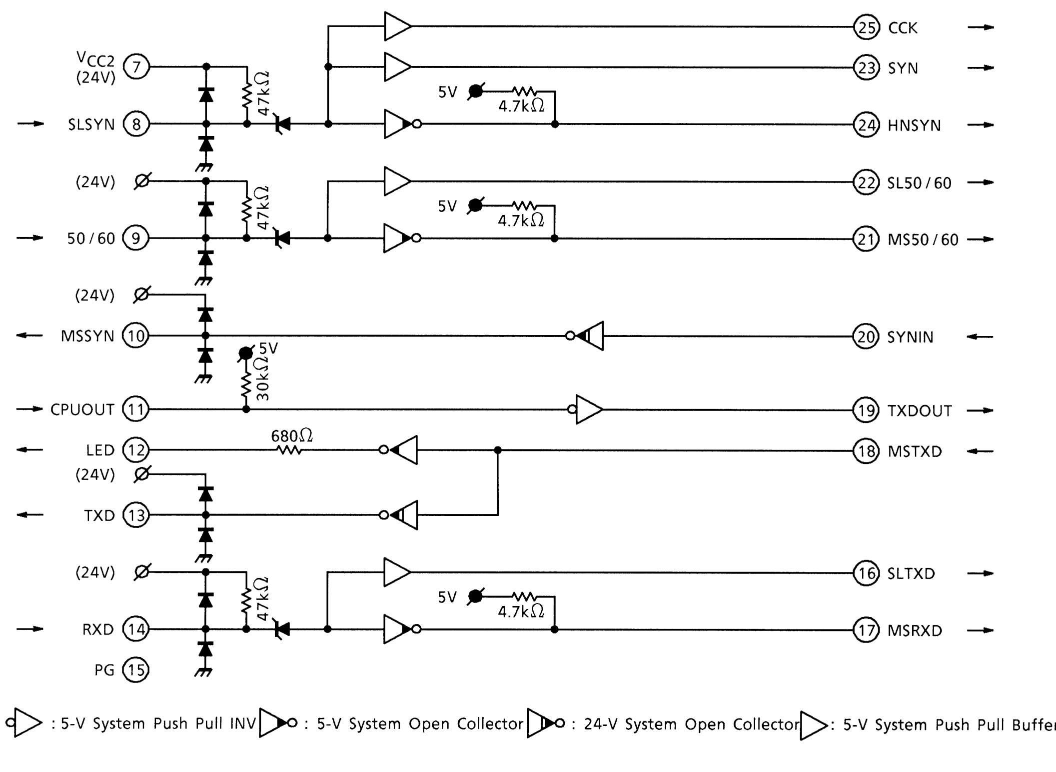


## TD62650FG BLOCK DIAGRAM

### 5V POWER SUPPLY + SUPPLY MONITORING

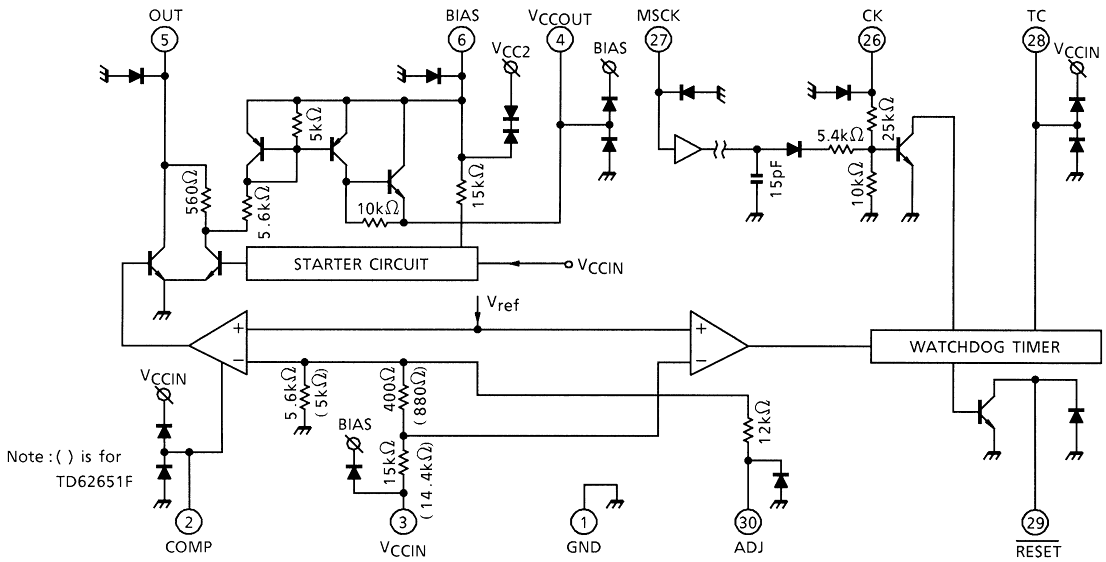



### INTERFACE

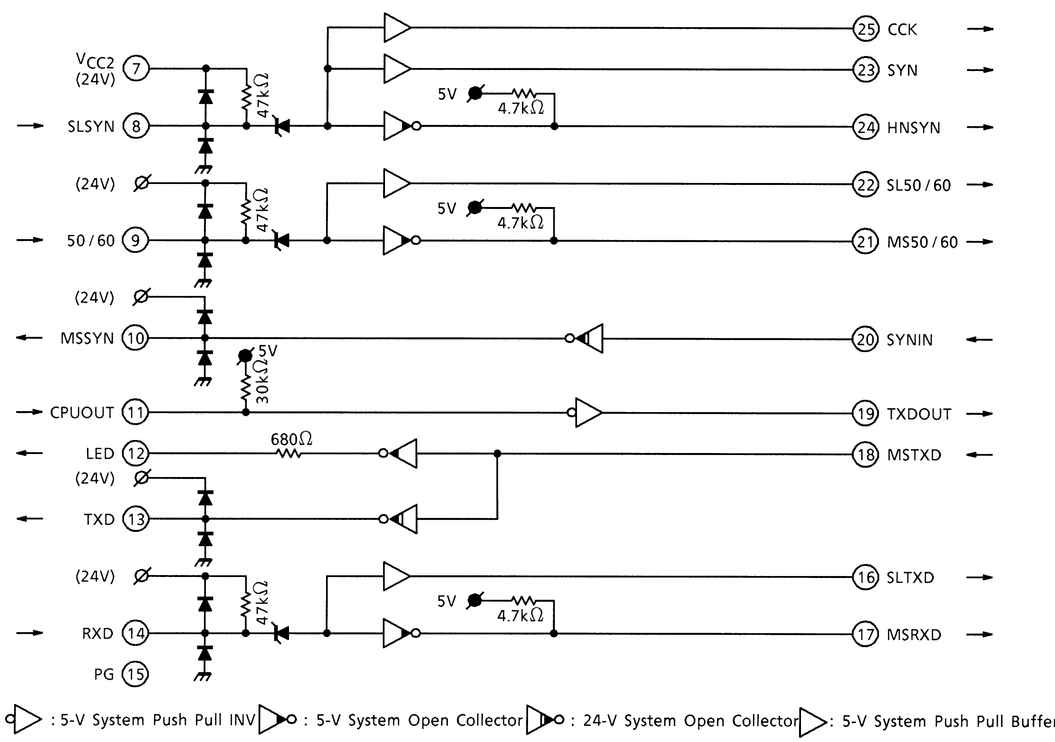


## TD62651FG / TD62652FG BLOCK DIAGRAM

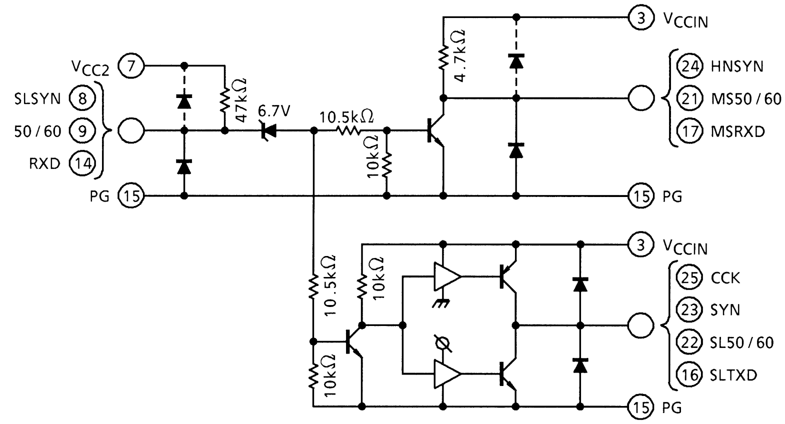
### 5V POWER SUPPLY + SUPPLY MONITORING

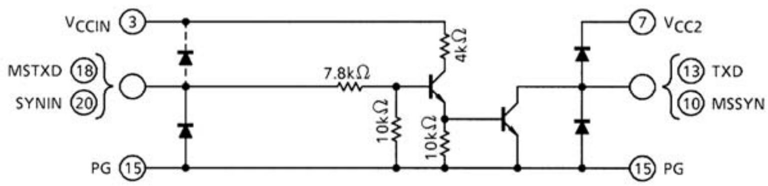


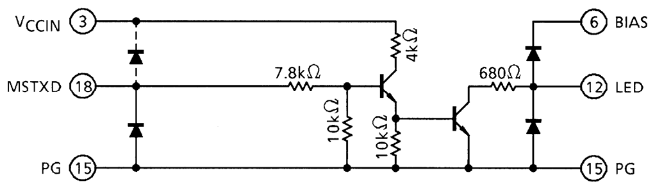

### INTERFACE

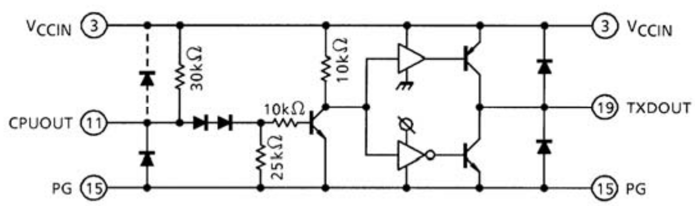


## INTERFACE INPUT / OUTPUT CIRCUITS



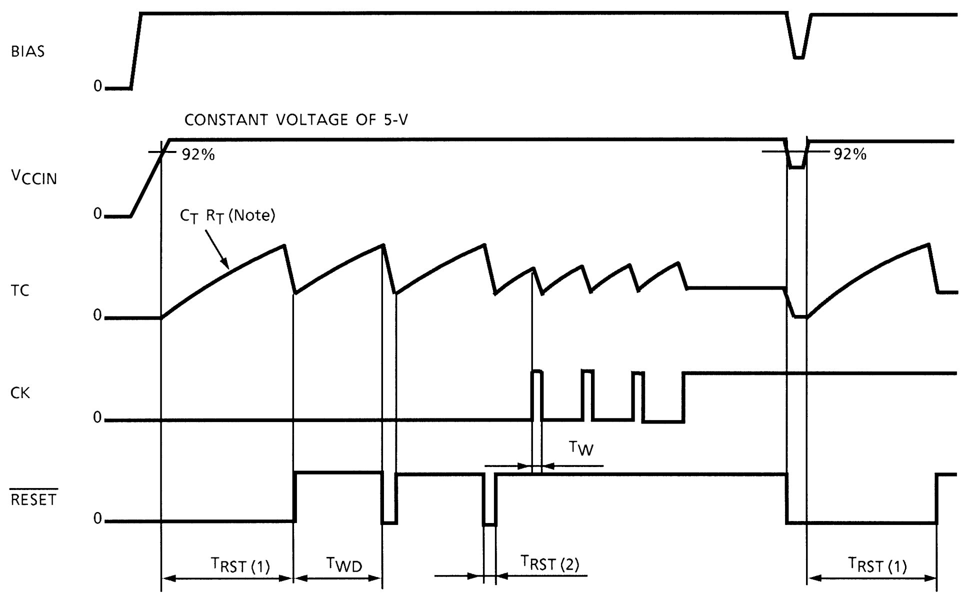



## PIN FUNCTION

| PIN No. | PIN NAME | PIN FUNCTION |
|---|---|---|
| 1 | GND | GND pin for 5 V power supply and supply monitoring. |
| 2 | COMP | Phase compensation pin for output stabilization. |
| 3 | $V_{CCIN}$ | Power supply pin for internal circuit. The output voltage can also be detected at this pin. |
| 4 | $V_{CCOUT}$ | Output pin for built−in Power Tr, having a current capacitance of 300 mA (max). It is also used as an output pin for 5 V constant power supply through shorting with $V_{CCIN}$ pin. |
| 5 | OUT | Connected to the base of an external PNP transistor so that the output voltage is stabilized. Current design suitable for load capacities is thus possible.<br>Since the recommended $I_{OUT}$ current is 5 mA, an output current of 300 mA is assured if the external transistor has an hFE of 60.<br>When the internal transistor is used, it can be opened. |
| 6 | BIAS | Power supply starting pin. The starting current is supplied through a resistor to which the input voltage is applied.<br>When $V_{CCIN}$ rises above 3.0 V, the starting current is absorbed in the internal circuit ; instead, $I_{OUT}$ is supplied via $V_{CCIN}$. |
| 7 | $V_{CC2}$ | Power supply pin for the 24−V system. |
| 8 | SLSYN | Input pin for the 24−V system interface. Pull−up resistor 47 kΩ is incorporated at $V_{CC2}$ pin. |
| 9 | 50 / 60 | Input pin for 24−V system interface. Pull−up resistor 47 kΩ is incorporated at $V_{CC2}$ pin. |
| 10 | MSSYN | Output pin for the 24−V system open collector. |
| 11 | CPUOUT | Input pin for the 5−V system Push / Pull inverter. Pull−up resistor 30 kΩ is incorporated at $V_{CCIN}$ pin. |
| 12 | LED | LED lighting pin for the 8 system open collector. 680 Ω limiting resistor is incorporated. |
| 13 | TXD | Output pin for the 24−V system open collector. |
| 14 | RXD | Input pin for the 24−V system interface. Pull−up resistor 47 kΩ is incorporated at the $V_{CC2}$ pin. |
| 15 | PG | GND pin for the 5−V / 24−V system interfaces. |
| 16 | SLTXD | Output pin for the 5−V system open collector. Pull−up resistor 4.7 kΩ is incorporated at the $V_{CCIN}$ pin. |
| 17 | MSRXD | Output pin for the 5−V system Push−Pull buffer. |
| 18 | MSTXD | Input pin for the 5−V system interface, for input at LED (12 pin) and TXD (13 pin) pins. |
| 19 | TXDOUT | Output pin for the 5−V system Push / Pull inverter (CPUOUT : 11 pin). |
| 20 | SYNIN | Input pin for the 5−V system interface. |
| 21 | MS50 / 60 | Output pin for the 5−V system open collector. Pull−up resistor 4.7 kΩ is incorporated at $V_{CCIN}$ pin. |
| 22 | SL50 / 60 | Output pin for the 5−V system Push / Pull buffer. |
| 23 | SYN | Output pin for the 5−V system Push−Pull buffer. |
| 24 | HNSYN | Output pin for the 5−V system open collector. Pull−up resistor 4.7 kΩ incorporated at $V_{CCIN}$ pin. |
| 25 | CCK | Output pin for the 5−V system Push−Pull buffer. |

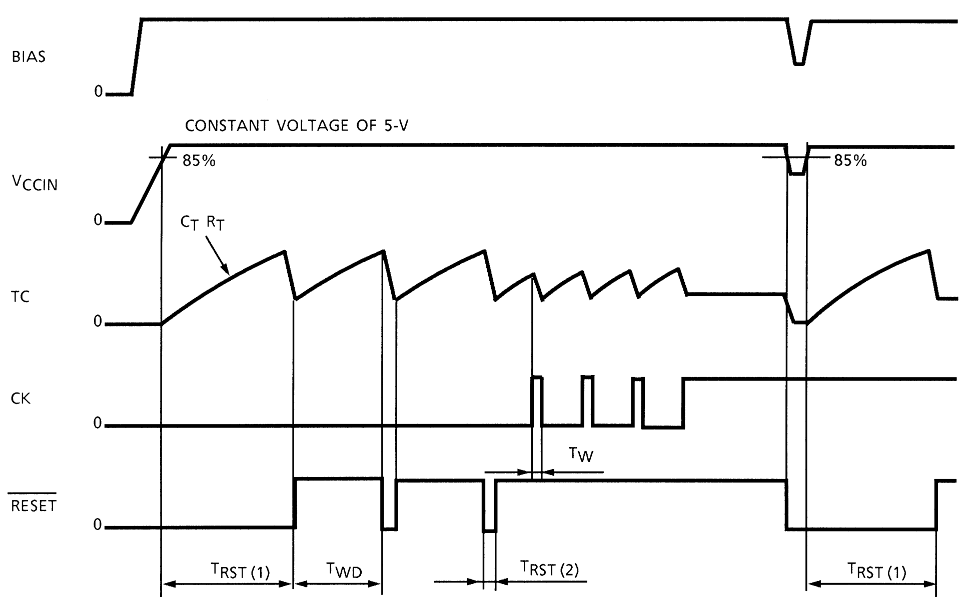
| PIN No. | PIN NAME | PIN FUNCTION |
|---|---|---|
| 26 | CK | Input pin for watchdog timer. The pin is pulled up to $V_{CCIN}$ if the IC is used only as a power−on reset timer. |
| 27 | MSCK | To input clock pulses, one−shot pulses can be generated for CK (26 pin) inputs at the rise edge. When the pin is not used, short it with GND. |
| 28 | TC | Time setting pin for the reset and watchdog timers. |
| 29 | $\overline{\text{RESET}}$ | NPN transistor open−collector output.<br>(1) The signal goes low when the output voltage drops below the specified 92% (TD62650 / 652) or 85% (651) level.<br>(2) The pin generates a reset signal that is determined by the external condenser connected to the TC pin.<br>(3) The pin generates reset pulses intermittently if no clock is attached to the CK pin.<br>This function can be used as a watchdog timer for microcomputers. |
| 30 | ADJ | Output voltage adjusting pin. The voltage will increase when a resistor is connected between ADJ and GND (1 pin). It can reduce the voltage when the resistor is inserted between ADJ and $V_{CCIN}$ (3 pin). The voltage can be changed by a maximum of ± 1V. |

## TIMING CHART (TD62650FG, TD62652FG)




Note: TD6250FG incorporates RT (22kΩ (Typ.) only for $C_T$.)

## TIMING CHART (TD62651FG)



## ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT | PIN |
|---|---|---|---|---|
| Input Voltage | $VV_{CC24}$ | −0.4~35 | V | $V_{CC2}$, BIAS |
| | $VV_{CCIN}$ | −0.4~7 | V | $V_{CCIN}$ |
| | $V_{IN24}$ (Condition 1) (Condition 2) | −0.4~$VV_{CC2}$ + 0.4−0.4~30 | V | SLSYN, 50 / 60, RXD |
| | $V_{IN5}$ | −0.4~$VV_{CCIN}$ + 0.4 | V | CPUOUT, MSCK, ADJ, COMP, CK, TC, SYNIN, MSTXD |
| Output Voltage | $V_{OUT24}$ | −0.4~$VV_{CC2}$ + 0.4 | V | MSSYN, TXD |
| | $VV_{CCOUT}$ | −0.4~$V_{BIAS}$ + 0.4 | V | $V_{CCOUT}$, OUT |
| | $V_{LED}$ (Condition 3) (Condition 4) | −0.4~$V_{BIAS}$ + 0.4−0.4~10 | V | LED |
| | $V_{OUT5}$ | −0.4~$VV_{CCIN}$ + 0.4 | V | $\overline{\text{RESET}}$, CCK, HNSYN, SYN, SL50 / 60, MS50 / 60, TXDOUT, MSRXD, SLTXD |
| Output Current | $I_{OUT}$ | 10 | mA | OUT |
| | $I_{RESET}$ | 4 | mA | $\overline{\text{RESET}}$ |
| | $I_{OUT}$ Push / Pull | ±4 | mA / ch | CCK, SYN, SL50 / 60, TXDOUT, SLTXD |
| | $I_{OUT5}$ | 10 | m / ch | HNSYN, MS50 / 60, LED, MSRXD |
| | $I_{OUT24}$ | 24 | mA / ch | MSSYN, TXD |
| | $IV_{CCOUT}$ | 300 | mA | $V_{CCOUT}$ |
| Power Dissipation | $P_D$ (Note 5) | 1.47 | W | |
| Operating Temperature | $T_{opr}$ | −40~85 | °C | |
| Storage Temperature | $T_{stg}$ | −55~150 | °C | |

Condition 1: $VV_{CC2} \leq 29.6$ V
Condition 2: $VV_{CC2} > 29.6$ V
Condition 3: $V_{BIAS} \leq 9.6$ V
Condition 4: $V_{BIAS} > 9.6$ V
Note 5: Board mounting time (50 × 50 × 1.6 mm, Cu = 30%)

## DC ELECTRICAL CHARACTERISTICS (Ta = 25°C, $V_{CCIN}$ = 5 V)

### Interface Section

| CHARACTERISTIC | SYMBOL | PIN | TEST CIR- CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | $V_{IH5}$ | (Note 1) | — | | $V_{CCIN}$ × 70% | — | — | V |
| | $V_{IL5}$ | | | | — | — | $V_{CCIN}$ × 30% | |
| | $V_{IH24}$ | (Note 1) | | | 13 | — | $V_{CC2}$ + 0.4 | |
| | $V_{IL24}$ | | | | −0.4 | — | 7 | |
| Input Current | $I_{IH5-1}$ | (Note 3) | — | $V_{IN}$ = 5 V | 320 | 462 | 600 | μA / ch |
| | $I_{IL5-1}$ | | | $V_{IN}$ = 0 V | — | 0 | 10 | μA |
| | $I_{IH5-2}$ | (Note 7) | | $V_{IN}$ = 5 V | 480 | 690 | 940 | |
| | $I_{IL5-2}$ | | | $V_{IN}$ = 0 V | 115 | 170 | 240 | |
| | $I_{IH24}$ | (Note 2) | | $V_{IN}$ = 24 V | 1.1 | 1.6 | 2.1 | mA / ch |
| | $I_{IL24}$ | | | $V_{IN}$ = 0 V | 350 | 510 | 690 | μA |
| Output Voltage | $V_{OH5-1}$ | (Note 4) | — | $I_{OH}$ = −20 μA | $V_{CC}$ − 0.1 | — | — | V |
| | $V_{OH5-2}$ | | | $I_{OH}$ = −4 mA | $V_{CCIN}$ × 70% | — | — | |
| | $V_{OL5-1}$ | | | $I_{OL}$ = 20 μA | — | — | 0.1 | |
| | $V_{OL5-2}$ | | | $I_{OL}$ = 4 mA | — | — | $V_{CCIN}$ × 30% | |
| | $V_{OL5-3}$ | (Note 5) | | $I_{IN}$ = 500 μA, $I_{OL}$ = 10 mA | — | — | 0.5 | |
| | $V_{OL}$ LED | LED | | $I_{IN}$ = 200 μA, $I_{OL}$ = 1 mA | — | — | 1.4 | |
| | $V_{OL24}$ | (Note 6) | | $I_{IN}$ = 200 μA, $I_{OL}$ = 24 mA | — | — | 0.5 | |
| Output Impedance | $R_{OL}$ LED | LED | — | (Note 8) | 540 | 680 | 1000 | Ω |
| | $R_{OH5}$ | (Note 5) | | (Note 9) | 3.2 | 4.7 | 6.2 | kΩ |
| Current Consumption 24 | $IV_{CC2}$ | | — | $VV_{CC2}$ = 24 V | — | 1.6 | 2.1 | mA |
| Leakage Current | $I_{LEAK24}$ | (Note 6) | — | $V_{OH}$ = 24.0 V | — | — | 10 | μA |
| | $I_{LEAK5}$ | (Note 4) | | $V_{OH}$ = 5 V | — | — | 10 | |
| Output Shorting Current | $I_{OS}$ (Note) | (Note 4) | — | $V_{CCIN}$ = 5.25 V, $V_{OH}$ = 0 V | — | 17.5 | — | mA |

Note: Two outputs or more must not be shorted at the same time.
Shorting duration must be limited to less than 1 second.

Note 1: CPUOUT, SYNIN, MSTXD
Note 2: SLSYN, 50 / 60, RXD
Note 3: SYNIN, MSTXD
Note 4: CCK, SYN, SL50 / 60, TXDOUT, SLTXD
Note 5: HNSYN, MS50 / 60, MSRXD
Note 6: MSSYN, TXD
Note 7: CPUOUT
Note 8: ($V_{OL}$ (@$I_{OL}$ = 5 mA) − $V_{OL}$ (@$I_{OL}$ = 1 mA)) ÷ 4 mA
Note 9: 4 V ÷ (@$I_{OH}$ ($V_{OH}$ = 0 V) − @$I_{OH}$ (VOH = 4 V))

## DC ELECTRICAL CHARACTERISTICS

**(Unless otherwise specified, $V_{BIAS}$ = 7 to 17 V, Ta = −40 to 85°C)**
**5V power supply, supply monitoring section**

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{CCOUT}$ | — | $IV_{CCOUT}$ = 0.1 A | 4.75 | 5.0 | 5.25 | V |
| Input Stability | $V_{CCOUT}$ LINE | — | $V_{BIAS}$ = 7~35 V | — | 0.1 | 0.5 | % |
| Load Stability | $V_{CCOUT}$ LOAD | — | $IV_{CCOUT}$ = 1~150 mA | — | 0.1 | 0.5 | % |
| Temperature Coefficient | $V_{CCOUT}$ t | — | | — | 0.01 | — | % / °C |
| Output Voltage | $V_{OL}$ $\overline{RESET}$ | — | $I_{OL}$ = 2 mA | — | — | 0.5 | V |
| Output Leakage Current | $I_{LEAK}$ $\overline{RESET}$ | — | $V_{RESET}$ = 7 V | — | — | 5 | μA |
| Input Current | $I_{TC}$ | — | $V_{TC}$ = 0 to 3.5 V (Note 8) | −3 | — | 3 | μA |
| Threshold Voltage | $V_{TC}$ H | — | $\overline{RESET}$ "High" to "Low" | — | 80% × $V_{CCIN}$ | — | V |
| | $V_{TC}$ L | | $\overline{RESET}$ "Low" to "High" | — | 40% × $V_{CCIN}$ | — | |
| Input Current | $I_{CK}$ | — | $V_{IN}$ = 5 V (Note 8) | — | 0.3 | 0.7 | mA |
| Input Voltage | $V_{IH}$ | — | (Note 4) | $V_{CCIN}$ × 70% | — | — | V |
| | $V_{IL}$ | | | — | — | $V_{CCIN}$ × 30% | |
| Reset Detecting Voltage | $V_{CC}$ $\overline{RESET}$ | — | TD62650 / 652FG | 89% × $V_{CCIN}$ | 92% × $V_{CCIN}$ | 95% × $V_{CCIN}$ | V |
| | | | TD62651FG | 82% × $V_{CCIN}$ | 85% × $V_{CCIN}$ | 88% × $V_{CCIN}$ | |
| Output Impedance | $R_{OH}$ $\overline{RESET}$ | — | TD62650FG (Note 1) | 3.2 | 4.7 | 6.2 | kΩ |
| | $R_{OH}$ TC | | TD62650FG (Note 1) | 15 | 22 | 29 | |
| Current Consumption 5 | $IV_{CCIN}$ | — | (Note 2) | — | 5 | 6.5 | mA |
| | | | (Note 5) | — | 11.5 | 15.0 | |
| Bias Current Consumption | $I_{BIAS}$ | — | $V_{BIAS}$ = 8V (Note 7) | — | 1.73 | 2.25 | mA |
| Watchdog Timer | $T_{WD}$ | — | TD62650FG (Note 6) | 15.4 × CT | 24.2 × CT | 33.0 × CT | ms |
| | | | TD62651 /652FG | 0.9 × CTRT | 1.1 × CTRT | 1.3 × CTRT | s |
| Reset Timer (1) (Note 3) | $T_{RST}$ (1) | — | TD62650FG (Note 6) | 24.2 × CT | 35.2 × CT | 48.4 × CT | ms |
| | | | TD62651 / 652FG | 1.3 × CTRT | 1.6 × CTRT | 1.9 × CTRT | s |
| Reset Timer (Note 3) | $T_{RST}$ (2) | — | (Note 6) | 300 × CT | 600 × CT | 900 × CT | ms |

| CHARACTERISTIC | SYMBOL | TEST CIR−CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Clock Input Pulse width | TW CK | — | | 3 | — | — | μs |
| Maximum Response Frequency 1 | $f_{MAX}$ MSCK | — | | 2 | — | — | kHz |
| Maximum Response Frequency 2 | $f_{MAX}$ CK | — | | 10 | — | — | kHz |
| Msck Pin Input Signal Rise Time | tr MSCK | — | (Note 9) | — | — | 500 | ns |
| Minimum Input / Output Voltage Difference | $V_{OH}$ $V_{CCOUT}$ | — | $IV_{CCOUT}$ = 0.1 A | — | — | 1.5 | V |

Note 1: 4 V ÷ (@$I_{OH}$ ($V_{OH}$ = 0 V) − @$I_{OH}$ ($V_{OH}$ = 4 V)
Note 2: $V_{BIAS}$ = 8 V, $V_{CCIN}$ − $V_{CCOUT}$ Short
Open Collector I / O : Open
Push−Pull I / O : Open
MSCK Input : Open
Note 3: Reset Timer (1) : Power On Reset Time
Reset Timer (2) : Watchdog Reset Time
Note 4: MSCK, CK Pins
Note 5: HNSYN, MS50 / 60, MSRXD Pull / UP Resistance + CCK, SYN, SL50 / 60, TXDOUT, SLTXD Driving Current
Note 6: CT Unit (μF)
Note 7: $V_{CCIN}$, $V_{CCOUT}$ Open
Note 8: Only TD62651FG, TD62652FG
Note 9: Input Condition 5 V : 0 to 100%

## AC ELECTRICAL CHARACTERISTICS (Ta = 25°C)

| CHARACTERISTIC | CHARACTERISTIC / INPUT CONDITION | SYMBOL | TEST CIR−CUIT | OUTPUT CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time (tpLH: 50%−50%, tpHL: 50%−50%) | SLSYN−CCK (Note 1) | tpLH | — | (Note 4) | — | 0.6 | — | μs |
| | | tpHL | | | — | 1.5 | — | |
| | SLSYN−SYN (Note 1) | tpLH | | (Note 4) | — | 0.6 | — | |
| | | tpHL | | | — | 1.5 | — | |
| | SLSYN−HNSYN (Note 1) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | 50 / 60−MS50 / 60 (Note 1) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | 50 / 60−SL50 / 60 (Note 1) | tpLH | | (Note 4) | — | 0.6 | — | |
| | | tpHL | | | — | 1.5 | — | |
| | SYNIN−MSSYN (Note 2) | tpLH | | (Note 3) | — | 1.0 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | CPUOUT−TXDOUT (Note 2) | tpLH | | (Note 4) | — | 1.0 | — | |
| | | tpHL | | | — | 1.2 | — | |
| | MSTXD−LED (Note 2) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | MSTXD−TXD (Note 2) | tpLH | | (Note 3) | — | 1.0 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | RXD−SLTXD (Note 1) | tpLH | | (Note 4) | — | 0.6 | — | |
| | | tpHL | | | — | 1.5 | — | |
| | RXD−MSRXD (Note 1) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| Rise Time (tr: 10%−90%) | MS50 / 60 | tr | — | | — | 0.3 | — | μs |
| | SL50 / 60 | | | | — | 0.2 | — | |
| | LED | | | | — | 0.2 | — | |
| | MSSYN | | | | — | 1.1 | — | |
| | TXDOUT | | | | — | 0.2 | — | |
| | TXD | | | | — | 1.1 | — | |
| | SYN | | | | — | 0.2 | — | |
| | CCK | | | | — | 0.2 | — | |
| | HNSYN | | | | — | 0.3 | — | |
| | SLTXD | | | | — | 0.2 | — | |
| | MSRXD | | | | — | 0.3 | — | |

| CHARACTERISTIC | CHARACTERISTIC / INPUT CONDITION | SYMBOL | TEST CIR−CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Fall Time (tr: 90%−10%) | MS50 / 60 | tf | — | | — | 0.1 | — | μs |
| | SL50 / 60 | | | | — | 0.5 | — | |
| | LED | | | | — | 0.1 | — | |
| | MSSYN | | | | — | 0.1 | — | |
| | TXDOUT | | | | — | 0.5 | — | |
| | TXD | | | | — | 0.1 | — | |
| | SYN | | | | — | 0.5 | — | |
| | CCK | | | | — | 0.5 | — | |
| | HNSYN | | | | — | 0.1 | — | |
| | SLTXD | | | | — | 0.5 | — | |
| | MSRXD | | | | — | 0.1 | — | |

Input / Output Conditions

- Input Condition

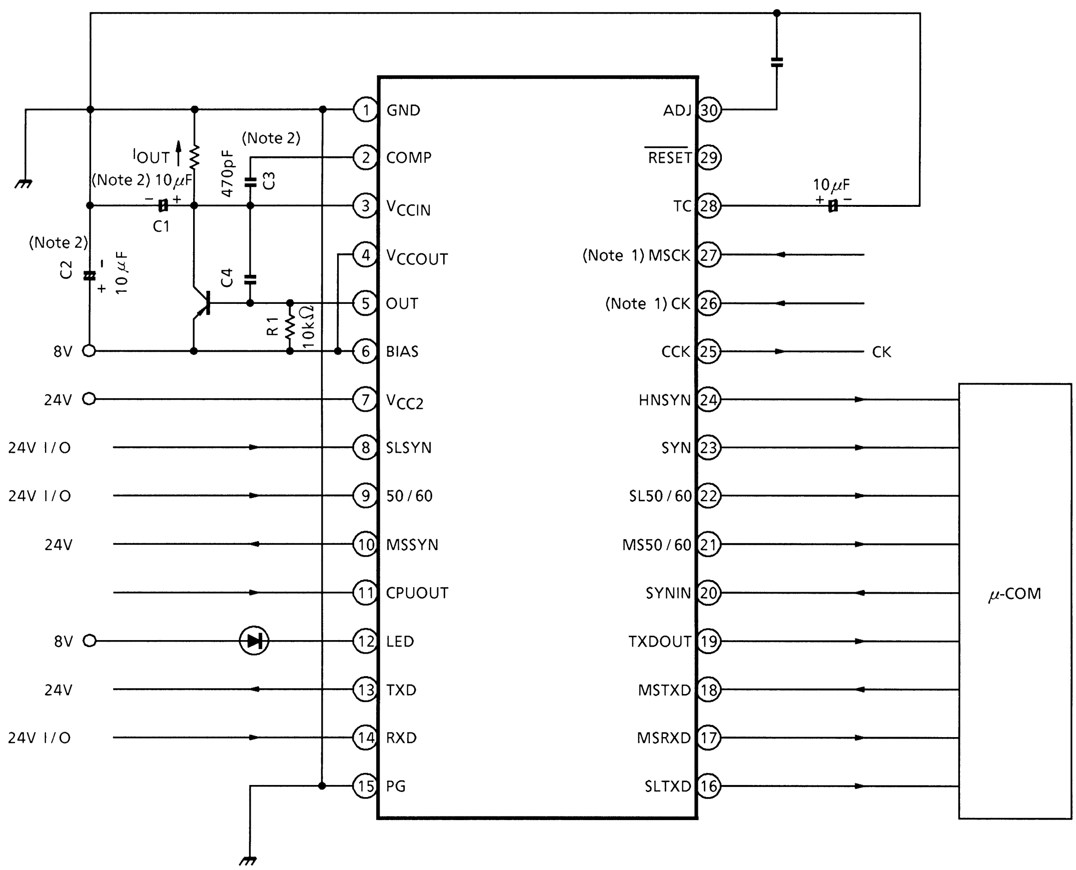
  Note 1: 24−V System : 0.2μs at 2 to 22−V
  Note 2: 5−V System : 0.1μs at 30 to 70%

- Output Conditions

  Note 3: 24−V System : $C_L$ = 50 pF
  Note 4: 5−V System : $C_L$ = 50 pF
  $R_L$ = 5 kΩ
  Note 5: 5−V System : $C_L$ = 50 pF

## APPLICATION CIRCUIT

When using an external PNP transistor :



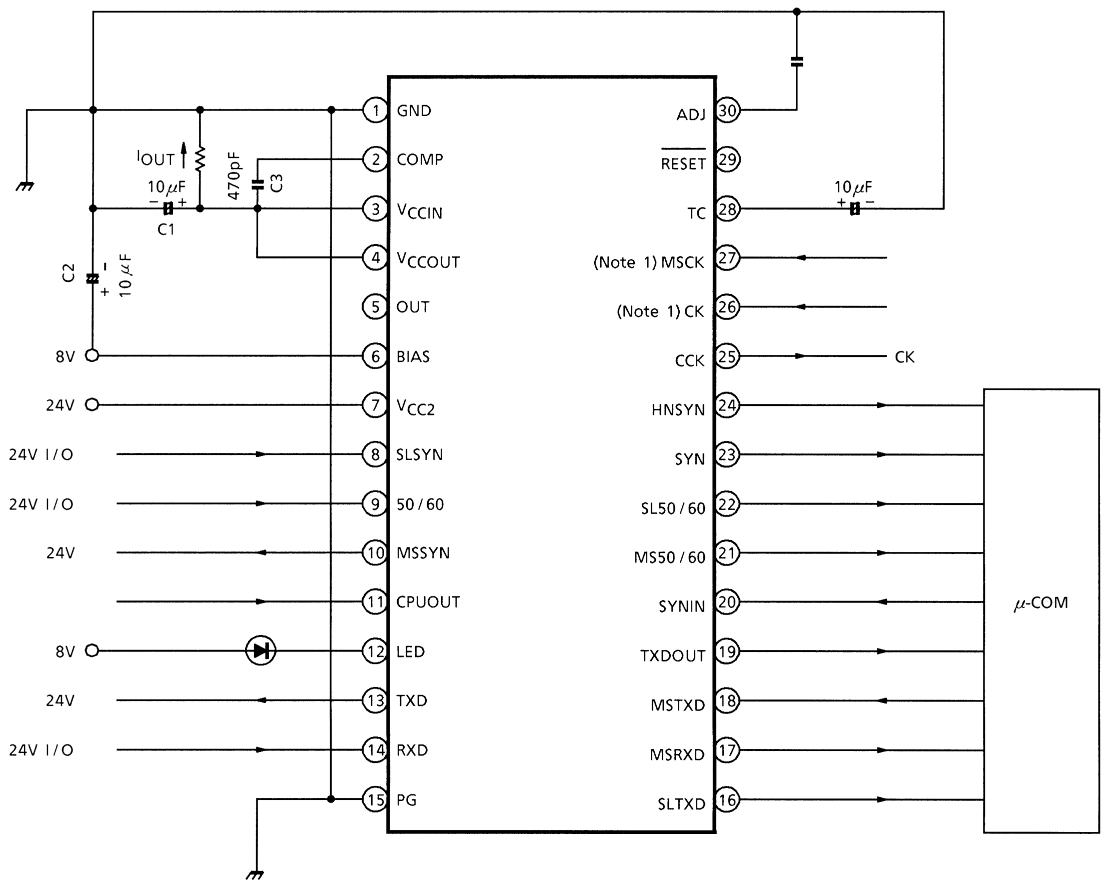

Note 1: When using the MSCK pin, short circuit the CK pin with GND.
When using the CK pin, short circuit the MSCK pin with GND.

Note 2: C1 and C2 are necessary to absorb external noise, etc. Connect them as close to the IC as possible.
C3 is used for phase correction, but this also must be connected as close to the IC as possible.
We recommend that C4 be connected between OUT and $V_{CCIN}$.

## PRECAUTIONS for USING

This IC does not integrate protection circuits such as overcurrent and overvoltage protectors.
Thus, if excess current or voltage is applied to the IC, the IC may be damaged. Please design the IC so that excess current or voltage will not be applied to the IC.
Utmost care is necessary in the design of the output line, $V_{CC}$ ($V_{CCIN}$, $V_{CCOUT}$, BIAS, $V_{CC2}$) and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

When using a built−in PNP transistor :

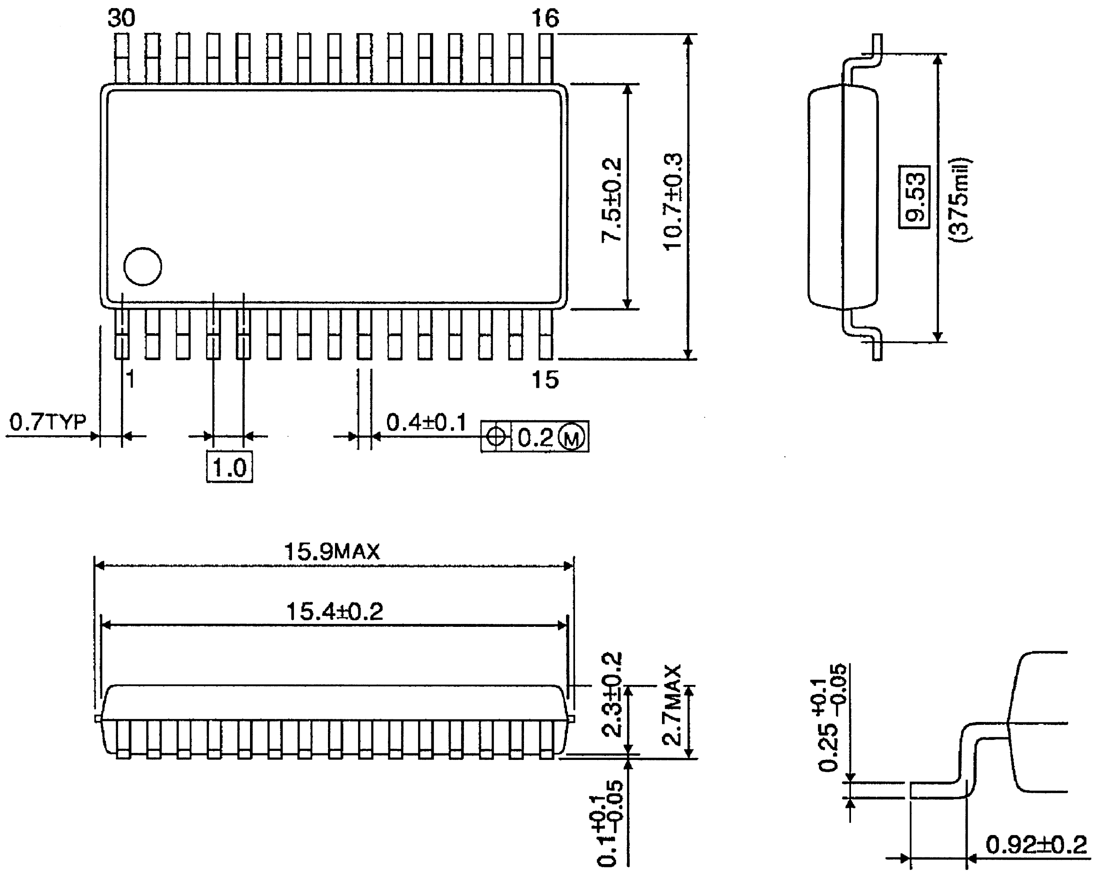



Note 1: When using the MSCK pin, short the CK pin with GND.
When using the CK pin, short the MSCK pin with GND.

Note 2: C1 and C2 are necessary to absorb external noise, etc.
Connect them as close to the IC as possible.
C3 is used for phase correction, but this also must be connected as close to the IC as possible.

## PACKAGE DIMENSIONS

SSOP30−P−375−1.00 Unit: mm




Weight: 0.63 g (Typ.)

## Notes on Contents

### 1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

### 2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### 3. Timing Charts

Timing charts may be simplified for explanatory purposes.

### 4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

## IC Usage Considerations

### Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

## Points to Remember on Handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

- Solderability

(1) Use of Sn-37Pb solder Bath
- · solder bath temperature = 230°C
- · dipping time = 5 seconds
- · the number of times = once
- · use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- · solder bath temperature = 245°C
- · dipping time = 5 seconds
- · the number of times = once
- · use of R-type flux