TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH245FU, TC7WH245FK

DUAL BUS TRANSCEIVER

The TC7WH245 is an advanced high speed CMOS DUAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

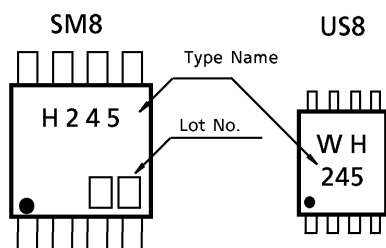All inputs are equipped with protection circuits against static discharge.

FEATURES
- High Speed ·························· $t_{pd} = 4.0\,ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation ············ $I_{CC} = 4\mu A$ (Max.) at $Ta = 25°C$
- High Noise Immunity ·············· $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min.)
- Balanced Propagation Delays ······ $t_{pLH} \doteq t_{pHL}$
- Wide Operating Voltage Range··· V_{CC} (opr) $= 2 \sim 5.5V$
- Low Noise ························· $V_{OLP} = 0.8V$ (Max.)

TC7WH245FU

SSOP8-P-0.65

TC7WH245FK

SSOP8-P-0.50A

Weight
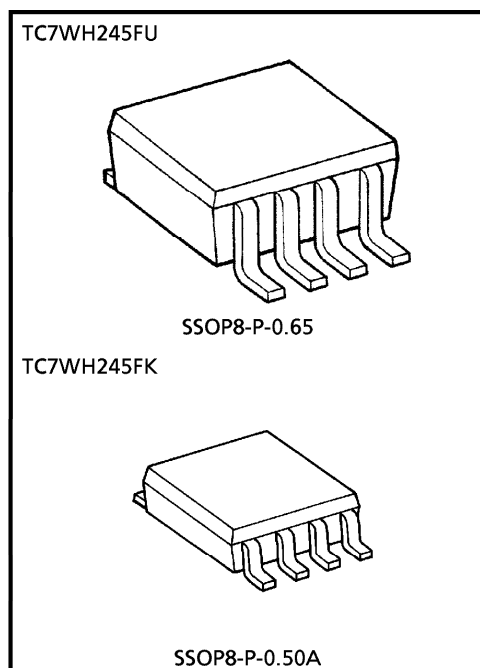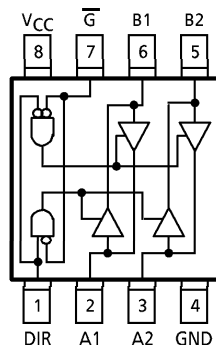SSOP8-P-0.65   : 0.02g (Typ.)
SSOP8-P-0.50A : 0.01g (Typ.)

APPLICATION NOTES
1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.
3) A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

MARKING

SM8   US8

Type Name

H 2 4 5

Lot No.

W H
245

PIN ASSIGNMENT (TOP VIEW)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	300 (SM8)	mW
		200 (US8)	
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature (10 s)	T_L	260	°C

LOGIC DIAGRAM
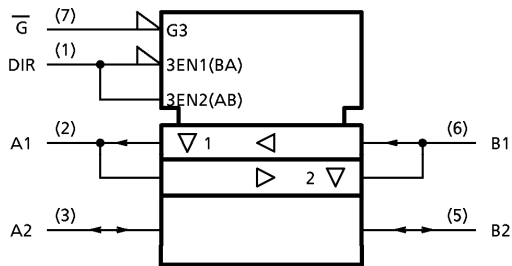
TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	×	High impedance		Z

× : Don't care
Z : High impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim 5.5$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt / dv	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3$V)	ns / V
		$0 \sim 20$ ($V_{CC} = 5 \pm 0.5$V)	

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—	
Low-Level Input Voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4mA$	3.0	2.58	—	—	2.48	—	
			$I_{OH} = -8mA$	4.5	3.94	—	—	3.80	—	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4mA$	3.0	—	—	0.36	—	0.44	
			$I_{OL} = 8mA$	4.5	—	—	0.36	—	0.44	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		5.5	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	$V_{IN} = 5.5V$ or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	2.0	—	20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
		V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}	3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	ns
			50	—	8.3	11.9	1.0	13.5	
		5.0 ± 0.5	15	—	4.0	5.5	1.0	6.5	
			50	—	5.5	7.5	1.0	8.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	3.3 ± 0.3 ($R_L = 1k\Omega$)	15	—	8.5	13.2	1.0	15.5	ns
			50	—	11.0	16.7	1.0	19.0	
		5.0 ± 0.5	15	—	5.8	8.5	1.0	10.0	
			50	—	7.3	10.6	1.0	12.0	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	3.3 ± 0.3 ($R_L = 1k\Omega$)	50	—	11.5	15.8	1.0	18.0	ns
		5.0 ± 0.5	50	—	7.0	9.7	1.0	11.0	
Output to Output Skew	t_{osLH} t_{osHL}	3.3 ± 0.3 (Note 1)	50	—	—	1.5	—	1.5	ns
		5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C_{IN}	DIR, $\overline{G}$		—	4	10	—	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		—	8	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 2)		—	21	—	—	—	pF

(Note 1) : Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 2) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Ta = 25°C, Input $t_r = t_f = 3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	IMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	− 0.5	− 0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT
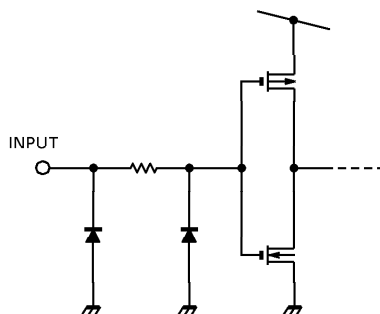
PACKAGE DIMENSIONS

SSOP8-P-0.65
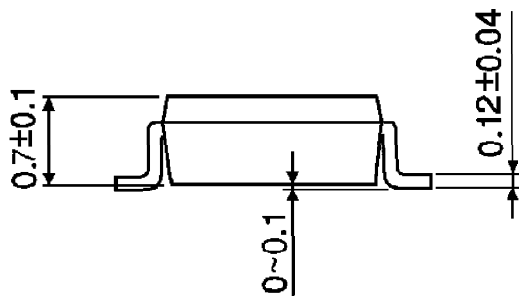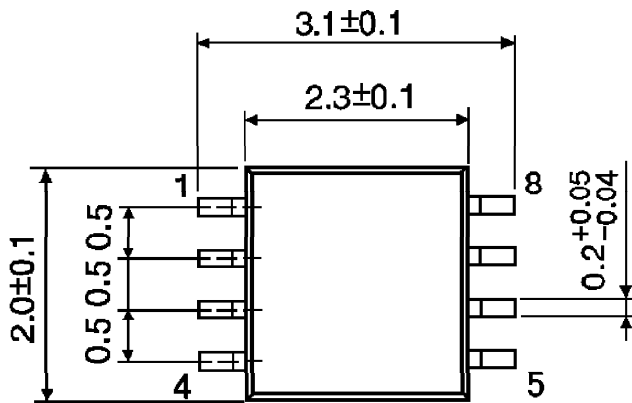
Unit : mm
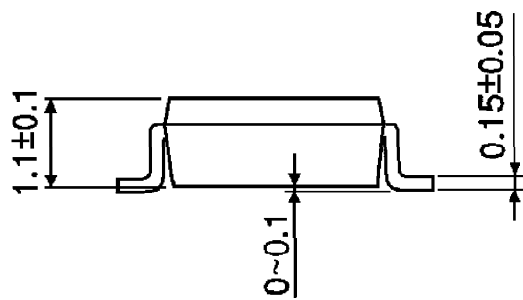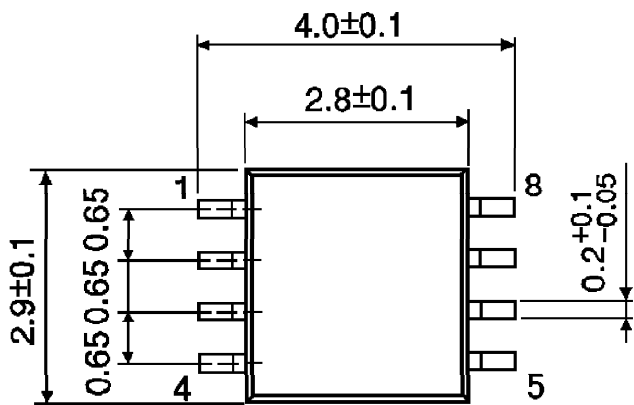
Weight : 0.02g (Typ.)

PACKAGE DIMENSIONS
SSOP8-P-0.50A

Unit : mm

Weight : 0.01g (Typ.)

RESTRICTIONS ON PRODUCT USE