TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

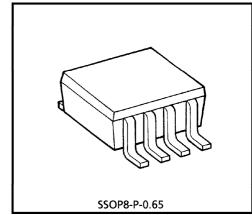
T C 7 W 2 4 0 F U

INVERTED, 3-STATE OUTPUTS

The TC7W240FU is a high speed C²MOS DUAL BUS BUFFERS fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

It is an inverting 3-state buffer having two active-low output enables.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

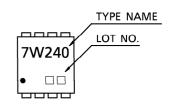


Weight: 0.02g (Typ.)

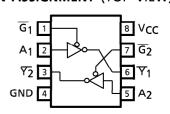
FEATURES

- High Speed $t_{pd} = 10$ ns (Typ.) at
- Low Power Dissipation $\cdots I_{CC} = 2\mu A$ (Max.) at $Ta = 25^{\circ}C$
- High Noise Immunity ················V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance ····· |I_{OH}| = I_{OL} = 6mA (Min.)
- Balanced Propagation Delays $\cdots t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range······ V_{CC} (opr) = 2∼6V

MARKING



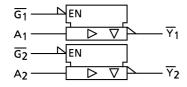
PIN ASSIGNMENT (TOP VIEW)



MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	Vout	-0.5~V _{CC} +0.5	٧
Input Diode Current	lικ	± 20	mΑ
Output Diode Current	^I ОК	± 20	mA
DC Output Current	lout	± 35	mA
DC V _{CC} /Ground Current	lcc	± 37.5	mA
Power Dissipation	PD	300	mW
Storage Temperature	T _{stg}	-65∼150	°C
Lead Temperature (10s)	TL	260	°C

LOGIC DIAGRAM



TRUTH TABLE

INP	TU	OUTPUT				
G	Α	Y				
L	L	Н				
L	Ι	L				
Н	Х	Z				

X : Don't Care Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	۷сс	2~6	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	VOUT	0~V _{CC}	V
Operating Temperature	T _{opr}	-40∼85	°C
		$0 \sim 1000 \text{ (V}_{CC} = 2.0\text{V)}$	
Input Rise and Fall Time	t _r , t _f	$0\sim 500 \ (V_{CC} = 4.5V)$	ns
		$0 \sim 400 \ (V_{CC} = 6.0V)$	

DC ELECTRICAL CHARACTERISTICS

DADAMETED	6) (1 4 1 2 0 1	TEST	TEGT CONDITION			Ta = 25°C			Ta = −40~85°C		
		CIR- TEST CONDITION CUIT		Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT	
High-Level Input Voltage	V _{IH}	_	_		2.0 4.5 6.0	1.5 3.15 4.2		_	1.5 3.15 4.2		V
Low-Level Input Voltage	V _{IL}	_	_		2.0 4.5 6.0	_ _ _	_ _ _	0.5 1.35 1.8		0.5 1.35 1.8	V
High-Level Output Voltage	Voн	_	- V _{IN} = V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		V
				$I_{OH} = -6mA$ $I_{OH} = -7.8mA$	4.5 6.0	4.18 5.68	4.31 5.80	_	4.13 5.63		
Low-Level Output Voltage	V _{OL}	_	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA I _{OL} = 6mA I _{OL} = 7.8mA	2.0 4.5 6.0 4.5 6.0	_ _ _	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	_ _ _	0.1 0.1 0.1 0.33 0.33	V
3-State Output Off-State Current	loz	_	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	_	_	± 0.5	_	± 5.0	
Input Leakage Current	IN	_	V _{IN} = V _{CC} or GND		6.0	_	_	±0.1	_	± 1.0	μ A
Quiescent Supply Current	lcc	_	V _{IN} = V _{CC} or GND		6.0	_	_	2.0	_	20.0	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

	CVMDOL	TEST CIR- CUIT	CONDITION			Ta = 25°C			Ta = −40~85°C		
PARAMETER	SYMBOL			CL	Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Output Transition	4				2.0	_	25	60	_	75	
Time	t _{TLH}	—	_	50	4.5		7	12	_	15	
Tillie	^t THL				6.0	_	6	10	-	13	
					2.0		36	90		115	
				50	4.5	<u> </u>	12	18	_	23	
Propagation	^t PLH	l	_		6.0	_	10	15	_	20	
Delay Time	^t pHL		_		2.0		51	130	_	165	
				150	4.5	_	17	26	_	33	
					6.0	_	14	22	_	28	ns
	^t pZL		$R_L = 1k\Omega$	50	2.0		48	125	_	155	113
					4.5	_	16	25	_	31	-
					6.0	_	14	21		26	
	^t pZH			150	2.0	_	63	165	_	205	
					4.5	_	21	33	_	41	
					6.0	_	18	28		35	
Output Disable	^t pLZ ^t pHZ				2.0		32	125	_	155	
Time		—	$R_L = 1k\Omega$	50	4.5	_	15	25	_	31	
					6.0	_	14	21	_	26	
Input Capacitance	CIN	_	_	_	_		5	10	-	10	
Output Capacitance	C _{OUT}	_	_	_	_	_	10	_		_	pF
Power Dissipation Capacitance	C _{PD}	_	Note (1)			_	31	_		_	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

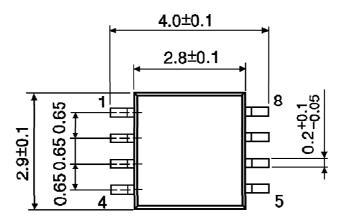
Average operating current can be obtained by the equation:

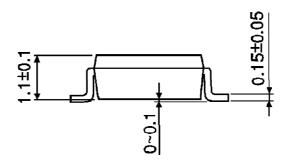
I_{CC} (opr) = C_{PD}·V_{CC}·f_{IN} + I_{CC}/2 (per Gate)

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PACKAGE DIMENSIONS

SSOP8-P-0.65 Unit: mm





Weight: 0.02g (Typ.)

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