TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

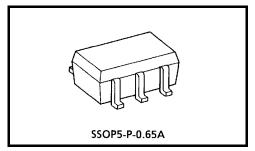
TC7SB384FU

Single Bus Switch

The TC7SB384FU provides single bit of high-speed TTL-compatible switching. The low on resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as just $\underline{1}$ -bit low-impedance switch with output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is \underline{on} and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits against static discharge.

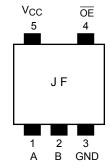


Weight: 0.006 g (typ.)

Features

- Operating voltage: $V_{CC} = 4.5 \sim 5.5 \text{ V}$
- High speed operation: $t_{pd} = 0.25 \text{ ns (max)}$
- Low on resistance: $RON = 5 \Omega$ (typ.)
- ESD performance: Machine model $\geq \pm 200 \text{ V}$ Human body model $\geq \pm 2000 \text{ V}$
- TTL level input (control input)
- Package: USV

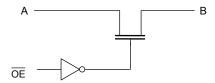
Pin Assignment (top view)



Truth Table

Input	Function	
ŌE	Function	
L	A port = B port	
Н	Disconnect	

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply range	V _{CC}	-0.5~7.0	V
DC input voltage	V _{IN}	-0.5~7.0	٧
DC switch voltage	Vs	-0.5~7.0	٧
Input diode current	I _{IK}	-50	mA
Continuous channel current	IS	128	mA
Power dissipation	P _D	200	mW
DC V _{CC} /GND current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	4.5~5.5	٧
Input voltage	V _{IN}	0~5.5	V
Switch voltage	Vs	0~5.5	V
Operating temperature	T _{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Electrical Characteristics

DC Characteristics ($Ta = -40 \sim 85$ °C)

Characte	ristics	Symbol	Test Condition		1	Min	Тур.	Max	Unit
Gridiando	101100	Cymbol	10010	orialion	V _{CC} (V)		(Note 1)	IVIAX	Orint
Input voltage	"H" level	V _{IH}	-	_	4.5~5.5	2.0	_	_	V
input voltage	"L" level	V _{IL}	_	_	4.5~5.5	_	_	8.0	V
Input leakage cur	rent	I _{IN}	V _{IN} = 0~5.5 V		4.5~5.5	_	_	±1.0	μА
Power off leakage	e current	I _{OFF}	A, B, $\overline{OE} = 0 \sim 5.5 \text{ V}$		0	_	_	±1.0	μА
Off-state leakage	current	la-	A, B = 0~5.5 V, OE = V _{CC}		4.5~5.5			±1.0	μА
(switch off)		I _{SZ}			4.5~5.5			±1.0	μΑ
ON resistance			V _{IS} = 0 V	$I_{IS} = 30 \text{ mA}$	4.5		5	7	
ON resistance	(Note2)	R _{ON}	VIS – U V	I _{IS} = 64 mA	4.5		5	7	Ω
	(NOIEZ)		$V_{IS} = 2.4 \text{ V}, I_{IS} = 15 \text{ mA}$		4.5	_	10	15	
Quiescent supply	current	Icc	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$		5.5		_	10	μА
Quiescent supply	Current	Δlcc	V _{IN} = 3.4 V (one input)		5.5	_	_	2.5	mA

Note 1: Typical values are at $V_{CC} = 5 \text{ V}$ and $Ta = 25^{\circ}\text{C}$.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics ($Ta = -40 \sim 85$ °C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t _{pLH} t _{pHL}	Figure 1, Figure 2 (Note)	4.5	_	0.25	ns
Output enable time	t _{pZL}	Figure 1, Figure 3	4.5	_	4.0	ns
Output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	4.5		4.5	ns

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

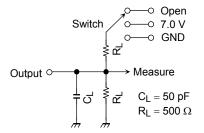
Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Control pin input capacitance	C _{IN}	(Note)	5.0	3	pF
Switch terminal capacitance	C _{I/O}	$\overline{OE} = V_{CC}$ (Note)	5.0	10	pF

3

Note: This item is guaranteed by design.

AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	7.0 V
t _{pHZ} , t _{pZH}	Open

Figure 1

AC Waveform

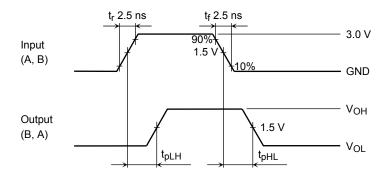


Figure 2 t_{pLH}, t_{pHL}

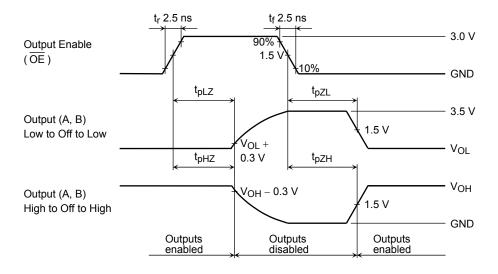
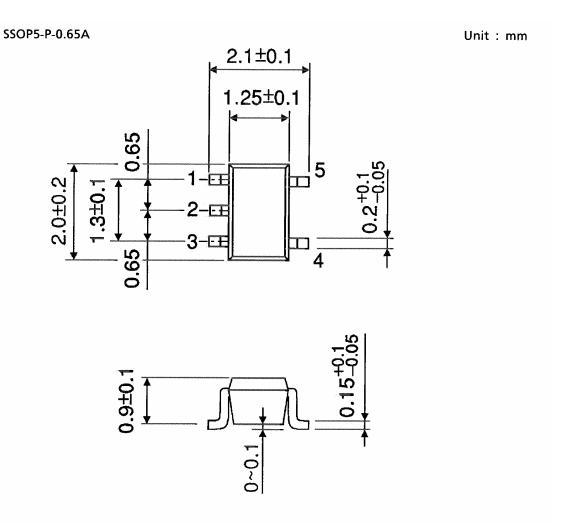


Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Package Dimensions



5

Weight: 0.006 g (typ.)

2007-10-19

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20070701-EN GENERAL

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