Precision, Dual-Channel, JFET Input Rail-to-Rail Instrumentation Amplifier

Preliminary Technical Data

AD8224

FEATURES

- Two channels in a small 4 mm × 4 mm LFCSP
- Low input currents
  - 10 pA maximum input bias current (B grade)
  - 0.6 pA maximum input offset current (B grade)
- High CMRR
  - 100 dB CMRR (minimum), G = 10 (B grade)
  - 80 dB CMRR (minimum) to 5 kHz, G = 1 (B grade)
- Excellent ac specifications and low power
  - 1.5 MHz bandwidth (G = 1)
  - 14 nV/√Hz input noise (1 kHz)
  - Slew rate 2 V/µs
  - 750 µA quiescent supply current per amplifier (maximum)
- Versatility
  - Rail-to-rail output
  - Input voltage range to below negative supply rail
  - 4 kV ESD protection
  - 4.5 V to 36 V single supply
  - ±2.25 V to ±18 V dual supply
  - Gain set with single resistor (G = 1 to 1000)

APPLICATIONS

Medical instrumentation
Precision data acquisition
Transducer interface
Differential drive for
High resolution input ADCs
Remote sensors

FUNCTIONAL BLOCK DIAGRAM

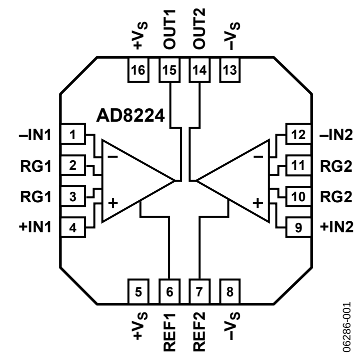

Figure 1. 4mm × 4 mm LFCSP

Table 1. In Amps and Difference Amplifiers by Category

High Perform.	Low Cost	High Volt.	Mil Grade	Low Power	Digital Gain
AD8220[1]	AD8553[1]	AD628	AD620	AD627[1]	AD8555[1]
AD8221	AD623[1]	AD629	AD621		AD8556[1]
AD8222			AD524		AD8557[1]
AD8224[1]			AD526		
			AD624		

[1] Rail-to-rail output.

GENERAL DESCRIPTION

The AD8224 is the first single-supply junction field effect transistor (JFET) input instrumentation amplifier available in the space-saving 16-lead, 4 mm×4 mm LFCSP. It requires the same board area as a typical single instrumentation amplifier, yet doubles the channel density and offers a lower cost per channel without compromising performance.

Designed to meet the needs of high performance, portable instrumentation, the AD8224 has a minimum common-mode rejection ratio (CMRR) of 86 dB at dc and a minimum CMRR of 80 dB at 5 kHz for G = 1. Maximum input bias current is 10 pA and typically remains below 300 pA over the entire industrial temperature range. Despite the JFET inputs, the AD8224 typically has a noise corner of only 10 Hz.

With the proliferation of mixed-signal processing, the number of power supplies required in each system has grown.

Designed to alleviate this problem, the AD8224 can operate on a ±18 V dual supply, as well as on a single +5 V supply. The device's rail-to-rail output stage maximizes dynamic range on the low voltage supplies common in portable applications. Its ability to run on a single 5 V supply eliminates the need for higher voltage, dual supplies. The AD8224 draws a maximum of 750 µA of quiescent current per amplifier, making it ideal for battery-powered devices.

In addition, the AD8224 can be configured as a single-channel, differential output instrumentation amplifier. Differential outputs provide high noise immunity, which can be useful when the output signal must travel through a noisy environment, such as with remote sensors. The configuration can also be used to drive differential input ADCs.

For a single-channel version, use the AD8220 device.

Rev. PrB

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SPECIFICATIONS

$V_S+ = +15$ V, $V_S- = -15$ V, $V_{REF} = 0$ V, $T_A = +25°C$, G = 1, $R_L = 2$ kΩ, unless otherwise noted.

Table 2. Single-Ended and Differential[1] Output Configuration

Parameter	Test Conditions	A Grade Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	$V_{CM} = \pm10$ V				
G = 1		78			dB
G = 10		94			dB
G = 100		94			dB
G = 1000		94			dB
CMRR at 5 kHz	$V_{CM} = \pm10$ V				
G = 1		74			dB
G = 10		84			dB
G = 100		84			dB
G = 1000		84			dB
NOISE	RTI noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$				
Voltage Noise, 1 kHz					
Input Voltage Noise, e_{ni}	$V_{IN}+$, $V_{IN}- = 0$ V		14		nV√Hz
Output Voltage Noise, e_{no}	$V_{IN}+$, $V_{IN}- = 0$ V		90		nV√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1			5		µV p-p
G = 1000			0.8		µV p-p
Current Noise	f = 1 kHz		1		fA/√Hz
VOLTAGE OFFSET	RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$				
Input Offset, V_{OSI}				250	µV
Average TC	T = −40°C to +85°C			10	µV/°C
Output Offset, V_{OSO}				750	µV
Average TC	T = −40°C to +85°C			10	µV/°C
Offset RTI vs. Supply (PSR)					
G = 1		86			dB
G = 10		96			dB
G = 100		96			dB
G = 1000		96			dB
INPUT CURRENT (PER CHANNEL)					
Input Bias Current				25	pA
Over Temperature[2]	T = −40°C to +85°C		300		pA
Input Offset Current				2	pA
Over Temperature[2]	T = −40°C to +85°C		5		pA
GAIN	G = 1 + (49.4 kΩ/R_G)				
Gain Range		1		1000	V/V
Gain Error	$V_{OUT} = \pm10$ V				
G = 1				0.06	%
G = 10				0.3	%
G = 100				0.3	%
G = 1000				0.3	%
Gain Nonlinearity	$V_{OUT} = -10$ V to +10 V				
G = 1	$R_L = 10$ kΩ		10	15	ppm
G = 10	$R_L = 10$ kΩ		5	10	ppm
G = 100	$R_L = 10$ kΩ		30	60	ppm

Parameter	Test Conditions	A Grade Min	Typ	Max	Unit
G = 1000	R_L = 10 kΩ		400	500	ppm
G = 1	R_L = 2 kΩ		10	15	ppm
G = 10	R_L = 2 kΩ		10	15	ppm
G = 100	R_L = 2 kΩ		50	75	ppm
Gain vs. Temperature					
G = 1			3	10	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Impedance (Pin to Ground)[3]			10^4||5		GΩ||pF
Input Operating Voltage Range[4]	V_S = ±2.25 V to ±18 V for dual supplies	$-V_S - 0.1$		$+V_S - 2$	V
Over Temperature	T = −40°C to +85°C	$-V_S - 0.1$		$+V_S - 2.1$	V
OUTPUT					
Output Swing	R_L = 2 kΩ	−14.3		+14.3	V
Over Temperature	T = −40°C to +85°C	−14.3		+14.1	V
Output Swing	R_L = 10 kΩ	−14.7		+14.7	V
Over Temperature	T = −40°C to +85°C	−14.6		+14.6	V
Short-Circuit Current			15		mA
REFERENCE INPUT					
R_{IN}			40		kΩ
I_{IN}	$V_{IN}+$, $V_{IN}-$ = 0 V			70	µA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0001		V/V
POWER SUPPLY (PER AMPLIFIER)					
Operating Range		±2.25[5]		±18	V
Quiescent Current				750	µA
Over Temperature	T = −40°C to +85°C			850	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+85	°C
Operational[6]		−40		+125	°C

[1] Refers to differential configuration shown in Figure 64.
[2] Please refer to Figure 16 and Figure 17 for the relationship between input current and temperature.
[3] Differential and common-mode input impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[4] The AD8224 can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.
[5] At this supply voltage, ensure that the input common-mode voltage is within the input voltage range specification.
[6] The AD8224 is characterized from −40°C to +125°C. See the Typical Performance Characteristics section for expected operation in this temperature range.

$V_S+ = +15\ V$, $V_S- = -15\ V$, $V_{REF} = 0\ V$, $T_A = +25°C$, G = 1, $R_L = 2\ k\Omega$, unless otherwise noted.

Table 3. Single-Ended Output Configuration—Dynamic Performance (Both Amplifiers)

Parameter	Conditions	A Grade Min	A Grade Typ	A Grade Max	Unit
DYNAMIC RESPONSE					
Small Signal Bandwidth –3 dB					
G = 1			TBD		kHz
G = 10			TBD		kHz
G = 100			TBD		kHz
G =1000			TBD		kHz
Settling Time 0.01%	10 V step				
G = 1			TBD		µs
G = 10			TBD		µs
G = 100			TBD		µs
G =1000			TBD		µs
Settling Time 0.001%	10 V step				
G = 1			TBD		µs
G = 10			TBD		µs
G = 100			TBD		µs
G =1000			TBD		µs
Slew Rate					
G = 1 to 100		TBD			V/µs

Please fill in TBDs if you can.

$V_S+ = +15\ V$, $V_S- = -15\ V$, $V_{REF} = 0\ V$, $T_A = +25°C$, G = 1, $R_L = 2\ k\Omega$, unless otherwise noted.

Table 4. Differential Output Configuration[1]—Dynamic Performance

Parameter	Conditions	A Grade Min	A Grade Typ	A Grade Max	Unit
DYNAMIC RESPONSE					
Small Signal Bandwidth–3 dB					
G = 1			TBD		kHz
G = 10			TBD		kHz
G = 100			TBD		kHz
G =1000			TBD		kHz
Settling Time 0.01%	10 V step				
G = 1			TBD		µs
G = 10			TBD		µs
G = 100			TBD		µs
G =1000			TBD		µs
Settling Time 0.001%	10 V step				
G = 1			TBD		µs
G = 10			TBD		µs
G = 100			TBD		µs
G =1000			TBD		µs
Slew Rate					
G = 1 to 100		TBD			V/µs

[1] Refers to differential configuration shown in Figure 64.

$V_S+ = 5$ V, $V_S- = 0$ V, $V_{REF} = 2.5$ V, $T_A = +25°C$, G = 1, $R_L = 2$ kΩ, unless otherwise noted.

Table 5. Single-Ended and Differential[1] Output Configuration

Parameter	Test Conditions	A Grade Min	A Grade Typ	A Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 to 2.5 V				
G = 1		78			dB
G = 10		94			dB
G = 100		94			dB
G = 1000		94			dB
CMRR at 5 kHz					
G = 1		74			dB
G = 10		84			dB
G = 100		84			dB
G = 1000		84			dB
NOISE	RTI noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$				
Voltage Noise, 1 kHz					
Input Voltage Noise, e_{ni}	$V_{IN}+$, $V_{IN}-$ = 0 V, V_{REF} = 0 V		14		nV√Hz
Output Voltage Noise, e_{no}	$V_{IN}+$, $V_{IN}-$ = 0 V, V_{REF} = 0 V		90		nV√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1			5		µV p-p
G = 1000			0.8		µV p-p
Current Noise	f = 1 kHz		1		fA/√Hz
VOLTAGE OFFSET	RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$				
Input Offset, V_{OSI}				300	µV
Average TC	T = −40°C to +85°C			10	µV/°C
Output Offset, V_{OSO}				800	µV
Average TC	T = −40°C to +85°C			10	µV/°C
Offset RTI vs. Supply (PSR)					
G = 1		86			dB
G = 10		96			dB
G = 100		96			dB
G = 1000		96			dB
INPUT CURRENT (PER CHANNEL)					
Input Bias Current				25	pA
Over Temperature[2]	T = −40°C to +85°C		300		pA
Input Offset Current				2	pA
Over Temperature[2]	T = −40°C to +85°C		5		pA
GAIN	G = 1 + (49.4 kΩ/R_G)				
Gain Range		1		1000	V/V
Gain Error	V_{OUT} = 0.3 V to 2.9 V for G = 1 V_{OUT} = 0.3 V to 3.8 V for G > 1				
G = 1				0.06	%
G = 10				0.3	%
G = 100				0.3	%
G = 1000				0.3	%
Nonlinearity	V_{OUT} = 0.3 V to 2.9 V for G = 1 V_{OUT} = 0.3 V to 3.8 V for G > 1				
G = 1	R_L = 10 kΩ		35	50	ppm
G = 10	R_L = 10 kΩ		35	50	ppm
G = 100	R_L = 10 kΩ		50	75	ppm

Parameter	Test Conditions	A Grade Min	Typ	Max	Unit
G = 1000	R_L = 10 kΩ		650	750	ppm
G = 1	R_L = 2 kΩ		35	50	ppm
G = 10	R_L = 2 kΩ		35	50	ppm
G = 100	R_L = 2 kΩ		50	75	ppm
Gain vs. Temperature					
G = 1			3	10	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Impedance (Pin to Ground)[3]			10^4||6		GΩ||pF
Input Voltage Range[4]		−0.1		$+V_S$ − 2	V
Over Temperature	T = −40°C to +85°C	−0.1		$+V_S$ − 2.	V
OUTPUT					
Output Swing	R_L = 2 kΩ	0.25		4.75	V
Over Temperature	T = −40°C to +85°C	0.3		4.70	V
Output Swing	R_L = 10 kΩ	0.15		4.85	V
Over Temperature	T = −40°C to +85°C	0.2		4.80	V
Short-Circuit Current			15		mA
REFERENCE INPUT					
R_{IN}			40		kΩ
I_{IN}	V_{IN}+, V_{IN}− = 0 V			70	µA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0001		V/V
POWER SUPPLY (PER AMPLIFIER)					
Operating Range		+4.5		+36	V
Quiescent Current				750	µA
Over Temperature	T = −40°C to +85°C			850	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+85	°C
Operational[5]		−40		+125	°C

[1] Refers to differential configuration shown in Figure 64.
[2] Refer to Figure 16 and Figure 17 for the relationship between input current and temperature.
[3] Differential and common-mode impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[4] The AD8224 can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.
[5] The AD8224 is characterized from −40°C to +125°C. See the Typical Performance Characteristics section for expected operation in that temperature range.

$V_S + = 5$ V, $V_S - = 0$ V, $V_{REF} = 2.5$ V, $T_A = +25°C$, G = 1, $R_L = 2$ kΩ, unless otherwise noted.

Table 6. Single-Ended Output Configuration—Dynamic Performance (Both Amplifiers)

Parameter	Conditions	A Grade		
		Min	Typ	Max
DYNAMIC RESPONSE				
Small Signal Bandwidth –3 dB				
G = 1			TBD	
G = 10			TBD	
G = 100			TBD	
G =1000			TBD	
Settling Time 0.01%				
G = 1	3 V Step		TBD	
G = 10	4 V Step		TBD	
G = 100	4 V Step		TBD	
G =1000	4 V Step		TBD	
Settling Time 0.001%				
G = 1	3 V Step		TBD	
G = 10	4 V Step		TBD	
G = 100	4 V Step		TBD	
G =1000	4 V Step		TBD	
Slew Rate				
G = 1 to 100		TBD		

$V_S + = 5$ V, $V_S - = 0$ V, $V_{REF} = 2.5$ V, $T_A = +25°C$, G = 1, $R_L = 2$ kΩ, unless otherwise noted.

Table 7. Differential Output Configuration[1]—Dynamic Performance

Parameter	Conditions	A Grade			Unit
		Min	Typ	Max	
DYNAMIC RESPONSE					
Small Signal Bandwidth –3 dB					
G = 1			TBD		kHz
G = 10			TBD		kHz
G = 100			TBD		kHz
G =1000			TBD		kHz
Settling Time 0.01%					
G = 1	3 V Step		TBD		µs
G = 10	4 V Step		TBD		µs
G = 100	4 V Step		TBD		µs
G =1000	4 V Step		TBD		µs
Settling Time 0.001%					
G = 1	3 V Step		TBD		µs
G = 10	4 V Step		TBD		µs
G = 100	4 V Step		TBD		µs
G =1000	4 V Step		TBD		µs
Slew Rate					
G = 1 to 100		TBD			V/µs

[1] Refers to differential configuration shown in Figure 64.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Supply Voltage	±18 V
Power Dissipation	See Figure 2
Output Short Circuit Current	Indefinite[1]
Input Voltage (Common Mode)	±Vs
Differential Input Voltage	±Vs
Storage Temperature	−65°C to +130°C
Operating Temperature Range[2]	−40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	130°C
Package Glass Transition Temperature	130°C
ESD (Human Body Model)	4 kV
ESD (Charge Device Model)	1 kV
ESD (Machine Model)	0.4 kV

[1]Assumes the load is referenced to mid-supply.
[2]Temperature for specified performance is −40°C to +85°C. For performance to +125°C, see the Typical Performance Characteristics section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

THERMAL RESISTANCE

Table 9.

Thermal Pad	θ_{JA}	Unit
Soldered to Board	48	°C/W
Not Soldered to Board	86	°C/W

The θ_{JA} values in Table 9 assume a 4-layer JEDEC standard board. If the thermal pad is soldered to the board, then it is also assumed it is connected to a plane. θ_{JC} at the exposed pad is 4.4°C/W.

Maximum Power Dissipation

The maximum safe power dissipation for the AD8224 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 130°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 130°C for an extended period can result in a loss of functionality.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the LFCSP on a 4-layer JEDEC standard board.

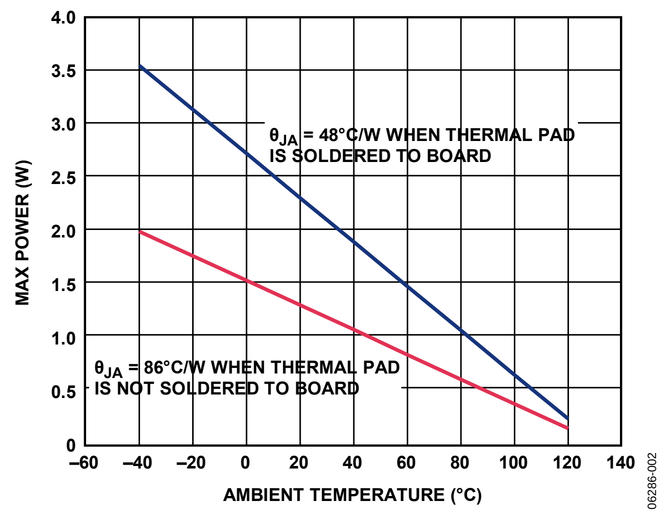
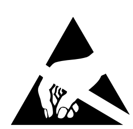


Figure 2. Maximum Power Dissipation

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

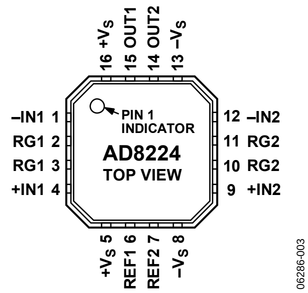


Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No	Mnemonic	Description
1	–IN1	Negative Input In-Amp 1.
2	RG1	Gain Resistor In-Amp 1.
3	RG1	Gain Resistor In-Amp 1.
4	+IN1	Positive Input In-Amp 1.
5	$+V_S$	Positive Supply.
6	REF1	Reference Adjust In-Amp 1.
7	REF2	Reference Adjust In-Amp 2.
8	$-V_S$	Negative Supply.
9	+IN2	Positive Input In-Amp 2.
10	RG2	Gain Resistor In-Amp 2.
11	RG2	Gain Resistor In-Amp 2.
12	–IN2	Negative Input In-Amp 2.
13	$-V_S$	Negative Supply.
14	OUT2	Output In-Amp 2.
15	OUT1	Output In-Amp 1.
16	$+V_S$	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 4. Typical Distribution of CMRR (G = 1)

TBD

Figure 5. Typical Distribution of Input Offset Voltage

TBD

Figure 6. Typical Distribution of Output Offset Voltage

TBD

Figure 7. Typical Distribution of Input Bias Current

TBD

Figure 8. Typical Distribution of Input Offset Current

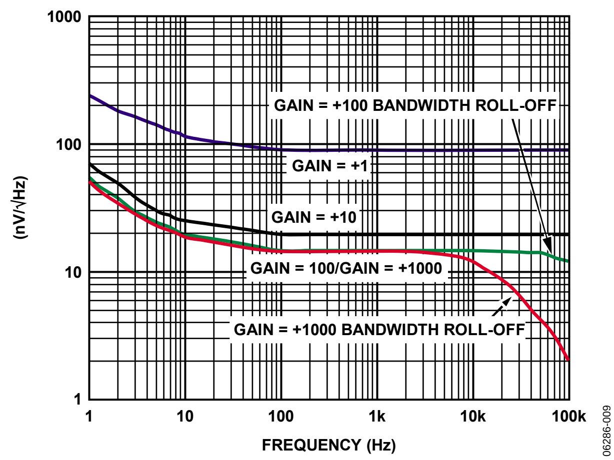


Figure 9. Voltage Spectral Density vs. Frequency

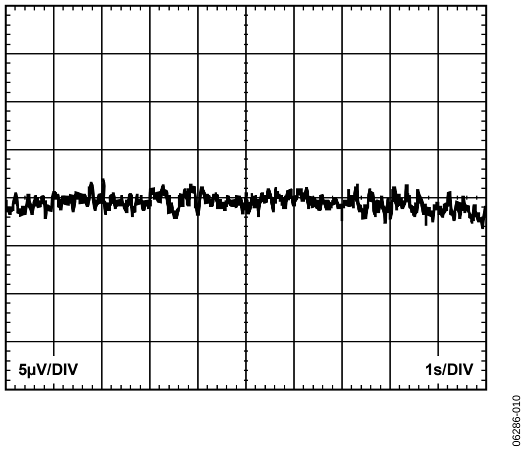


Figure 10. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

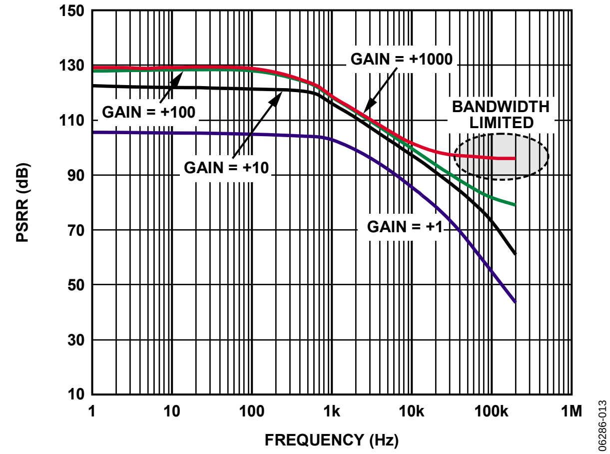


Figure 13. Positive PSRR vs. Frequency, RTI

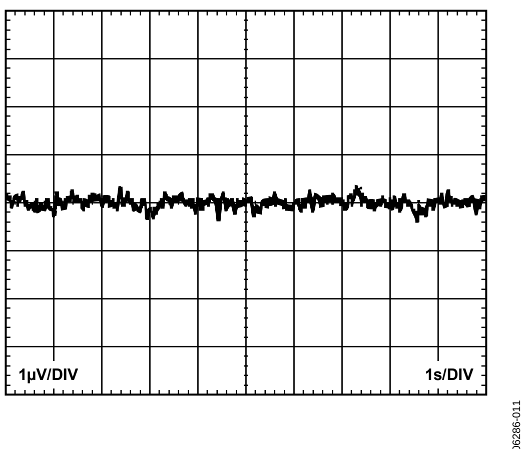


Figure 11. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

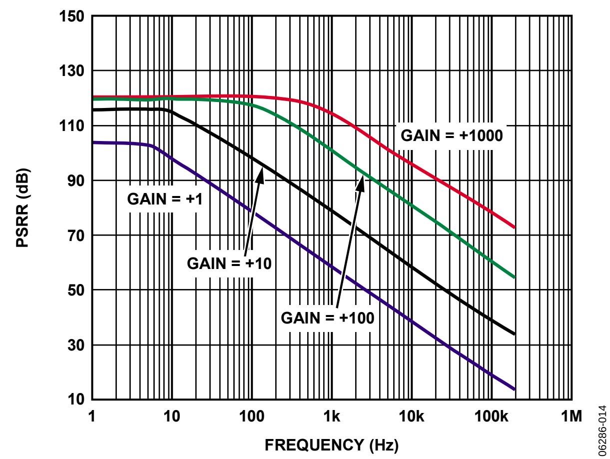


Figure 14. Negative PSRR vs. Frequency, RTI

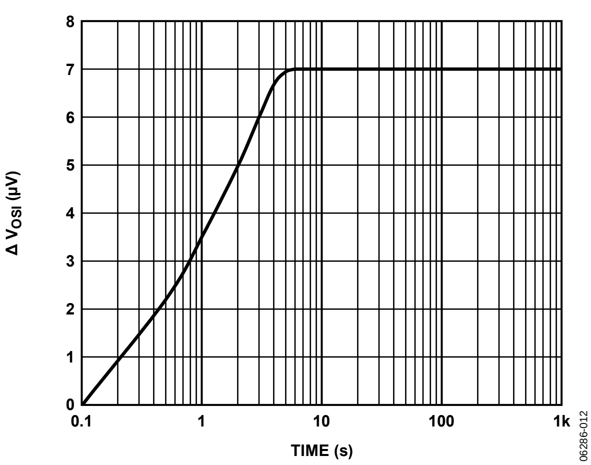


Figure 12. Change in Input Offset Voltage vs. Warmup Time

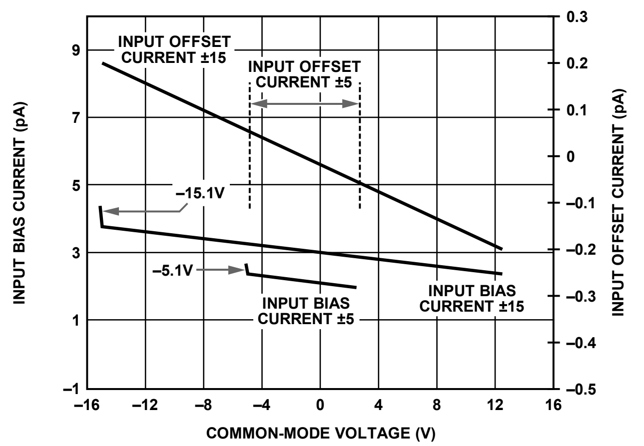


Figure 15. Input Current vs. Common-Mode Voltage

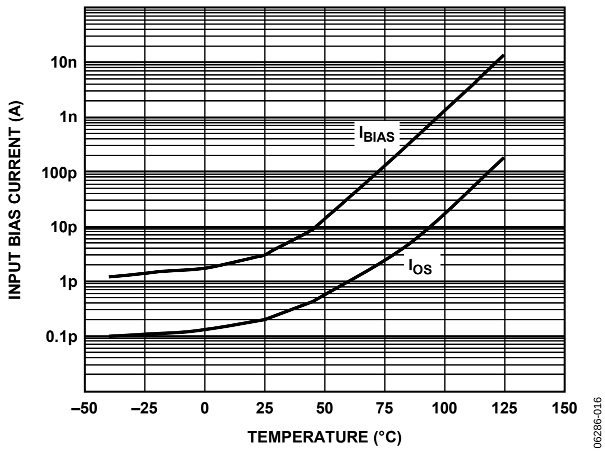


Figure 16. Input Bias Current and Offset Current Temperature, $V_S = \pm 15$ V, $V_{REF} = 0$ V

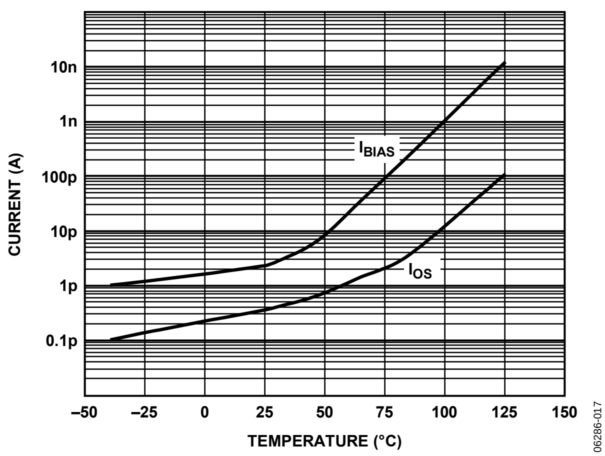


Figure 17. Input Bias Current and Offset Current vs. Temperature, $V_S = +5$ V, $V_{REF} = 2.5$ V

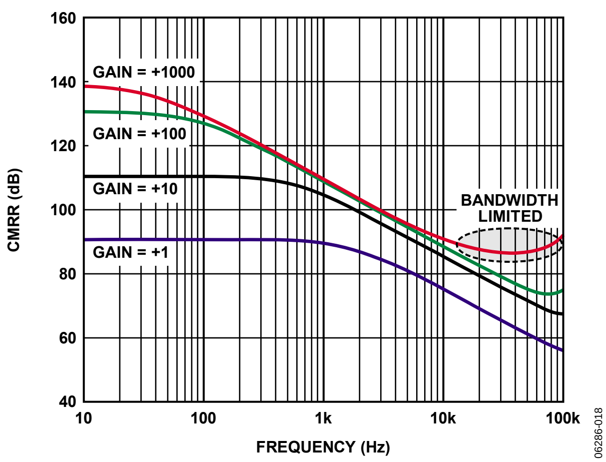


Figure 18. CMRR vs. Frequency

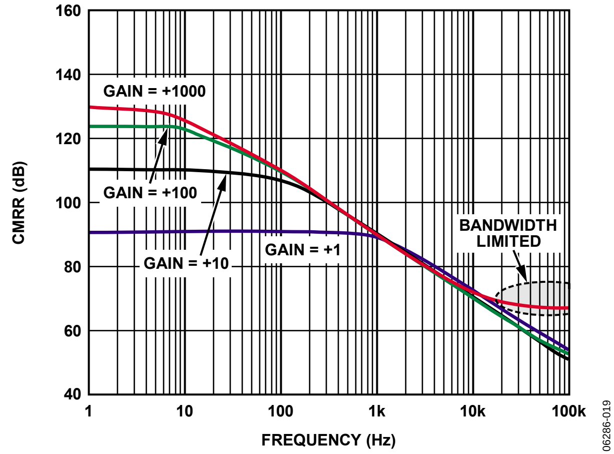


Figure 19. CMRR vs. Frequency, 1 kΩ Source Imbalance

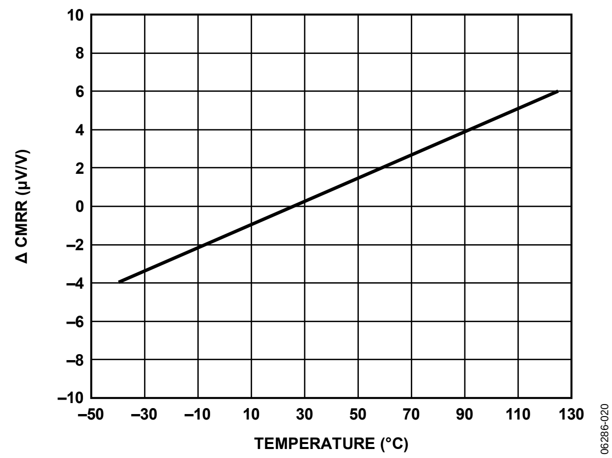


Figure 20. Change in CMRR vs. Temperature, G = 1

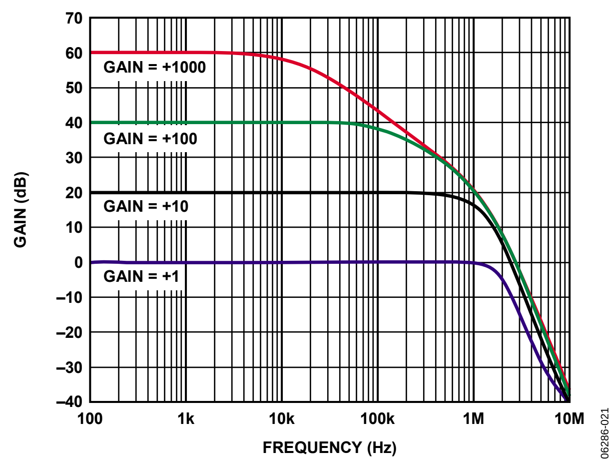


Figure 21. Gain vs. Frequency

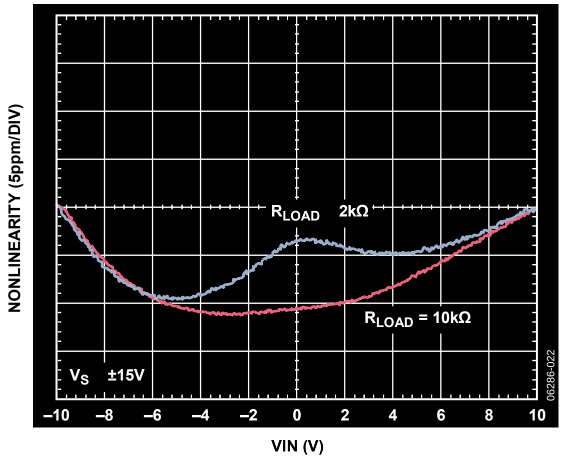


Figure 22. Gain Nonlinearity, G = 1

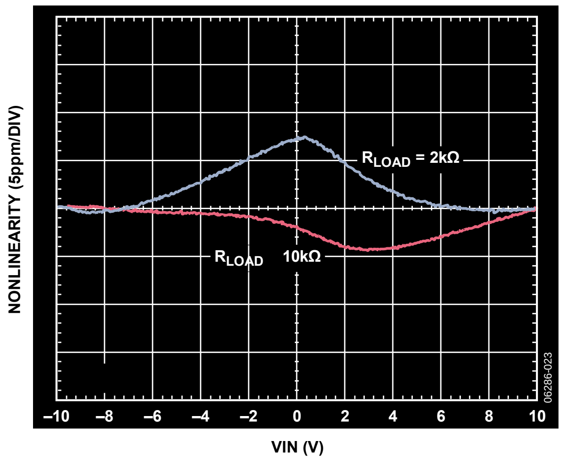


Figure 23. Gain Nonlinearity, G = 10

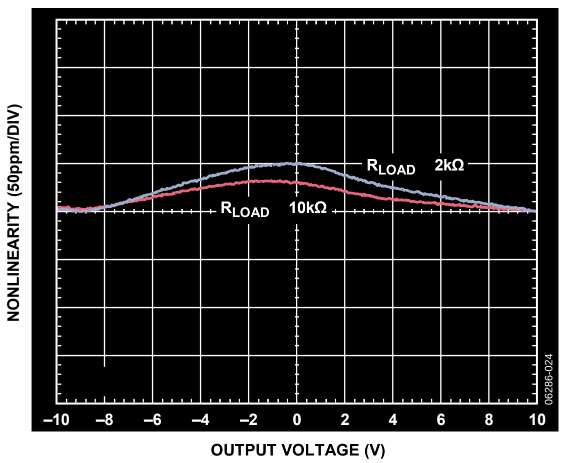


Figure 24. Gain Nonlinearity, G = 100

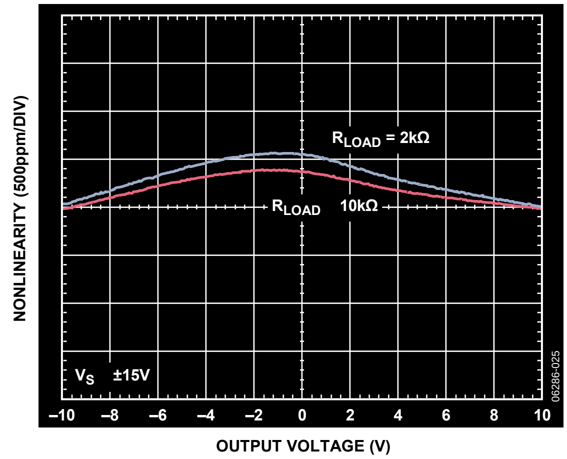


Figure 25. Gain Nonlinearity, G = 1000

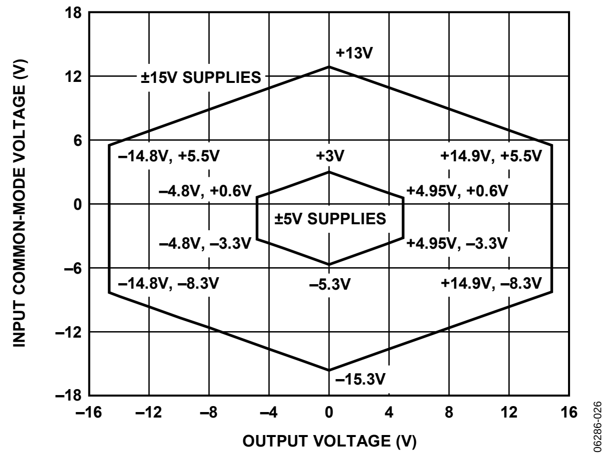


Figure 26. Input Common-Mode Voltage Range vs. Output Voltage, G = 1, V_{REF} = 0 V

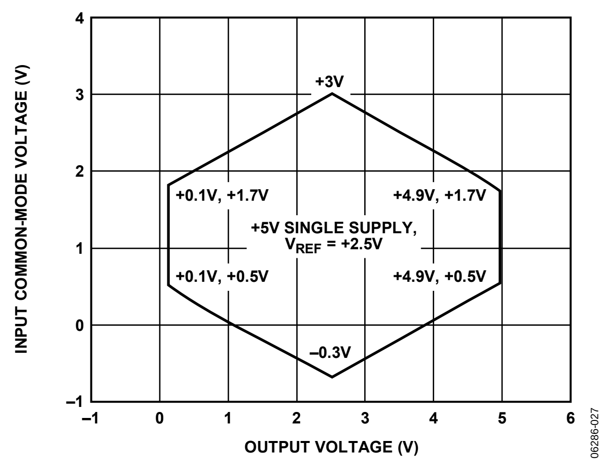


Figure 27. Input Common-Mode Voltage Range vs. Output Voltage, G = 1, V_S = +5 V, V_{REF} = 2.5 V

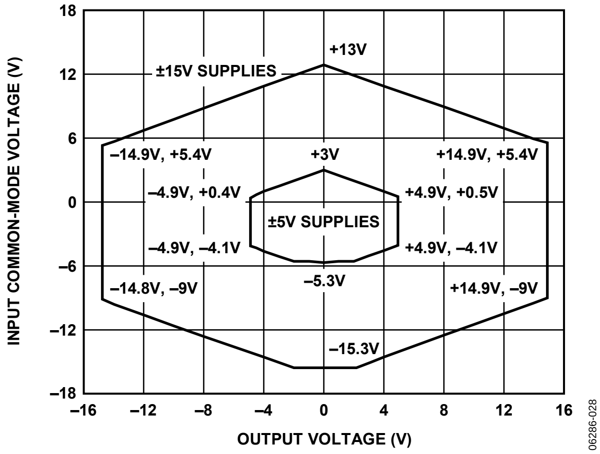


Figure 28. Input Common-Mode Voltage Range vs. Output Voltage, G = 100, V_{REF} = 0 V

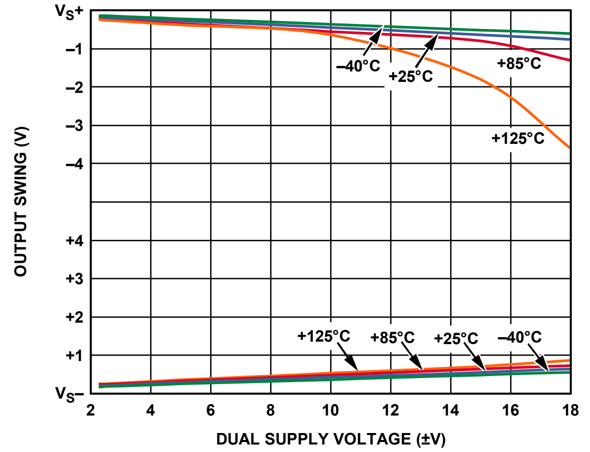


Figure 31. Output Voltage Swing vs. Supply Voltage, R_L = 2 kΩ, G = 10, V_{REF} = 0 V

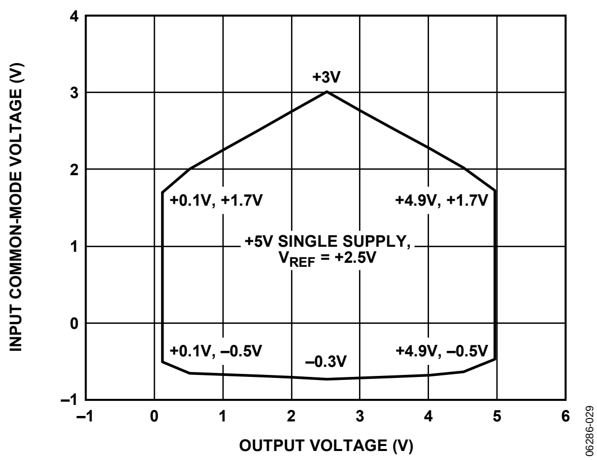


Figure 29. Input Common-Mode Voltage Range vs. Output Voltage, G = 100, V_S = +5 V, V_{REF} = 2.5 V

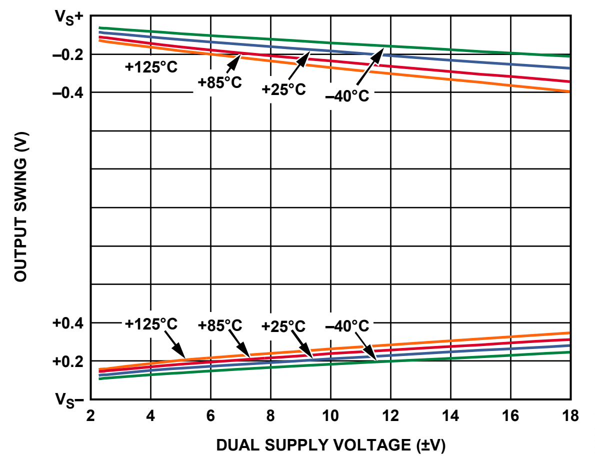


Figure 32. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ, G = 10, V_{REF} = 0 V

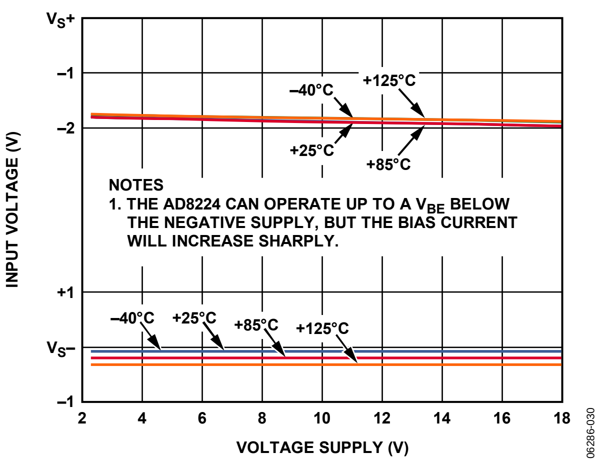


Figure 30. Input Voltage Limit vs. Supply Voltage, G = 1, V_{REF} = 0 V

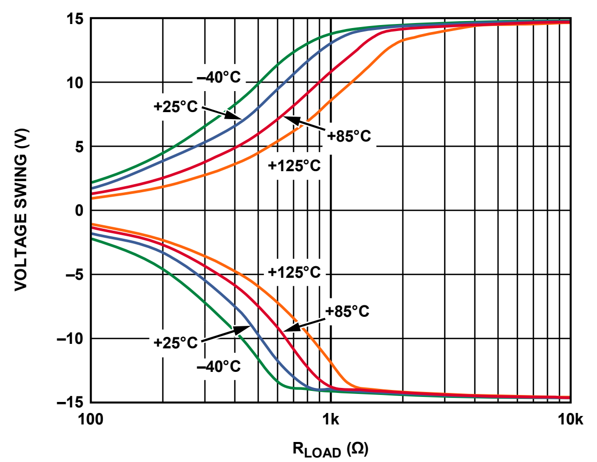


Figure 33. Output Voltage Swing vs. Load Resistance V_S = ±15 V, V_{REF} = 0 V

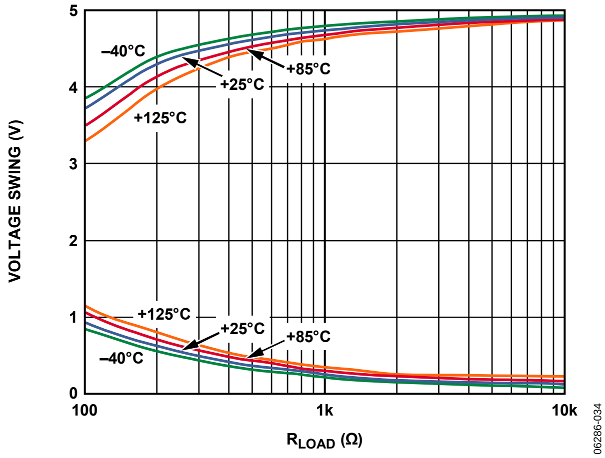


Figure 34. Output Voltage Swing vs. Load Resistance V_S = +5 V, V_{REF} = 2.5 V

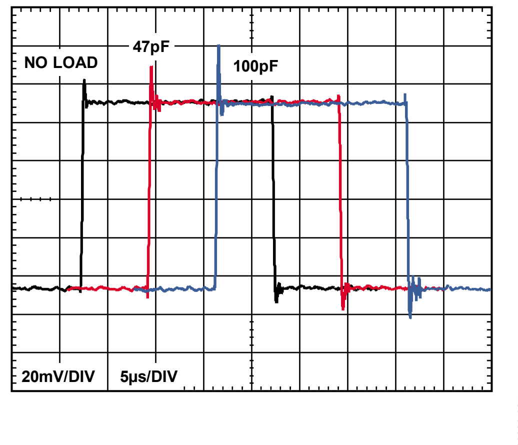


Figure 37. Small Signal Pulse Response for Various Capacitive Loads, V_S = ±15 V, V_{REF} = 0 V

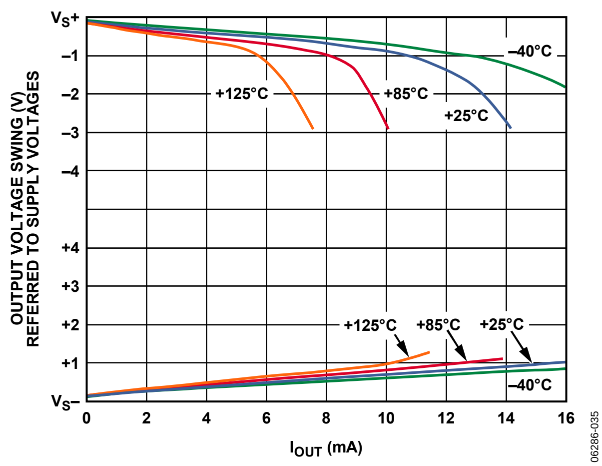


Figure 35. Output Voltage Swing vs. Output Current, V_S = ±15 V, V_{REF} = 0 V

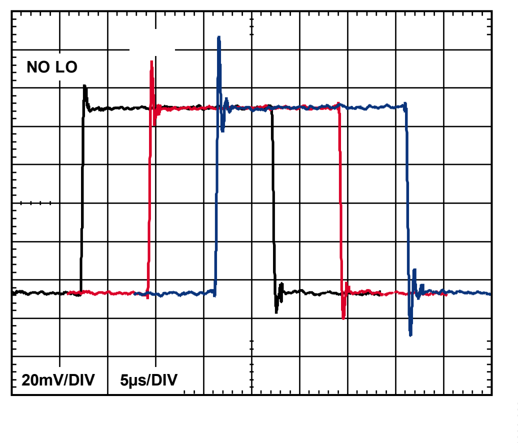


Figure 38. Small Signal Pulse Response for Various Capacitive Loads, V_S = +5 V, V_{REF} = 2.5 V

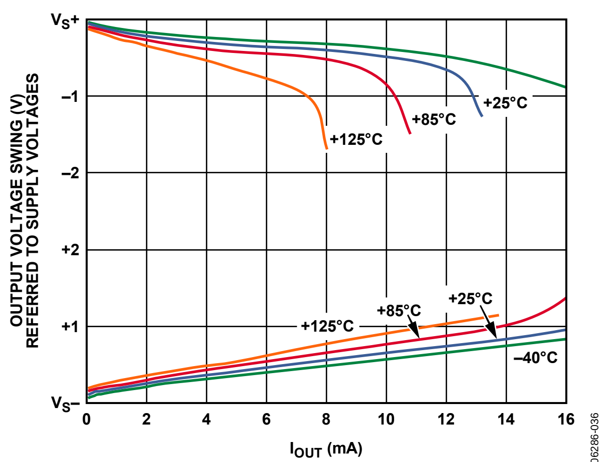


Figure 36. Output Voltage Swing vs. Output Current, V_S = +5 V, V_{REF} = 2.5 V

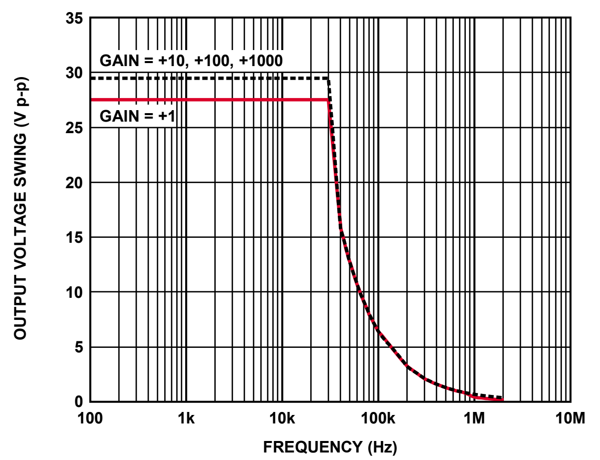


Figure 39. Output Voltage Swing vs. Large Signal Frequency Response

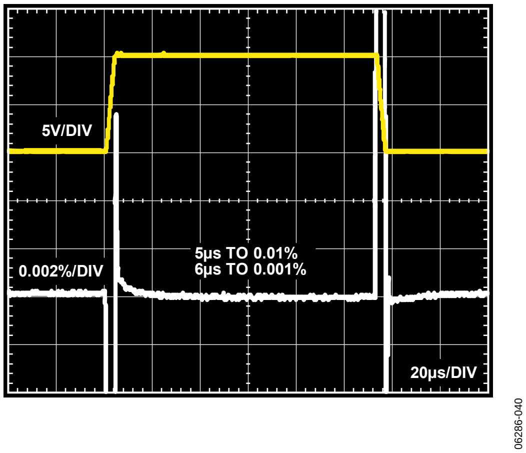


Figure 40. Large Signal Pulse Response and Settle Time, G = 1, R_L = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

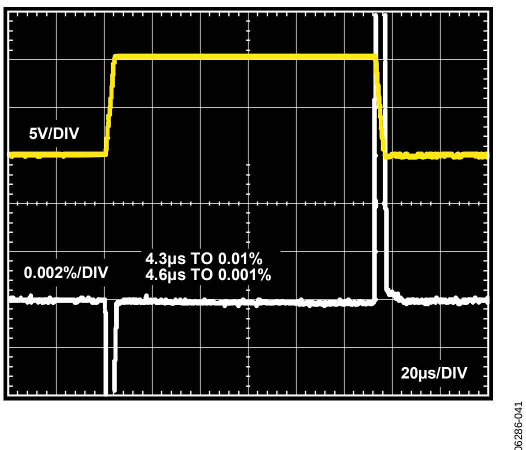


Figure 41. Large Signal Pulse Response and Settle Time, G = 10, R_L = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

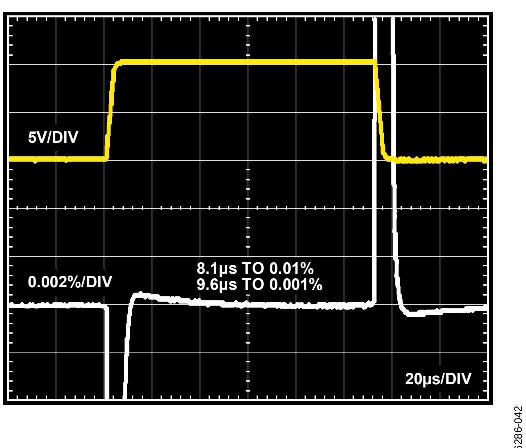


Figure 42. Large Signal Pulse Response and Settle Time, G = 100, R_L = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

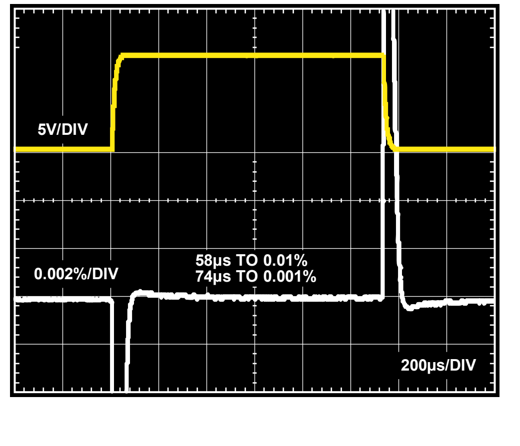


Figure 43. Large Signal Pulse Response and Settle Time, G = 1000, R_L = 10 kΩ, V_S = ±15 V, V_{REF} = 0 V

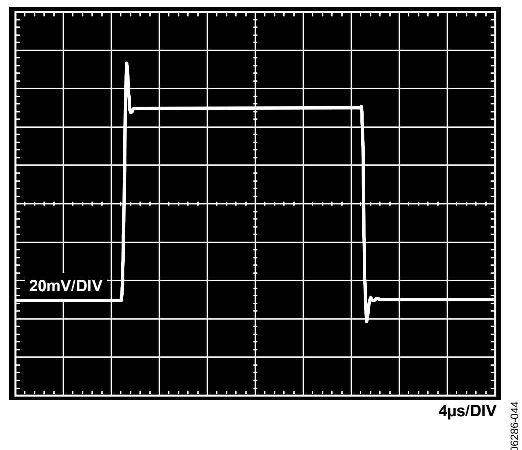


Figure 44. Small Signal Pulse Response, G = 1, R_L = 2 kΩ, CL = 100 pF, V_S = ±15 V, V_{REF} = 0 V

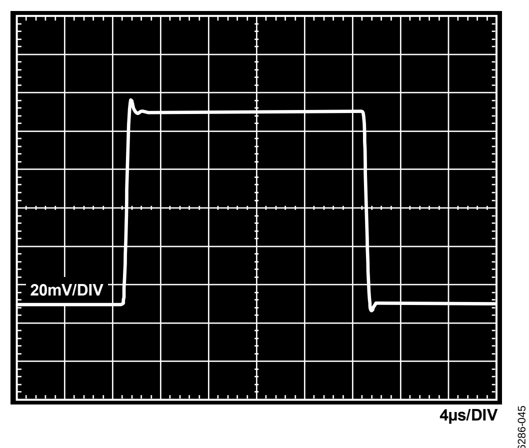


Figure 45. Small Signal Pulse Response, G = 10, R_L = 2 kΩ, CL = 100 pF, V_S = ±15 V, V_{REF} = 0 V.

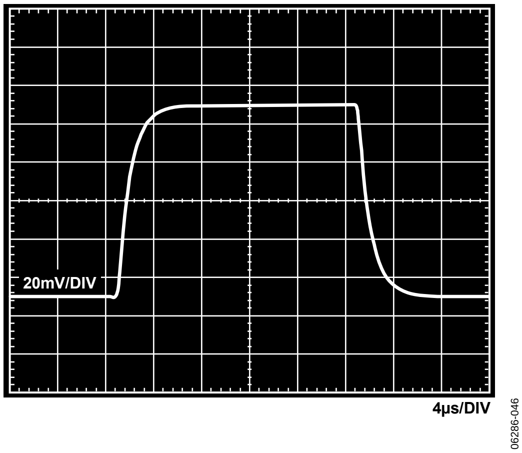


Figure 46. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C L= 100 pF, V_S = ±15 V, V_{REF} =0 V

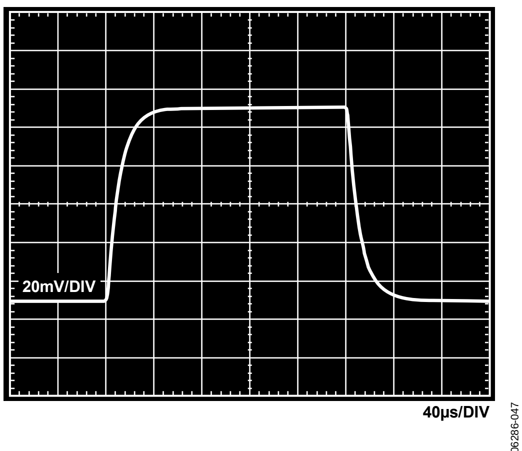


Figure 47. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, CL = 100 pF, V_S = ±15 V, V_{REF} = 0 V

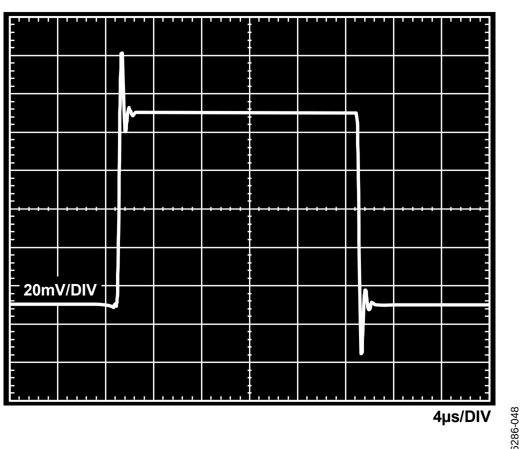


Figure 48. Small Signal Pulse Response, G = 1, R_L = 2 kΩ, CL = 100 pF, V_S = +5 V, V_{REF} = 2.5 V

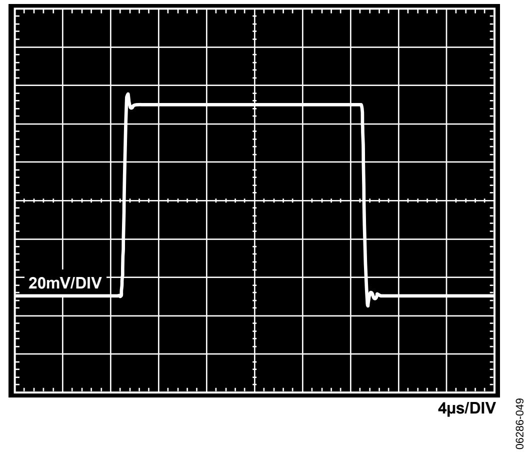


Figure 49. Small Signal Pulse Response, G = 10, R_L = 2 kΩ, CL = 100 pF, V_S = +5 V, V_{REF} = 2.5 V

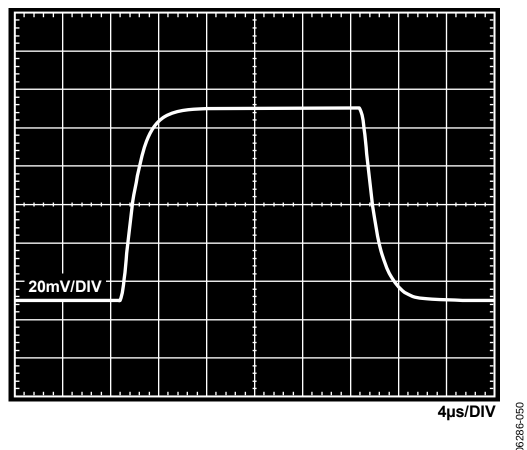


Figure 50. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, CL = 100 pF, V_S = +5 V, V_{REF} = 2.5 V

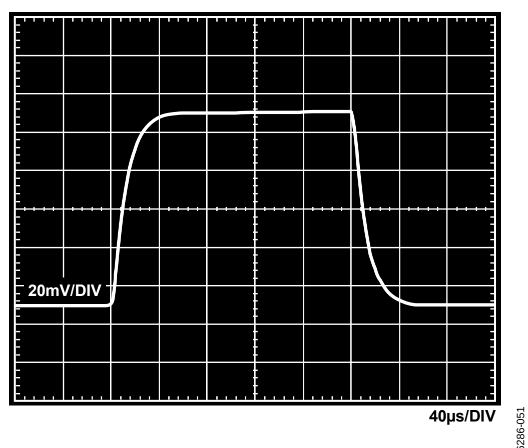


Figure 51. Small Signal Pulse Response, G = 1000,R_L = 2 kΩ, CL = 100 pF, V_S = +5 V, V_{REF} = 2.5 V

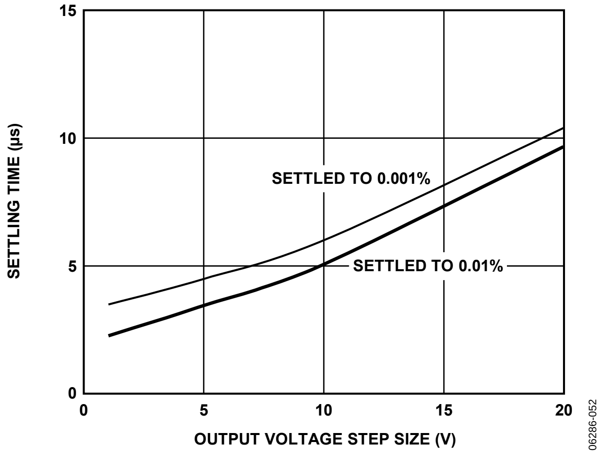


Figure 52. Settling Time vs. Step Size (G = 1) ±15 V, V_{REF} = 0 V

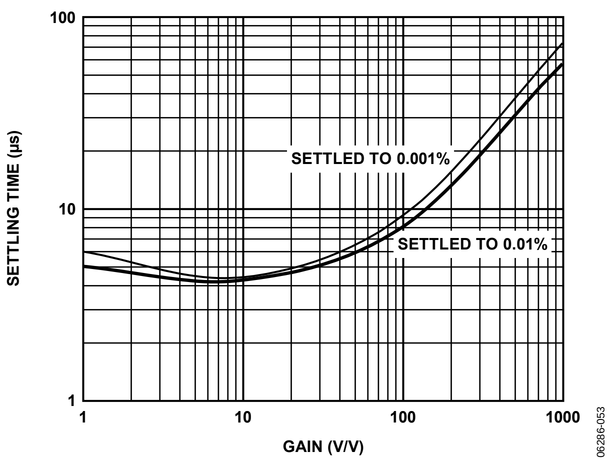


Figure 53. Settling Time vs. Gain for a 10 V Step, V_S = ±15 V, V_{REF} = 0 V

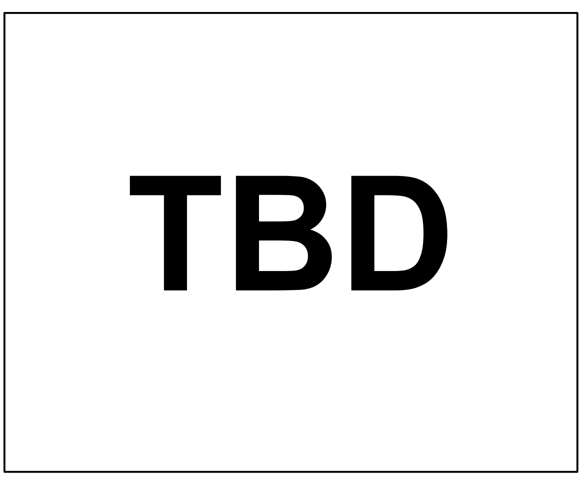


Figure 54 Channel Separation vs. Frequency, R_L = 2 kΩ, Source Channel at G = 1

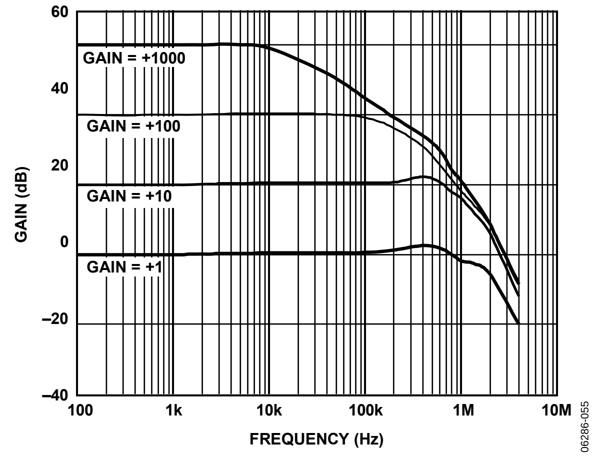


Figure 55. Differential Output Configuration: Gain vs. Frequency

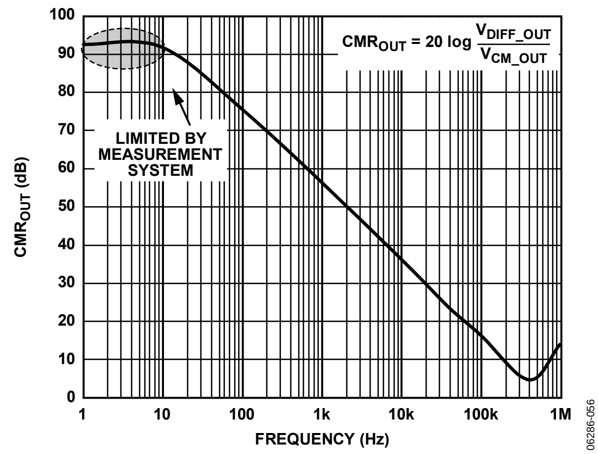


Figure 56. Differential Output Configuration: Common-Mode Output vs. Frequency

THEORY OF OPERATION

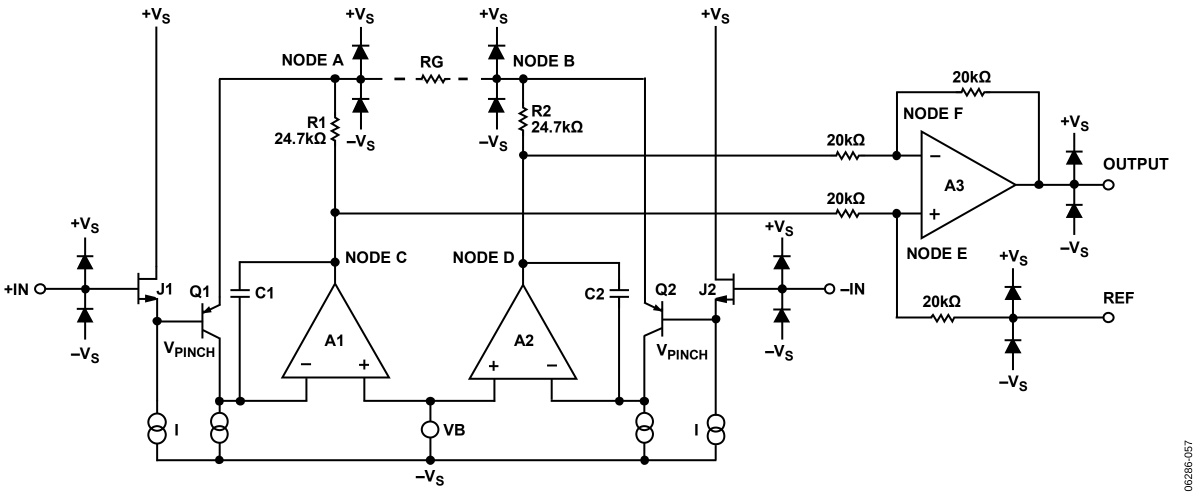


Figure 57. Simplified Schematic

The AD8224 is a JFET input, monolithic instrumentation amplifier based on the classic three op amp topology (see Figure 57). Input Transistor J1 and Input Transistor J2 are biased at a fixed current so that any input signal forces the output voltages of A1 and A2 to change accordingly. The input signal creates a current through RG that flows in R1 and R2 such that the outputs of A1 and A2 provide the correct, gained signal. Topologically, J1, A1, R1 and J2, A2, R2 can be viewed as precision current feedback amplifiers with a gain bandwidth of 1.5 MHz. The common-mode voltage and amplified differential signal from A1 and A2 are applied to a difference amplifier that rejects the common-mode voltage but amplifies the differential signal. The difference amplifier employs 20 kΩ laser trimmed resistors that result in an in-amp with gain error less than 0.04%. New trim techniques were developed to ensure that CMRR exceeds 86 dB (G = 1).

Using JFET transistors, the AD8224 offers extremely high input impedance, extremely low bias currents of 10 pA maximum, low offset current of 0.6 pA maximum, and no input bias current noise. In addition, input offset is less than 125 μV and drift is less than 5 μV/°C. Ease of use and robustness were considered. A common problem for instrumentation amplifiers is that at high gains, when the input is overdriven, an excessive milliampere input bias current can result and the output can undergo phase reversal. Overdriving the input at high gains refers to when the input signal is within the supply voltages but the amplifier cannot output the gained signal. For example, at a gain of 100, driving the amplifier with 10 V on ±15 V constitutes overdriving the inputs since the amplifier cannot output 100 V.

The AD8224 has none of these problems; its input bias current is limited to less than 10 μA and the output does not phase reverse under overdrive fault conditions.

The AD8224 has extremely low load induced nonlinearity. All amplifiers that comprise the AD8224 have rail-to-rail output capability for enhanced dynamic range. The input of the AD8224 can amplify signals with wide common-mode voltages even slightly lower than the negative supply rail. The AD8224 operates over a wide supply voltage range. It can operate from either a single +4.5 V to +36 V supply or a dual ±2.25 V to ±18 V. The transfer function of the AD8224 is

$$G = 1 + \frac{49.4\ k\Omega}{RG}$$

Users can easily and accurately set the gain using a single, standard resistor. Since the input amplifiers employ a current feedback architecture, the AD8224 gain bandwidth product increases with gain, resulting in a system that does not experience as much bandwidth loss as voltage feedback architectures at higher gains.

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8224. This is calculated by referring to Table 11 or by using the following gain equation.

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Table 11. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

The AD8224 defaults to G = 1 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the AD8224's specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are kept to a minimum.

REFERENCE TERMINAL

The output voltage of the AD8224 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF1 or REF2 pin to level-shift the output so that the AD8224 can drive a single-supply ADC. Pin REFx is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, source impedance to the REF terminal should be kept below 1 Ω. As shown in Figure 57 the reference terminal, REF, is at one end of a 20 kΩ resistor. Additional impedance at the REF terminal adds to this 20 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be computed by

$$\frac{2\left(20\ \text{k}\Omega + R_{REF}\right)}{40\ \text{k}\Omega + R_{REF}}$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades the amplifier's CMRR.

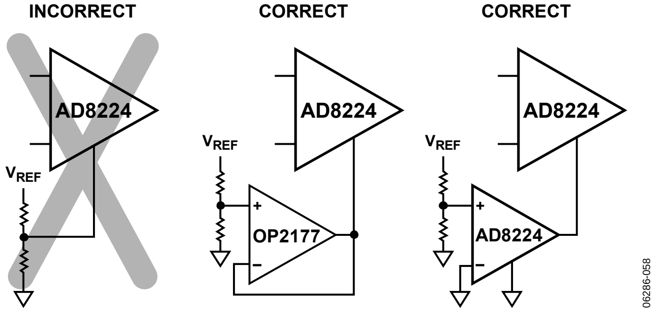


Figure 58. Driving the Reference Pin

LAYOUT

The AD8224 is a high precision device. To ensure optimum performance at the PC board level, care must be taken in the design of the board layout. The AD8224 pinout is arranged in a logical manner to aid in this task.

Package Considerations

The AD8224 is available in a 16-lead, 4 mm × 4 mm LFCSP. Blindly copying the footprint from another 4 mm × 4 mm LFCSP part is not recommended; it may not have the same thermal pad size and leads. Refer to the Outline Dimensions section to verify that the PCB symbol has the correct dimensions. Space between the leads and thermal pad should be kept as wide as possible for the best bias current performance.

Thermal Pad

The AD8224's 4 mm × 4 mm LFCSP comes with a thermal pad. This pad is connected internally to $+V_S$. The pad can either be left unconnected or connected to the positive supply rail.

To preserve maximum pin compatibility with future dual instrumentation amplifiers, leave the pad unconnected. This can be done by not soldering the paddle at all or by soldering the part to a landing that is a not connected to any other net. For high vibration applications, a landing is recommended.

Because the AD8224 dissipates little power, heat dissipation is rarely an issue. If improved heat dissipation is desired (for example, when driving heavy loads), connect the thermal pad to the positive supply rail. For the best heat dissipation performance, the positive supply rail should be a plane in the board. See the section for thermal coefficients with and without the pad soldered.

Common-Mode Rejection over Frequency

The AD8224 has a higher CMRR over frequency than typical in-amps, which gives it greater immunity to disturbances, such as line noise and its associated harmonics. A well-implemented layout is required to maintain this high performance. Input source impedances should be matched closely. Source resistance should be placed close to the inputs so that it interacts with as little parasitic capacitance as possible.

Parasitics at the RGx pins can also affect CMRR over frequency. The PCB should be laid out so that the parasitic capacitances at each pin match. Traces from the gain setting resistor to the RGx pins should be kept short to minimize parasitic inductance.

Reference

Errors introduced at the reference terminal feed directly to the output. Take care to tie the REFx pins to the appropriate local ground.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

The AD8224 has two positive supply pins (Pin 5 and Pin 16) and two negative supply pins (Pin 8 and Pin 13). While the part functions with only one pin from each supply pair connected, both pins should be connected for specified performance and optimum reliability.

The AD8224 should be decoupled with 0.1 µF bypass capacitors, one for each supply. The positive supply decoupling capacitor should be placed near Pin 16, and the negative supply decoupling capacitor should be placed near Pin 8. Each supply should also be decoupled with a 10 µF tantalum capacitor. The tantalum capacitor can be placed further away from the AD8224 and can generally be shared by other precision integrated circuits. Figure 59 shows an example layout.

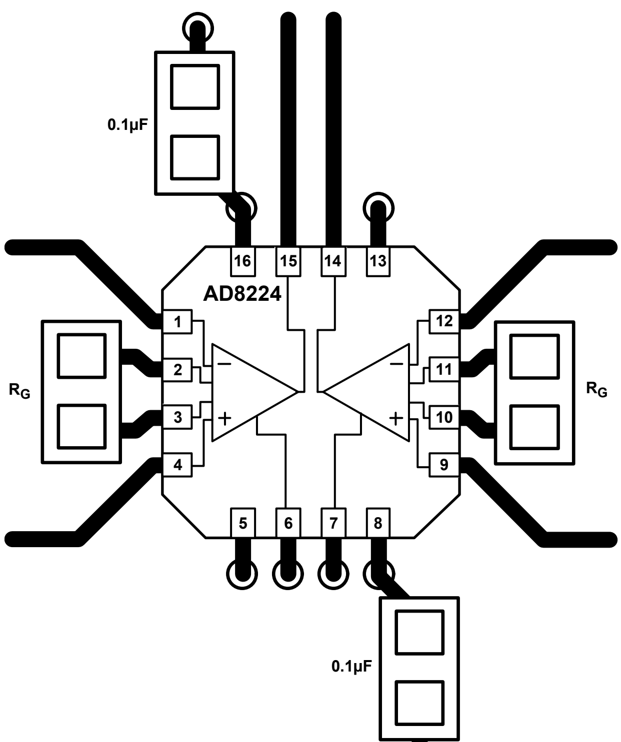


Figure 59. Example Layout

SOLDER WASH

The solder process can leave flux and other contaminants on the board. When these contaminants are between the AD8224 leads and thermal pad, they can create leakage paths that are larger than the AD8224's bias currents. A thorough washing process removes these contaminants and restores the device's excellent bias current performance.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8224 must have a return path to common. When the source, such as a transformer, cannot provide a return current path, one should be created, as shown in Figure 60.

INPUT PROTECTION

All terminals of the AD8224 are protected against ESD. ESD protection is guaranteed to 4 kV (human body model).In addition, the input structure allows for dc overload conditions a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, an external resistor should be used in series with each of the inputs to limit current for voltages above +Vs. In either scenario, the AD8224 safely handles a continuous 6 mA current at room temperature.

For applications where the AD8224 encounters extreme overload voltages, as in cardiac defibrillators, external series resistors and low leakage diode clamps, such as BAV199L, FJH1100, or SP720, should be used.

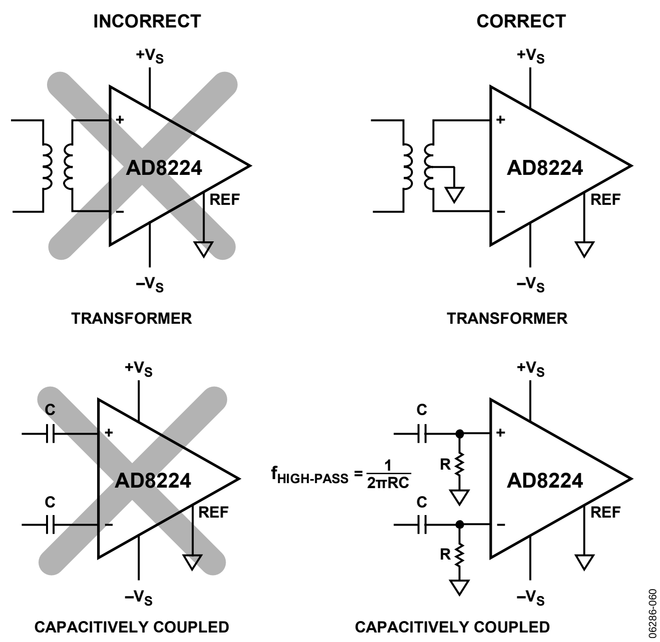


Figure 60. Creating an I_{BIAS} Path

RF INTERFERENCE

RF rectification is often a problem in applications where there are large RF signals. The problem appears as a small dc offset voltage. The AD8224 by its nature has a 5 pF gate capacitance (C_G) at its inputs. Matched series resistors form a natural low-pass filter that reduces rectification at high frequency (see Figure 61). The relationship between external, matched series resistors and the internal gate capacitance is expressed as follows:

$$FilterFreq_{DIFF} = \frac{1}{2\pi RC_G}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_G}$$

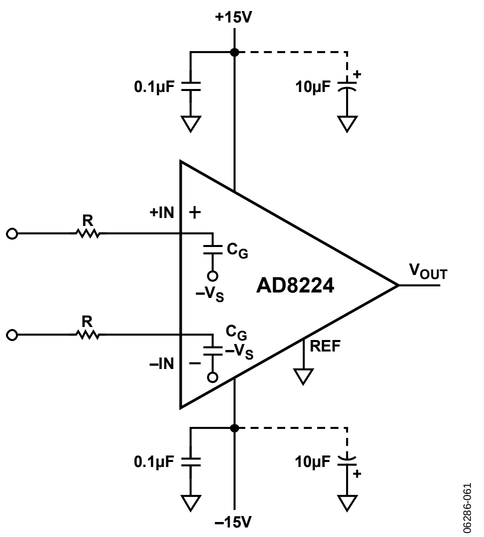


Figure 61. RFI Filtering Without External Capacitors

To eliminate high frequency common-mode signals while using smaller source resistors, a low-pass R-C network can be placed at the input of the instrumentation amplifier (see Figure 62). The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C + C_G)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi R(C_C + C_G)}$$

Mismatched C_C capacitors result in mismatched low-pass filters. The imbalance causes the AD8224 to treat what would have been a common-mode signal as a differential signal. To reduce the effect of mismatched external C_C capacitors, select a value of C_D greater than 10 times C_C. This sets the differential filter frequency lower than the common-mode frequency.

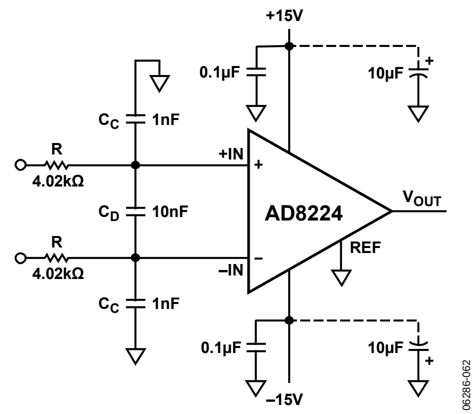


Figure 62. RFI Suppression

COMMON-MODE INPUT VOLTAGE RANGE

The three op amp architecture of the AD8224 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8224 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. Figure 26, Figure 27, Figure 28, and Figure 29 show the allowable common-mode input voltage ranges for various output voltages, supply voltages, and gains.

APPLICATIONS

DRIVING AN ANALOG-TO-DIGITAL CONVERTER

An instrumentation amplifier is often used in front of an analog-to-digital converter to provide CMRR and additional conditioning such as a voltage level shift and gain (see Figure 63). In this example, a 2.7 nF capacitor and a 500 Ω resistor create an anti-aliasing filter for the AD7685. The 2.7 nF capacitor also serves to store and deliver necessary charge to the switched capacitor input of the ADC. The 500 Ω series resistor reduces the burden of the 2.7 nF load from the amplifier. However, large source impedance in front of the ADC can degrade total harmonic distortion (THD).

For applications where THD performance is critical, the series resistor needs to be small. At worst, a small series resistor can load the AD8224, potentially causing the output to overshoot or ring. In such cases, a buffer amplifier, such as the AD8615, should be used after the AD8224 to drive the ADC.

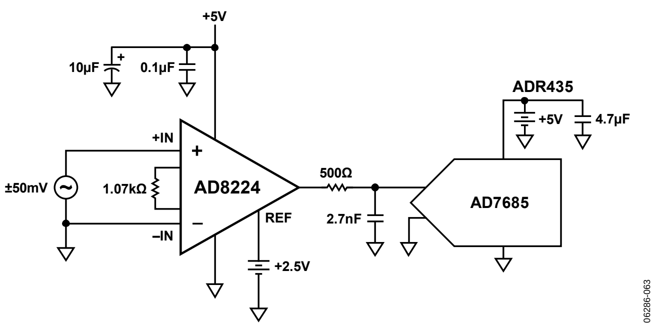


Figure 63. Driving an ADC in a Low Frequency Application

DIFFERENTIAL OUTPUT

The differential configuration of the AD8224 has the same excellent dc precision specifications as the single-ended output configuration and is recommended for applications in the frequency range of dc to 100 kHz.

The circuit configuration, outlined in Table 7, refers to the configuration shown in Figure 64 only. The circuit includes an RC filter that maintains the stability of the loop.

The transfer function for the differential output is:

$$V_{DIFF\_OUT} = V_{+OUT} - V_{-OUT} = (V_{+IN} - V_{-IN}) \times G$$

where:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

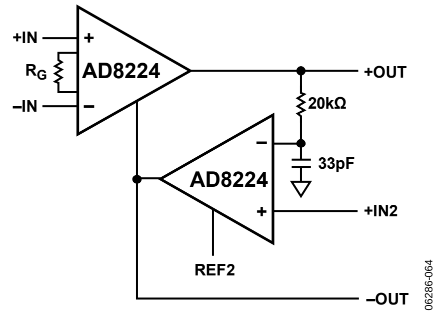


Figure 64. Differential Circuit Schematic

Setting the Common-Mode Voltage

The output common-mode voltage is set by the average of +IN2 and REF2. The transfer function is

$$V_{CM\_OUT} = (V_{+OUT} + V_{-OUT})/2 = (V_{+IN2} + V_{REF2})/2$$

+IN2 and REF2 have different properties that allow the reference voltage to be easily set for a wide variety of applications. +IN2 has high impedance but cannot swing to the supply rails of the part. REF2 must be driven with a low impedance, but can go 300 mV beyond the supply rails.

A common application sets the common-mode output voltage to the midscale of a differential ADC. In this case, the ADC reference voltage is sent to the +IN2 terminal, and ground is connected to the REF2 terminal. This produces a common-mode output voltage of half the ADC reference voltage.

2-Channel Differential Output Using a Dual Op Amp

Another differential output topology is shown in Figure 65. Instead of a second in-amp, ½ of a dual OP2177 op amp creates the inverted output. Because the OP2177 comes in an MSOP, this configuration allows the creation of a dual channel, precision differential output in-amp with little board area.

Errors from the op amp are common to both outputs and are thus common mode. Errors from mismatched resistors also create a common-mode dc offset. Because these errors are common mode, they are likely to be rejected by the next device in the signal chain.

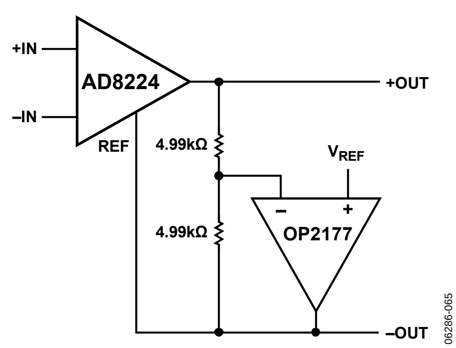


Figure 65. Differential Output Using Op Amp

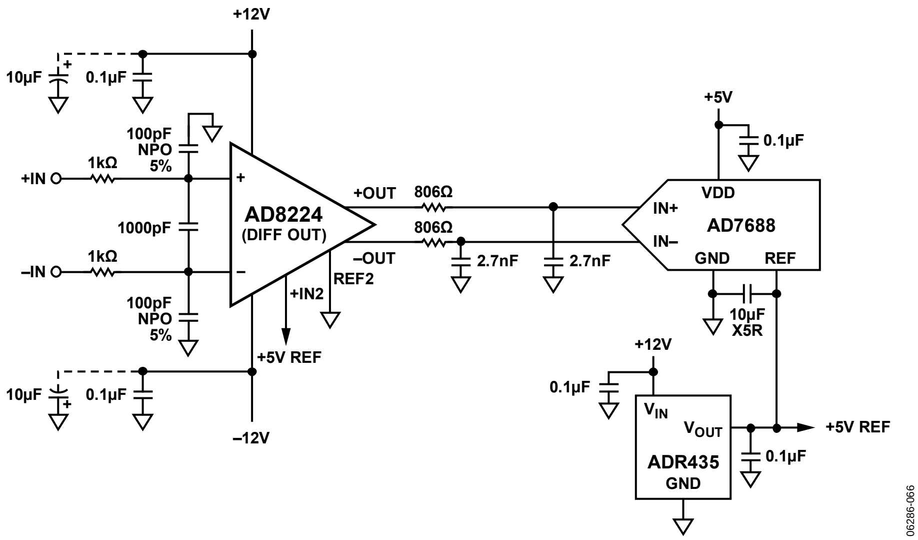


Figure 66. Driving a Differential ADC

DRIVING A DIFFERENTIAL INPUT ADC

The AD8224 can be configured in differential output mode to drive a differential analog-to-digital converter. Figure 66 illustrates several of the concepts.

First Antialiasing Filter

The 1 kΩ resistor, 1000 pF capacitor, and 100 pF capacitors in front of the in-amp form a 76 kHz filter. This is the first of two antialiasing filters in the circuit and helps to reduce the noise of the system. The 100 pF capacitors protect against common-mode RFI signals. Note that they are 5% COG/NPO types. These capacitors match well over time and temperature, which keeps the system's CMRR high over frequency.

Second Antialiasing Filter

An 806 Ω resistor and 2.7 nF capacitor are located between each AD8224 output and ADC input. They create a 73 kHz low-pass filter for another stage of antialiasing protection.

These four elements also isolate the ADC from loading the AD8224. The 806 Ω resistor shields the AD8224 from the ADC's switched capacitor input which looks like a time varying load. The 2.7 nF capacitor provides charge to the switched capacitor front end of the ADC. If the application requires a lower frequency antialiasing filter, increase the value of the capacitor rather than the resistor.

The 1 kΩ resistors can also protect an ADC from overvoltages. Because the AD8224 runs on wider supply voltages than a typical ADC, there is a possibility of overdriving the ADC. This is not an issue with a PulSAR® converter, such as the AD7688. Its input can handle a 130 mA overdrive, which is much higher than the short-circuit limit of the AD8224. However, other converters have less robust inputs and may need the added protection.

Reference

The ADR435 supplies a reference voltage to both the ADC and the AD8224. Because REF2 on the AD8224 is grounded, the common-mode output voltage is precisely half the reference voltage, exactly where it needs to be for the ADC.

DRIVING CABLING

All cables have a certain capacitance per unit length, which varies widely with cable type. The capacitive load from the cable may cause peaking in the AD8224 output response. To reduce peaking, use a resistor between the AD8224 and the cable. Because cable capacitance and desired output response vary widely, this resistor is best determined empirically. A good starting point is 50 Ω.

The AD8224 operates at a low enough frequency that transmission line effects are rarely an issue; therefore, the resistor need not match the characteristic impedance of the cable.

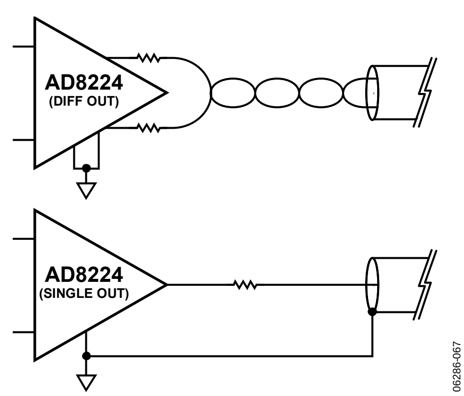


Figure 67. Driving a Cable

OUTLINE DIMENSIONS

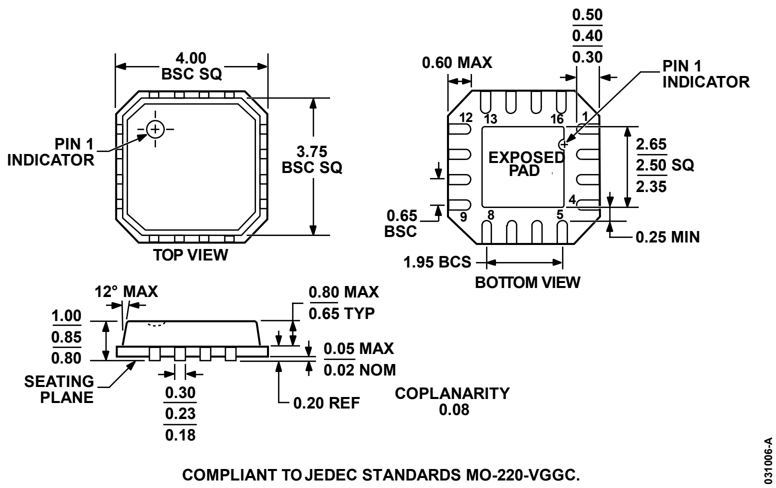


Figure 68. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-13)
Dimensions are shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Product Description	Package Option
AD8224ACPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-13
AD8224ACPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-13
AD8224ACPZ-WP[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-13
AD8224BCPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-13
AD8224BCPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-13
AD8224BCPZ-WP[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-13
AD8224-EVALZ		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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