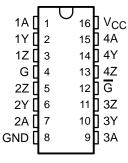
- Meets Standard EIA-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Supports Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of –7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)

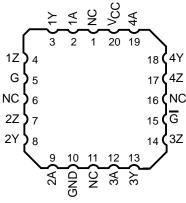
#### description

The SN55LBC172 is a monolithic quadruple differential line driver with 3-state outputs. This device is designed to meet the requirements of the Electronics Industry Association (EIA) standard RS-485. The SN55LBC172 is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry, making it suitable for party-line applications in noisy environments. The device is designed using the LinBiCMOS™ process, facilitating ultralow power consumption and inherent robustness.

#### J OR W PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN55LBC172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. This device offers optimum performance when used with the SN55LBC173M quadruple line receiver.

#### ORDERING INFORMATION<sup>‡</sup>

TA	PACKAGE <sup>§</sup>		PACKAGE§		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	LCCC – FK	Tube	SNJ55LBC172FK	SNJ55LBC172FK		
–55°C to 125°C	CDIP – J	Tube	SNJ55LBC172J	SNJ55LBC172J		
	CFP – W	Tube	SNJ55LBC172W	SNJ55LBC172W		

<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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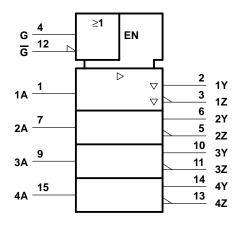
# FUNCTION TABLE (each driver)

INPUT	ENA	BLES	OUTI	PUTS
Α	G	G	Y	Z
Н	Н	Х	Н	L
L	Н	X	L	Н
Н	Х	L	Н	L
L	Х	L	L	Н
Х	L	Н	Z	Z

H = high level, L = low level, X = irrelevant,

Z = high impedance (off)

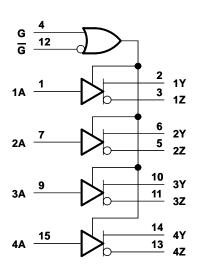
# logic symbol†



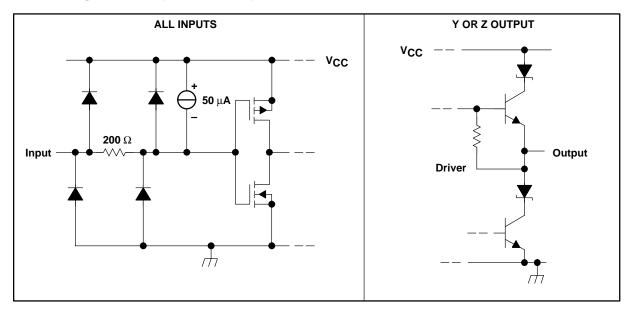
<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J or W package.

## logic diagram (positive logic)



## schematic diagrams of inputs and outputs



## **SN55LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER**

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> (see Note 1)	0.3 V to 7 V
Output voltage range, VO	
Input voltage range, V <sub>I</sub>	0.3 V to 7 V
Continuous power dissipation	
Operating free-air temperature range, T <sub>A</sub>	–55°C to 125°C
Storage temperature range, T <sub>stq</sub>	
Lead temperature 1.6 mm (1/16 inch) from case for	or 10 seconds ——65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE** 

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> =125°C	T <sub>A</sub> = 125°C POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

#### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>				5.25	V
High-level input voltage, V <sub>IH</sub>		2			V
Low-level input voltage, V <sub>IL</sub>				0.8	V
Output valtage at any bus terminal (constraint or common mode) \/a	Y or Z			12	V
Output voltage at any bus terminal (separately or common mode), VO	1 01 2			-7	ľ
High-level output current, IOH	Y or Z			-60	mA
Low-level output current, I <sub>OL</sub>	Y or Z			60	mA
Continuous total power dissipation			Dissipatio	on Rating	g Table
Operating free-air temperature, T <sub>A</sub>				125	°C



<sup>‡</sup> The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature. NOTE 1: All voltage values are with respect to GND.

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# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST	MIN	TYP <sup>†</sup>	MAX	UNIT	
VIK	Input clamp voltage	$I_{I} = -18 \text{ mA}$				-1.5	V
IV.			See Figure 1	1.1	1.8	5	٧
IVODI	Differential output voltage‡	$R_L = 60 \Omega$ ,	See Figure 2	1.1	1.7	5	V
$\Delta  VOD $	Change in magnitude of differential output voltage§					±0.2	V
Voc	Common-mode output voltage	$R_L = 54 \Omega$ , See Figure 1				3 -1	٧
ΔIVOCI	Change in magnitude of common-mode output voltage§					±0.2	V
IO	Output current with power off	$V_{CC} = 0$ ,	$V_0 = -7 \text{ V to } 12 \text{ V}$			±100	μΑ
loz	OZ High-impedance-state output current		$V_0 = -7 \text{ V to } 12 \text{ V}$			±100	μΑ
lн	High-level input current	V <sub>I</sub> = 2.4 V				-100	μΑ
IլL	Low-level input current	V <sub>I</sub> = 0.4 V				-100	μΑ
los	Short-circuit output current	$V_0 = -7 V tc$	12 V			±250	mA
loo	Supply current (all drivers)	No load	Outputs enabled			7	mA
ICC	Supply current (an univers)	INU IUdu	Outputs disabled			1.5	IIIA

 $<sup>\</sup>uparrow$  All typical values are at  $V_{CC} = 5$  V and  $T_A = 25$ °C.

# switching characteristics, $V_{CC} = 5 \text{ V}$

	PARAMETER	TEST CONDITIONS		TA	MIN	TYP	MAX	UNIT
t work	Differential output delay time	$R_1 = 54 \Omega$	See Figure 3	25°C	2	11	20	ns
td(OD)	Differential output delay time	KL = 54 52,	See Figure 3	−55°C to 125°C	2		40	115
t. (0.7)	Differential output transition time	$R_1 = 54 \Omega$	D 540 Caa Figure 2		10	15	25	ns
t <sub>t</sub> (OD)	Differential output transition time	N_ = 54 52,	See Figure 3	−55°C to 125°C	4		60	115
t	Output anable time to high lovel		See Figure 4	25°C			30	20
<sup>t</sup> PZH	Output enable time to high level	$R_L = 110 \Omega$ ,	See Figure 4	-55°C to 125°C			40	ns
t	Output anable time to law level	D: 440.0 Con Figure 5		25°C			30	ns
tPZL	Output enable time to low level $R_L = 110 \Omega$ , See Figu		See Figure 5	−55°C to 125°C			40	115
t	Output disable time from high level	$R_1 = 110 \Omega$	See Figure 4	25°C			60	ns
<sup>t</sup> PHZ	Output disable time nom night level	KL = 110 12, See Figure 4		−55°C to 125°C			115	115
to. 7	Output disable time from low level	$R_1 = 110 \Omega$	See Figure 5	25°C			30	ns
<sup>t</sup> PLZ	Output disable time nom low level	INL = 110 52,	See i igule 5	-55°C to 125°C			55	115

<sup>&</sup>lt;sup>‡</sup> The minimum V<sub>OD</sub> specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.

<sup>§ ∆|</sup>V<sub>OD</sub>| and ∆|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

#### PARAMETER MEASUREMENT INFORMATION

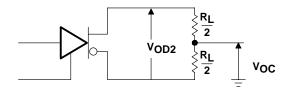


Figure 1. Differential and Common-Mode Output Voltages

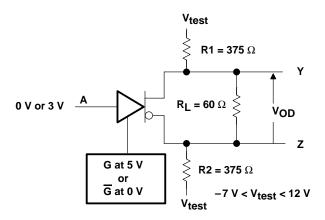
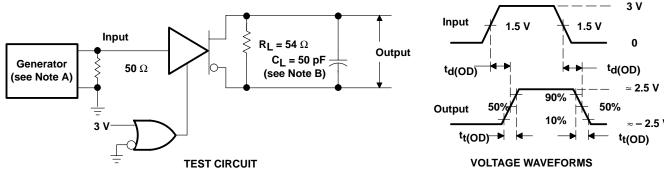


Figure 2. Driver V<sub>OD</sub> Test Circuit



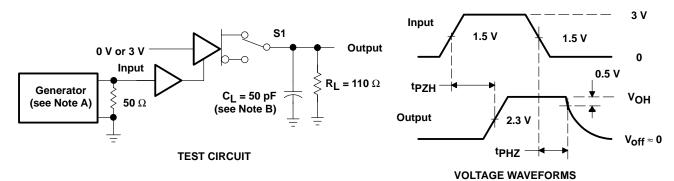
NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle  $\leq$  50%,  $t_f \leq$  5 ns,  $t_f \leq$  6 ns,  $t_f \leq$  7 ns,  $t_f \leq$  7 ns,  $t_f \leq$  7 ns,  $t_f \leq$  7 ns,  $t_f \leq$  8 ns,  $t_f \leq$  9 ns,

B. C<sub>L</sub> includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

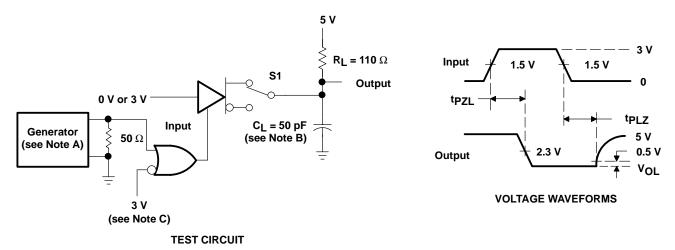


#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle  $\leq$  50%,  $t_{f} \leq$  5 ns,  $Z_{O} = 50 \ \Omega$ .
  - B. C<sub>L</sub> includes probe and stray capacitance.

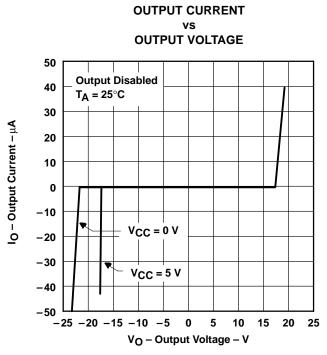
Figure 4. tpzH and tpHZ Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle  $\leq$  50%,  $t_f \leq$  5 ns,  $t_f \leq$  6 ns,  $t_f \leq$  7 ns,  $t_f \leq$  7 ns,  $t_f \leq$  7 ns,  $t_f \leq$  8 ns,  $t_f \leq$  9 ns,
  - B. C<sub>L</sub> includes probe and stray capacitance.
  - C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform to  $\overline{G}$ .

Figure 5. tpzL and tpLZ Test Circuit and Waveforms

#### **TYPICAL CHARACTERISTICS**



**LOW-LEVEL OUTPUT CURRENT** 5 V<sub>CC</sub> = 5 V 4.5 T<sub>A</sub> = 25°C VOL - Low-Level Output Voltage - V 4 3.5 3 2.5 2 1.5 1 0.5 0 -20 20 40 60 100 120 IOL - Low-Level Output Current - mA

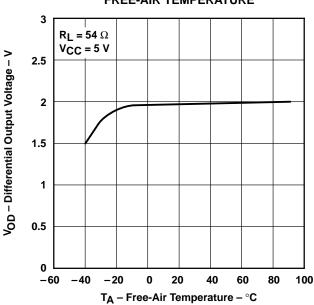
**LOW-LEVEL OUTPUT VOLTAGE** 

Figure 6

Figure 7

**HIGH-LEVEL OUTPUT VOLTAGE** 





VS
HIGH-LEVEL OUTPUT CURRENT

5
VCC = 5

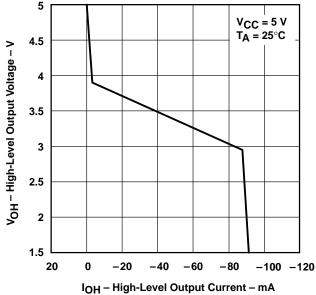


Figure 8

Figure 9



#### TYPICAL CHARACTERISTICS

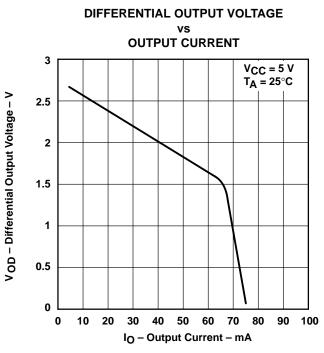


Figure 10

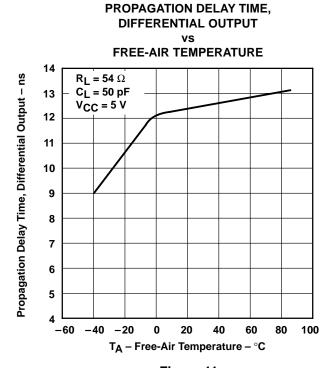


Figure 11

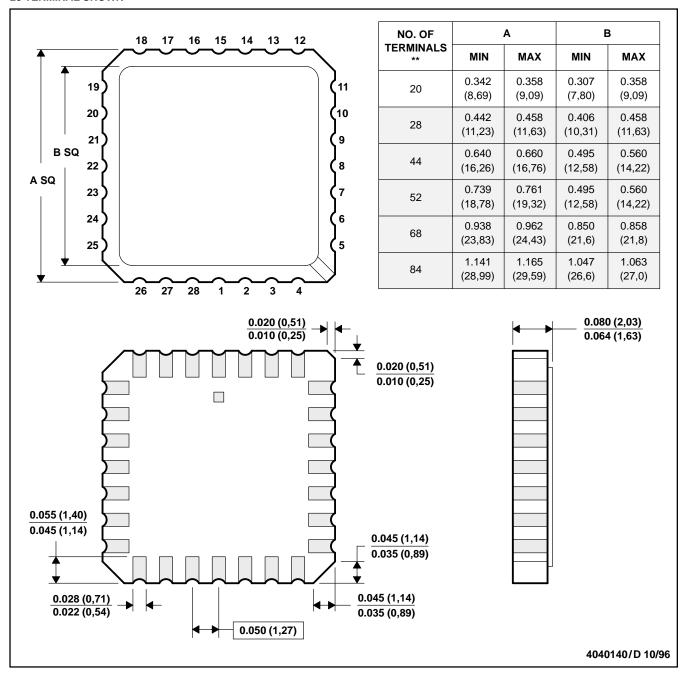
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#### **MECHANICAL DATA**

#### FK (S-CQCC-N\*\*)

#### 28 TERMINAL SHOWN

#### LEADLESS CERAMIC CHIP CARRIER



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004



#### **MECHANICAL DATA**

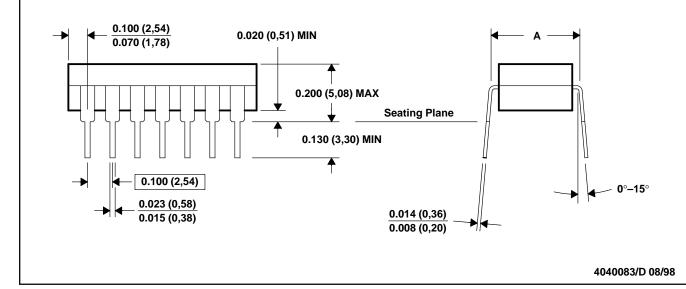
# J (R-GDIP-T\*\*) 14 PIN SHOWN

#### **CERAMIC DUAL-IN-LINE PACKAGE**

# 

0.045 (1,14)

PINS **	14	16	18	20
A MAX	0.310	0.310	0.310	0.310
	(7,87)	(7,87)	(7,87)	(7,87)
A MIN	0.290	0.290	0.290	0.290
	(7,37)	(7,37)	(7,37)	(7,37)
B MAX	0.785	0.785	0.910	0.975
	(19,94)	(19,94)	(23,10)	(24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	_	0.930 (23,62)
C MAX	0.300	0.300	0.300	0.300
	(7,62)	(7,62)	(7,62)	(7,62)
C MIN	0.245	0.245	0.245	0.245
	(6,22)	(6,22)	(6,22)	(6,22)



NOTES: A. All linear dimensions are in inches (millimeters).

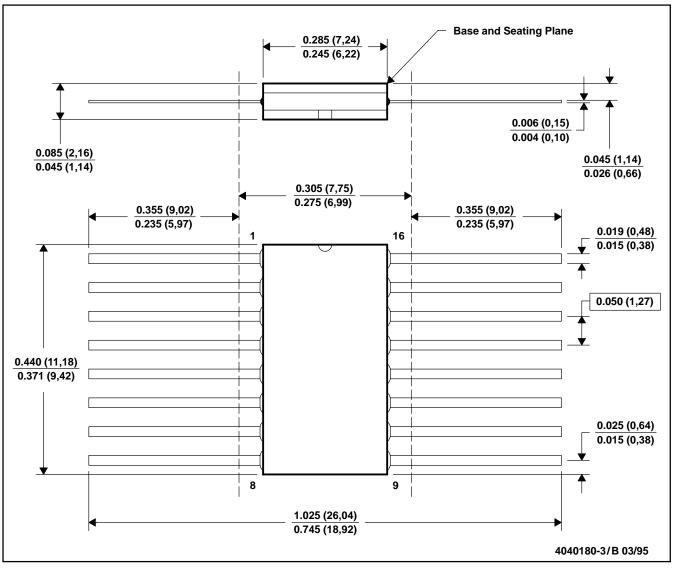
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

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#### **MECHANICAL DATA**

#### W (R-GDFP-F16)

#### **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC







.com 9-Oct-2007

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9076503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9076503QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9076503QFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55LBC172FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55LBC172J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55LBC172W	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### 14 LEADS SHOWN

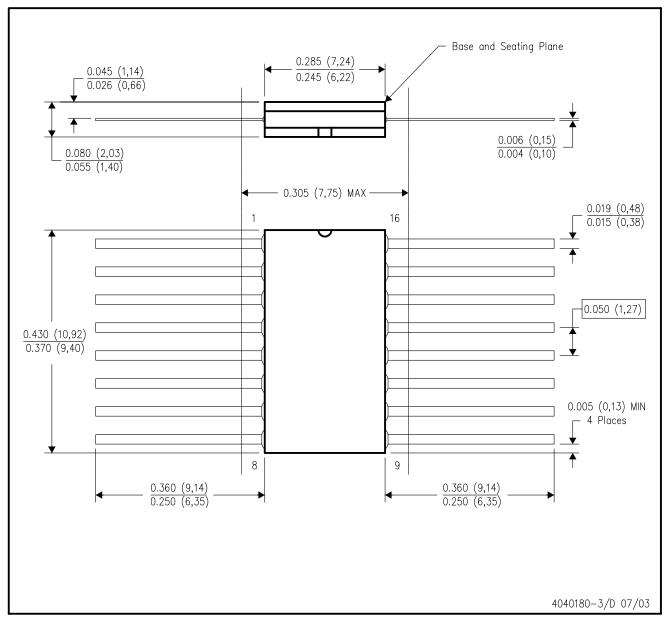


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F16)

# CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



#### FK (S-CQCC-N\*\*)

#### **28 TERMINAL SHOWN**

#### **LEADLESS CERAMIC CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



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logic.ti.com	Military	www.ti.com/military
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