- **Three Differential Transceivers in One Package**
- **Signaling Rates† Up to 30 Mbps**
- **Low Power and High Speed**
- **Designed for TIA/EIA-485, TIA/EIA-422, ISO 8482, and ANSI X3.277 (HVD SCSI Fast−20) Applications**
- **Common-Mode Bus Voltage Range –7 V to 12 V**
- **ESD Protection on Bus Terminals Exceeds 12 kV**
- **Driver Output Current up to ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Power-Up, Power-Down Glitch-Free Operation**
- **Pin-Compatible With the SN75ALS170**
- **Available in Shrink Small-Outline Package**

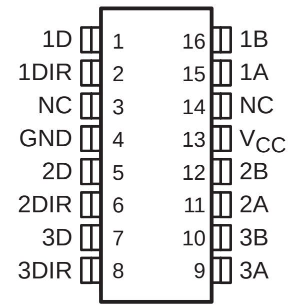
description

The SN65LBC170 and SN75LBC170 are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. Potential applications include serial or parallel data transmission, cabled peripheral buses with twin axial, ribbon, or twisted-pair cabling. These devices are suitable for FAST-20 SCSI and can transmit or receive data pulses as short as 25 ns, with skew less than 3 ns.

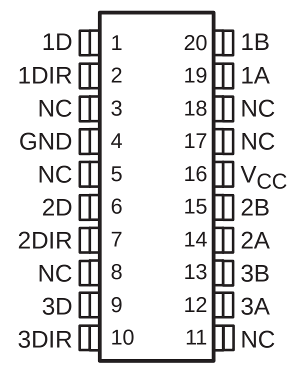
These devices combine three 3-state differential line drivers and three differential input line receivers, all of which operate from a single 5-V power supply.

The driver differential outputs and the receiver differential inputs are connected internally to form three differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature a wide common-mode voltage range making the device suitable for party-line applications over long cable runs.

SN65LBC170DB (marked as BL170)
SN75LBC170DB (marked as BL170)
(TOP VIEW)

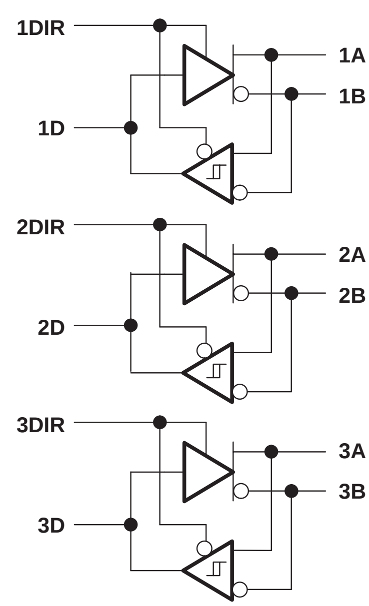


SN65LBC170DW (marked as 65LBC170)
SN75LBC170DW (marked as 75LBC170)
(TOP VIEW)



NC − No internal connection

logic diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

description (continued)

The driver's active-high enable and the receiver's active-low enable are tied together internally and provide a direction input for each driver/receiver pair.

The SN75LBC170 is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC170 is characterized for operation over the temperature range of −40°C to 85°C.

AVAILABLE OPTIONS†

T_A	PACKAGE	
	PLASTIC SHRINK SMALL-OUTLINE (JEDEC MO-150)	PLASTIC SMALL-OUTLINE (JEDEC MS-013)
0°C to 70°C	SN75LBC170DB	SN75LBC170DW
−40°C to 85°C	SN65LBC170DB	SN65LBC170DW

† Add R suffix for taped and reel

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Function Tables

EACH DRIVER

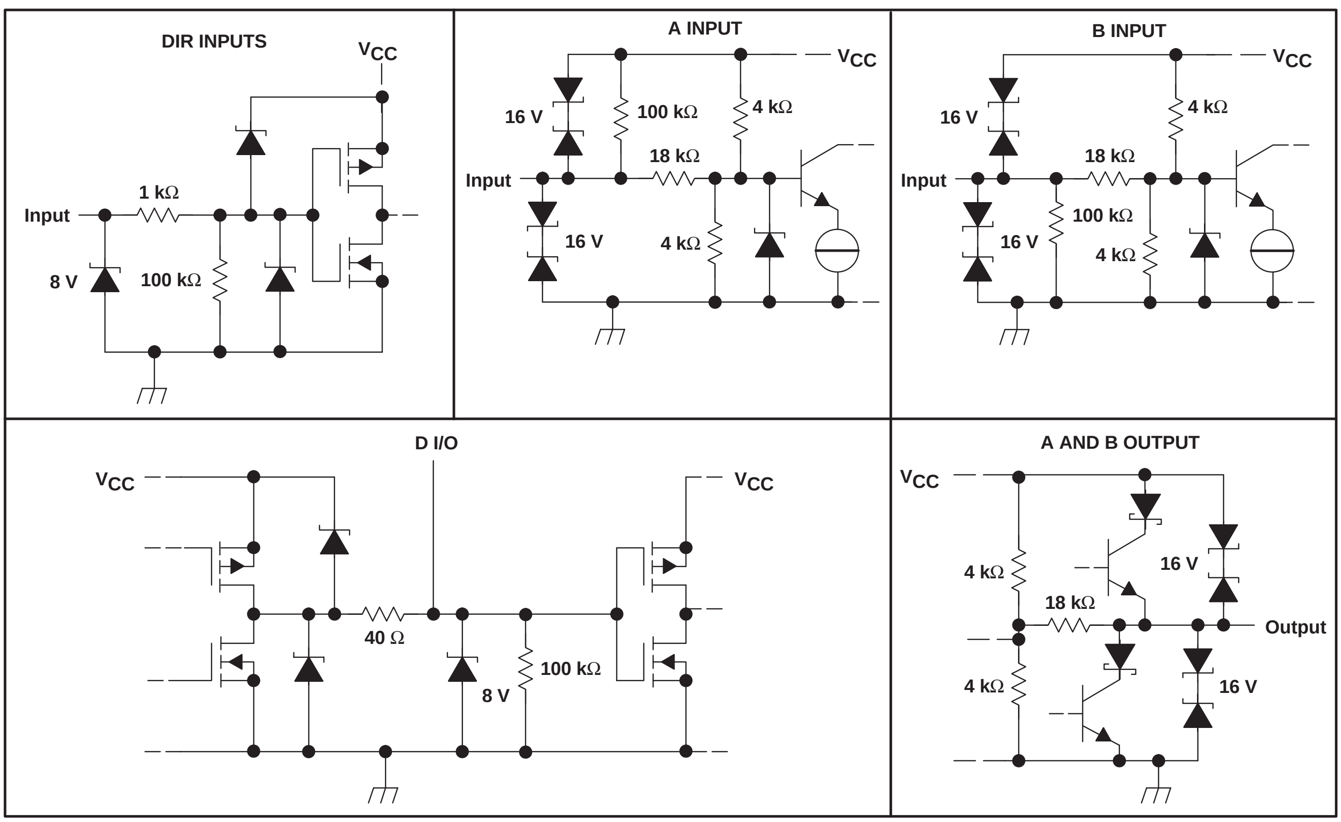
INPUT D	ENABLE DIR	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
OPEN	H	L	H
X	L	Z	Z
X	OPEN	X	X

EACH RECEIVER

DIFFERENTIAL INPUT ($V_A - V_B$)	ENABLE DIR	OUTPUT D
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
OPEN	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

equivalent input and output schematic diagrams



absolute maximum ratings† over operating free−air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . . −0.3 V to 6 V
Voltage range at any bus I/O terminal (steady state) . . . . . . −10 V to 15 V
Voltage input range, A and B, (transient pulse through 100 Ω, see Figure 12) . . . . . . −30 V to 30 V
Voltage range at any D or DIR terminal . . . . . . − 0.5 V to V_{CC} + 0.5 V
Receiver output current, I_O . . . . . . ±10 mA
Electrostatic discharge: Human body model (A, B, GND) (see Note 2) . . . . . . 12 kV
All pins . . . . . . 5 kV
Charged-device model (all pins) (see Note 3) . . . . . . 1 kV
Continuous total power dissipation . . . . . . See Power Dissipation Rating Table

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114−A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DB	995 mW	8.0 mW/°C	635 mW	515 mW
DW	1480 mW	11.8 mW/°C	950 mW	770 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal	A, B	−7		12	V
High-level input voltage, V_{IH}	D, DIR	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DIR	0		0.8	V
Differential input voltage, V_{ID}	A with respect to B	−12		12	V
Output current	Driver	−60		60	mA
Output current	Receiver	−8		8	mA
Operating free-air temperature, T_A	SN75LBC170	0		70	°C
Operating free-air temperature, T_A	SN65LBC170	−40		85	°C

DRIVER SECTION

electrical characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D and DIR	I_I = 18 mA		−1.5	−0.7		V
V_O	Open-circuit output voltage (single-ended)		A or B,	No load	0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude‡		No load		3.8	4.3	V_{CC}	V
			R_L = 54 Ω,	See Figure 1	1	1.6	2.4	
			With common-mode loading, See Figure 2		1	1.6	2.4	
ΔV_{OD}	Change in differential output voltage magnitude, $\| V_{OD(H)} \| - \|V_{OD(L)} \|$		R_L = 54 Ω, C_L = 50 pF	See Figure 1	−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				2	2.4	2.8	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage ($V_{OC(H)} - V_{OC(L)}$)				−0.2		0.2	V
I_I	Input current		D, DIR		−100		100	µA
I_O	Output current with power off		V_{CC} = 0 V,	V_O = −7 V to 12 V	−700		900	µA
I_{OS}	Short-circuit output current		V_O = −7 V to 12 V,	See Figure 7	−250		250	mA
I_{CC}	Supply current (driver enabled)		D at 0 V or V_{CC},	DIR at V_{CC}, No load		14	20	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Differential output propagation delay, low-to high	R_L = 54 Ω, C_L = 50 pF, See Figure 3	4	8.5	12	ns
t_{PHL}	Differential output propagation delay, high-to-low		4	8.5	11	
t_r	Differential output rise time		3	7.5	11	
t_f	Differential output fall time		3	7.5	11	
$t_{sk(p)}$	Pulse skew $\| (t_{PLH} - t_{PHL}) \|$				2	
$t_{sk(o)}$	Output skew§				1.5	
$t_{sk(pp)}$	Part-to-part skew¶				2	
t_{PLH}	Differential output propagation delay, low-to high	See Figure 4, (HVD SCSI double-terminated load)	3	7	10	ns
t_{PHL}	Differential output propagation delay, high-to-low		3	7.5	10	
t_r	Differential output rise time		3	7.5	12	
t_f	Differential output fall time		3	7.5	12	
$t_{sk(p)}$	Pulse skew $\| (t_{PLH} - t_{PHL}) \|$				3	
$t_{sk(o)}$	Output skew§				1.5	
$t_{sk(pp)}$	Part-to-part skew¶				2.5	
t_{PZH}	Output enable time to high level	See Figure 5		15	25	ns
t_{PHZ}	Output disable time from high level			18	25	
t_{PZL}	Output enable time to low level	See Figure 6		10	25	ns
t_{PLZ}	Output disable time from low level			17	25	

§ Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
¶ Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER SECTION

electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 8				0.2	V
V_{IT-}	Negative-going differential input voltage threshold			−0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				40		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −8 mA, See Figure 8		4	4.7	V_{CC}	V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = −8 mA, See Figure 8		0	0.2	0.4	
I_I	Line input current	Other input = 0 V	V_I = 12 V			0.9	mA
			V_I = −7 V	−0.7			
R_I	Input resistance	A, B		12			kΩ
I_{CC}	Supply current (receiver enabled)	A, B, D, and DIR open				16	mA

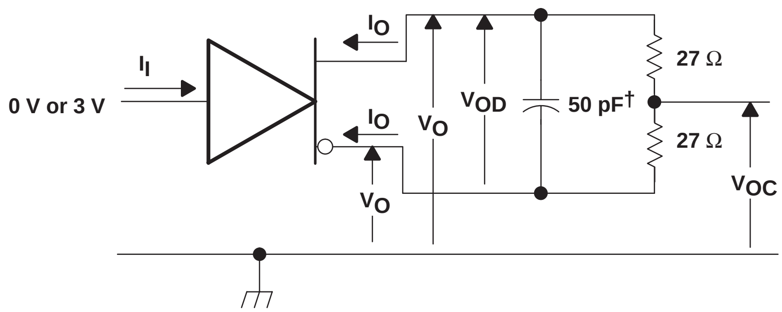
† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 9	7		16	ns
t_{PHL}	Propagation delay time, high-to-low level output		7		16	ns
t_r	Receiver output rise time			1.3	3	ns
t_f	Receiver output fall time			1.3	3	ns
t_{PZH}	Receiver output enable time to high level	See Figure 10		26	40	ns
t_{PHZ}	Receiver output disable time from high level				40	
t_{PZL}	Receiver output enable time to low level	See Figure 11		29	40	ns
t_{PLZ}	Receiver output enable time to high level				40	
$t_{sk(p)}$	Pulse skew (| $t_{PLH} - t_{PHL}$ |)				2	ns
$t_{sk(o)}$	Output skew‡				1.5	ns
$t_{sk(pp)}$	Part-to-part skew§				3	ns

‡ Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
§ Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION



† Includes probe and jig capacitance

Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

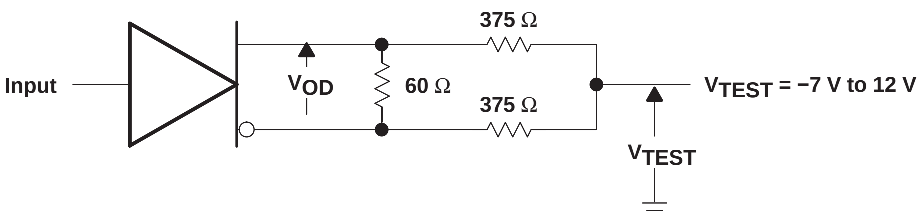
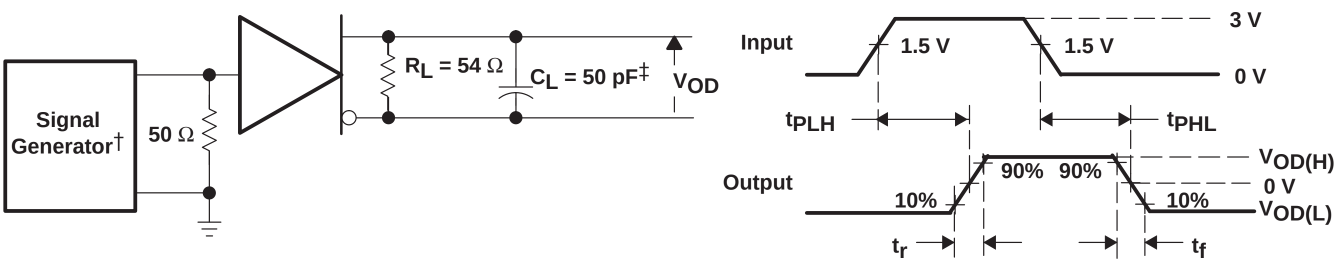


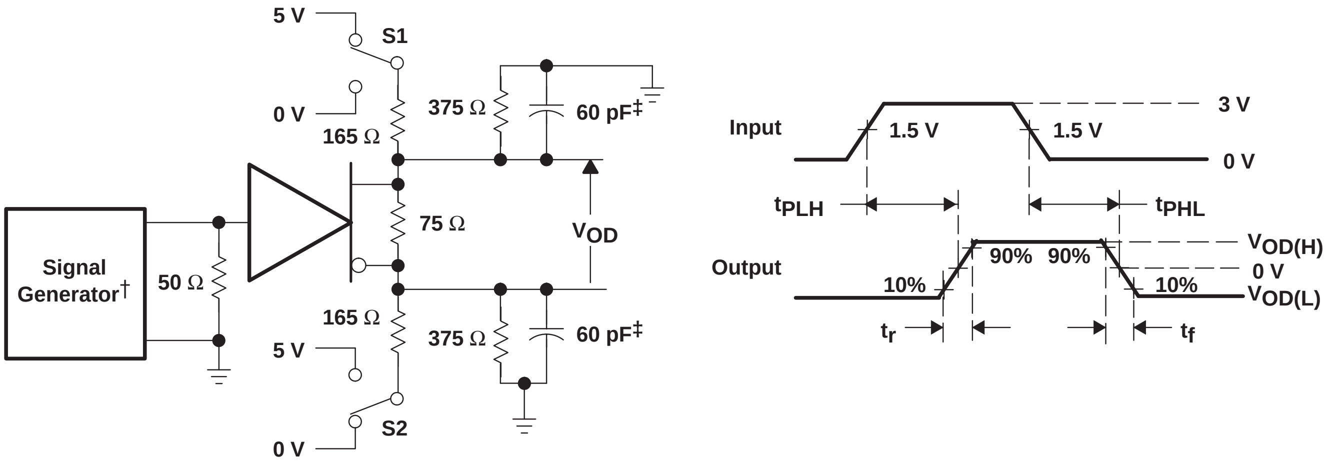
Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

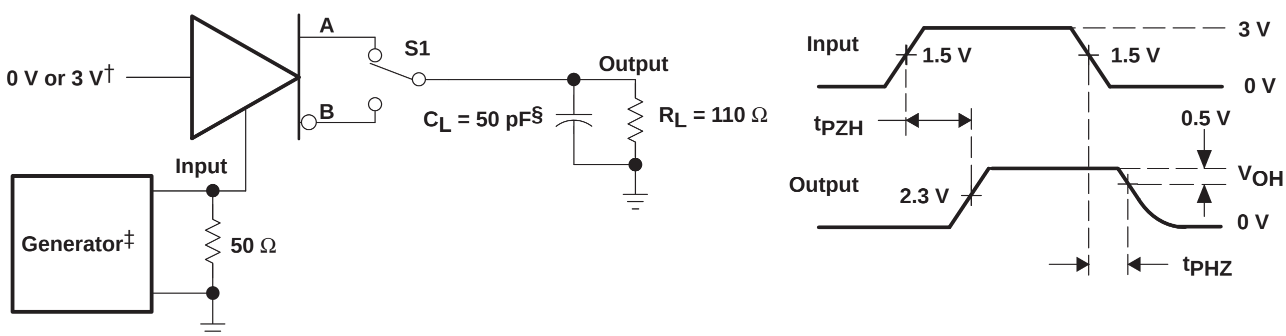
Figure 3. Driver Switching Test Circuit and Waveforms, 485-Loading

PARAMETER MEASUREMENT INFORMATION



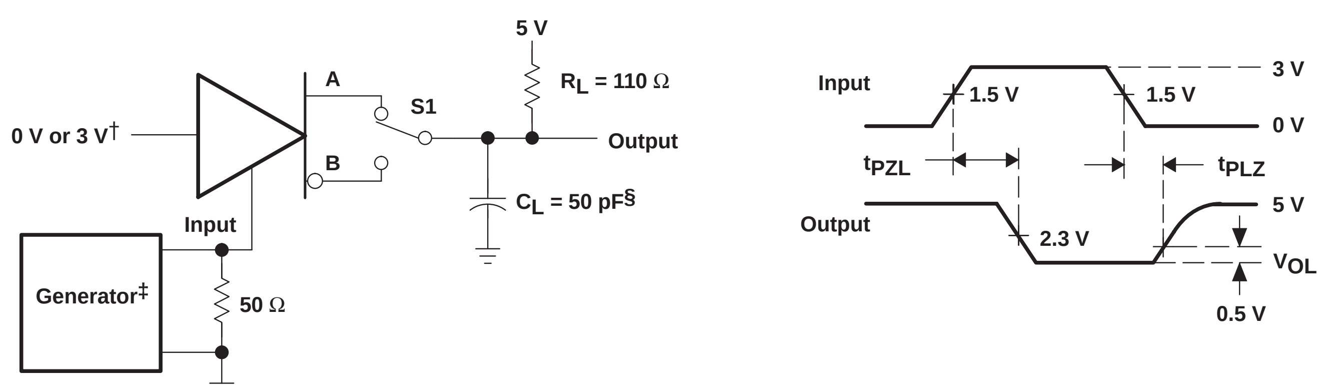
† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 4. Driver Switching Test Circuit and Waveforms, HVD SCSI-Loading (double terminated)



† 3 V if testing A output, 0 V if testing B output
‡ PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
§ Includes probe and jig capacitance

Figure 5. Driver Enable/Disable Test, High Output



† 0 V if testing A output, 3 V if testing B output
‡ PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
§ Includes probe and jig capacitance

Figure 6. Driver Enable/Disable Test, Low Output

PARAMETER MEASUREMENT INFORMATION

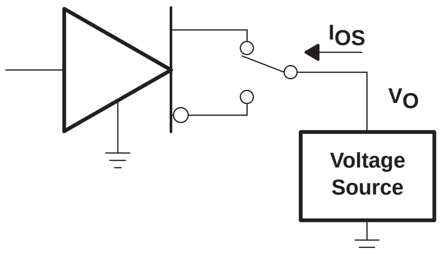


Figure 7. Driver Short-Circuit Test

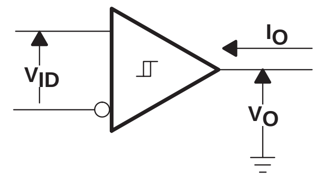
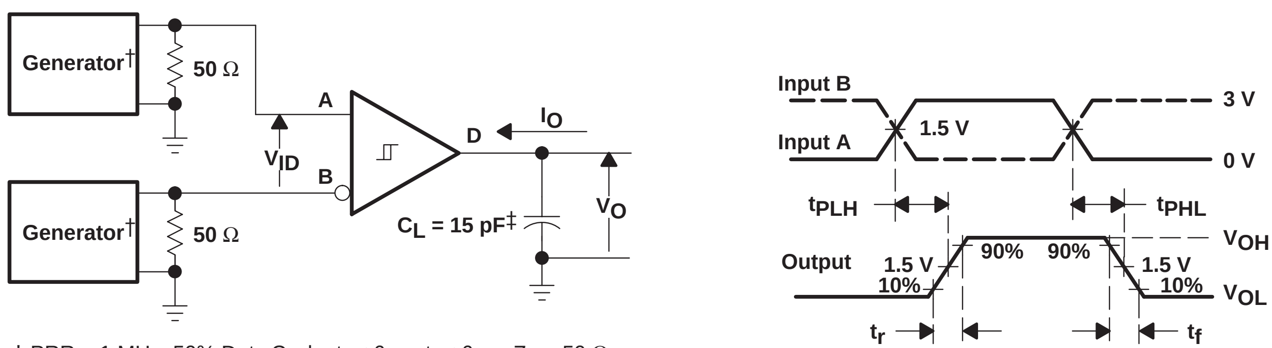
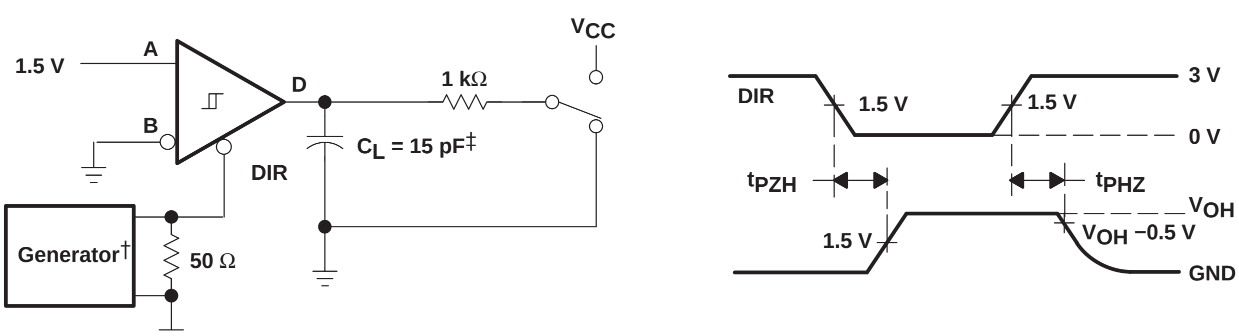


Figure 8. Receiver DC Parameters



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

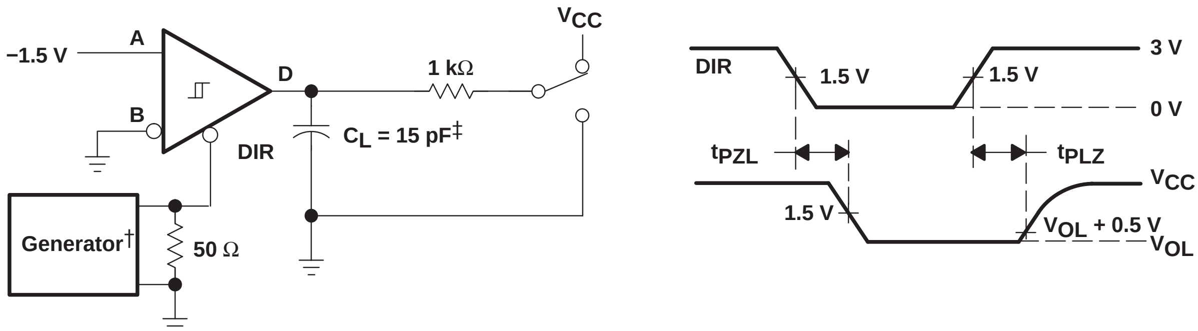
Figure 9. Receiver Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 10. Receiver Enable/Disable Test, High Output

PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 11. Receiver Enable/Disable Test, Low Output

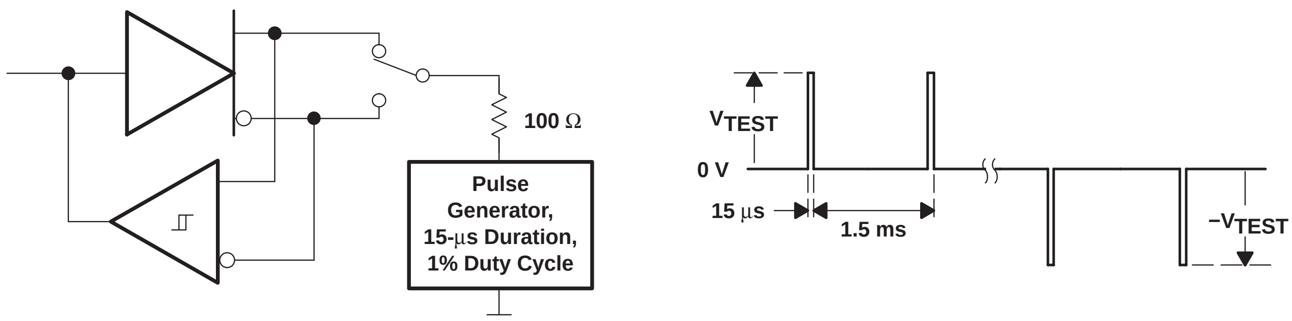


Figure 12. Test Circuit and Waveform, Transient Over Voltage Test

TYPICAL CHARACTERISTICS

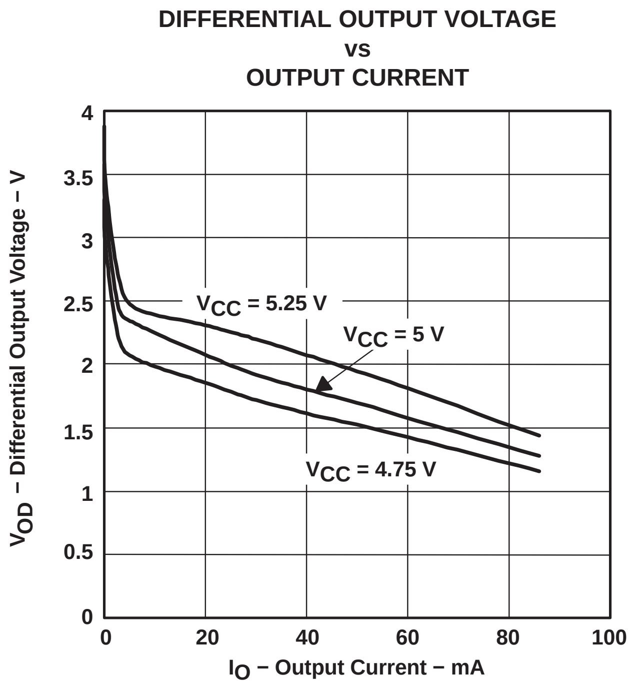


Figure 13

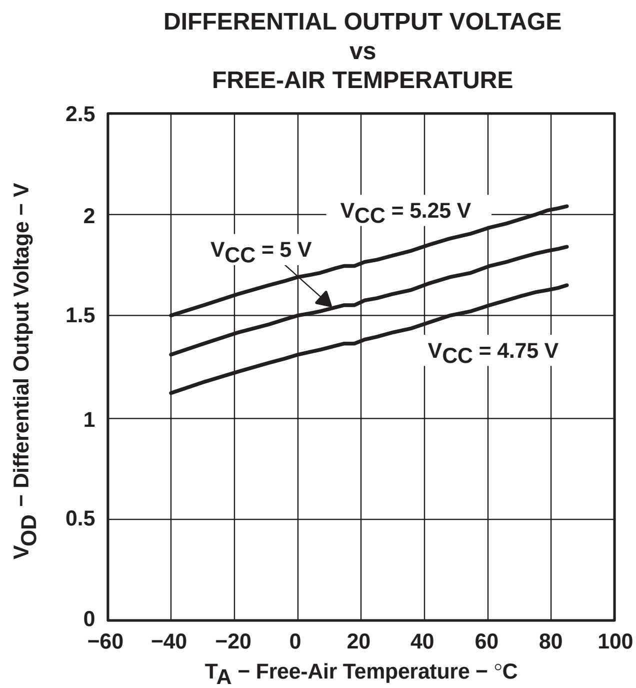


Figure 14

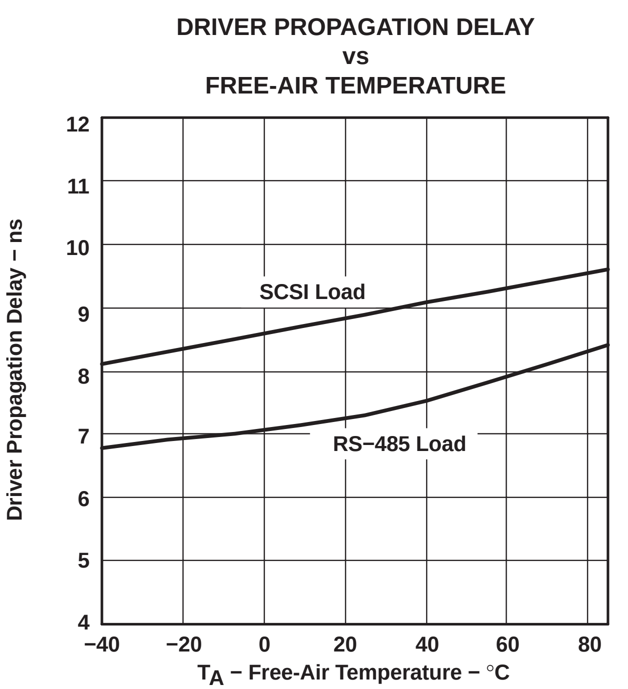


Figure 15

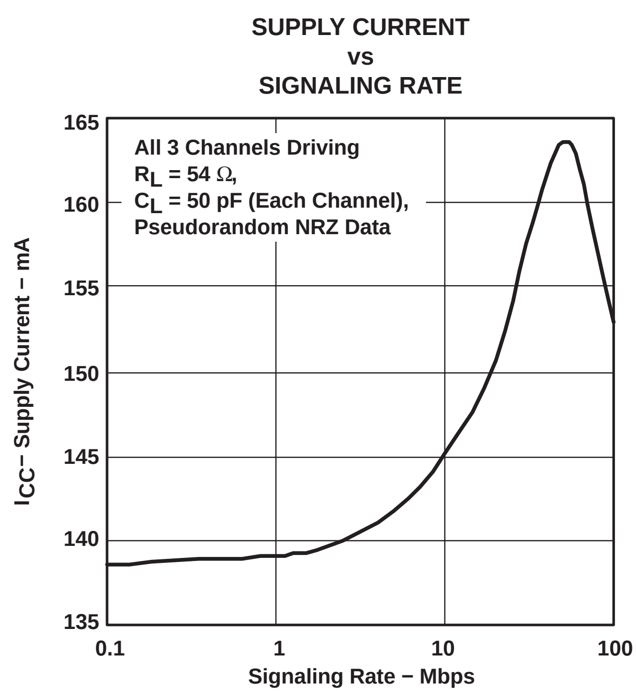


Figure 16

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

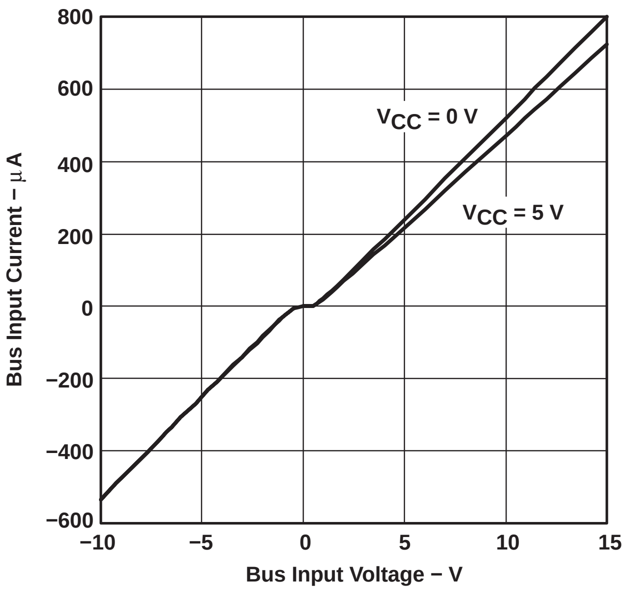


Figure 17

RECEIVER PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

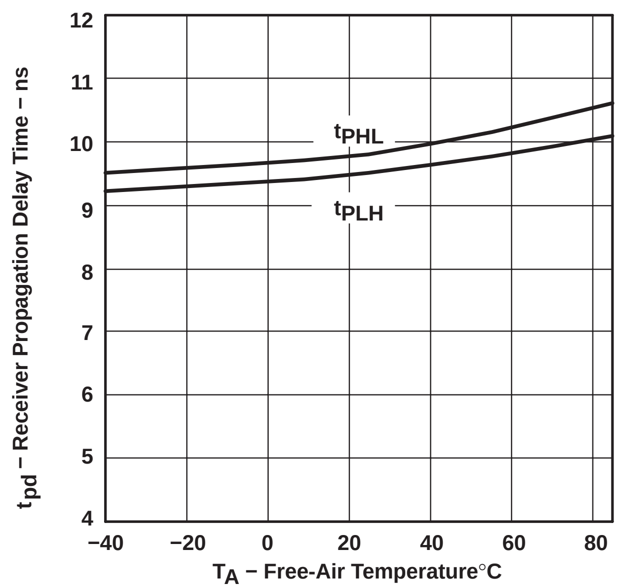


Figure 18

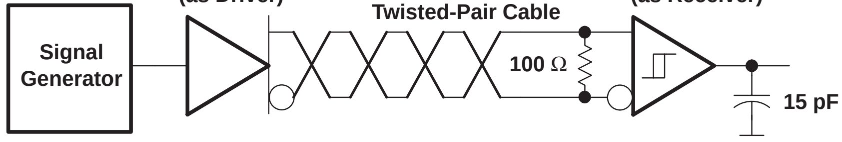


Figure 19. Circuit Diagram for Signaling Characteristics

TYPICAL CHARACTERISTICS

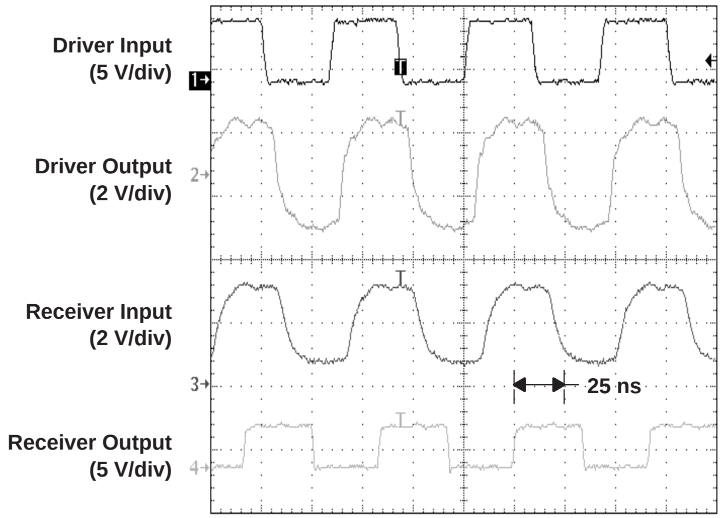


Figure 20. Signal Waveforms at 30 Mbps

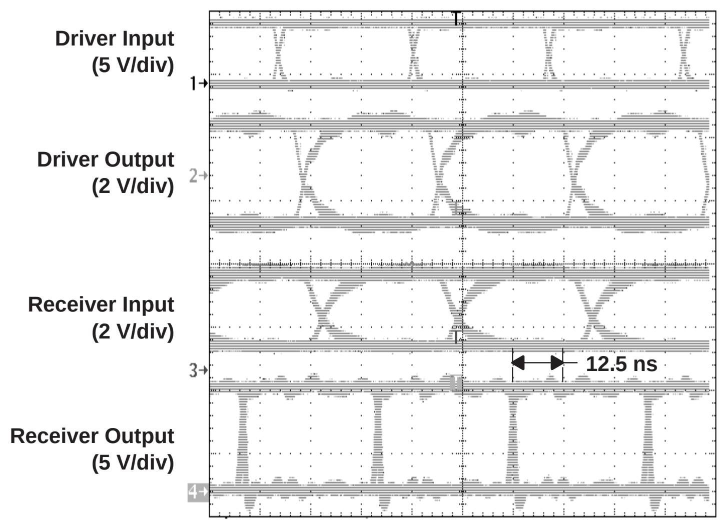


Figure 21. Eye Patterns, Pseudorandom Data at 30 Mbps

TYPICAL CHARACTERISTICS

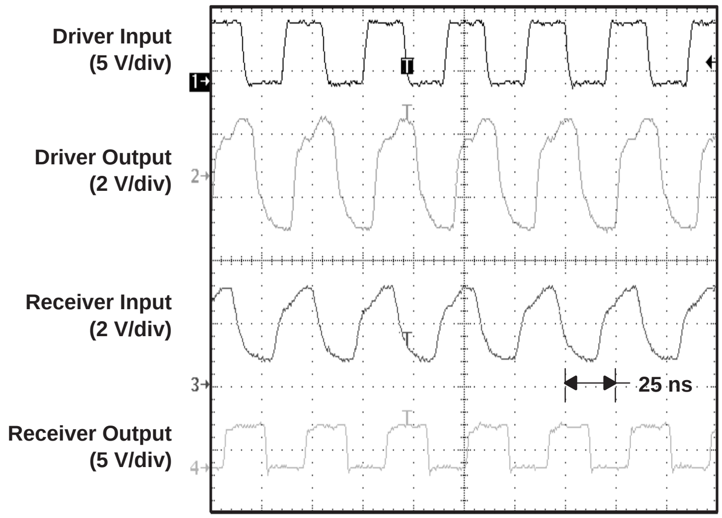


Figure 22. Signal Waveforms at 50 Mbps

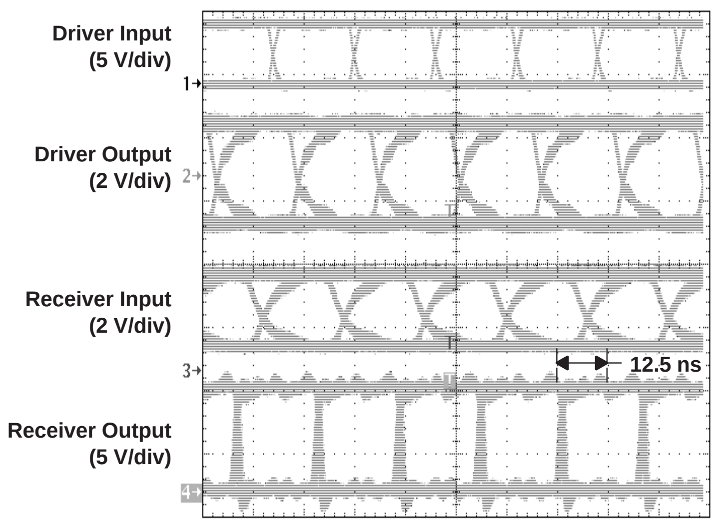


Figure 23. Eye Patterns, Pseudorandom Data at 50 Mbps

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LBC170DB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DWR	ACTIVE	SOIC	DW	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC170DWRG4	ACTIVE	SOIC	DW	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DW	ACTIVE	SOIC	DW	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DWG4	ACTIVE	SOIC	DW	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DWR	ACTIVE	SOIC	DW	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC170DWRG4	ACTIVE	SOIC	DW	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

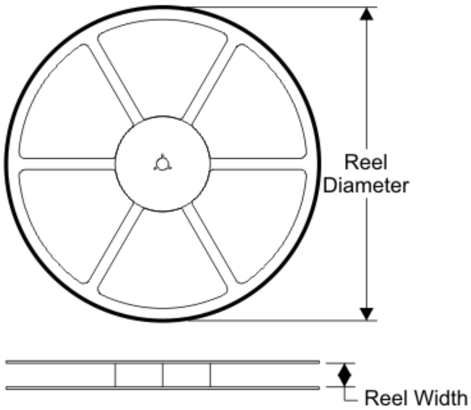
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

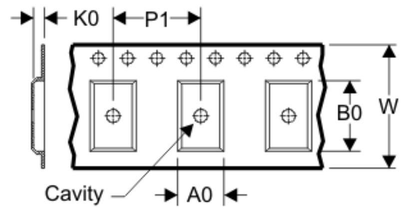
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

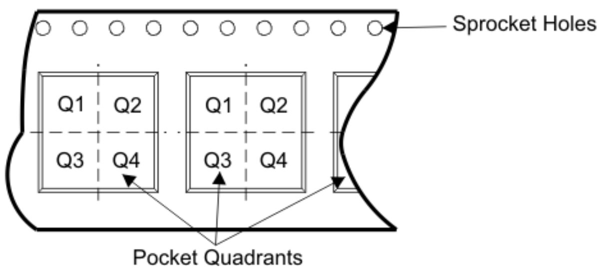


TAPE DIMENSIONS



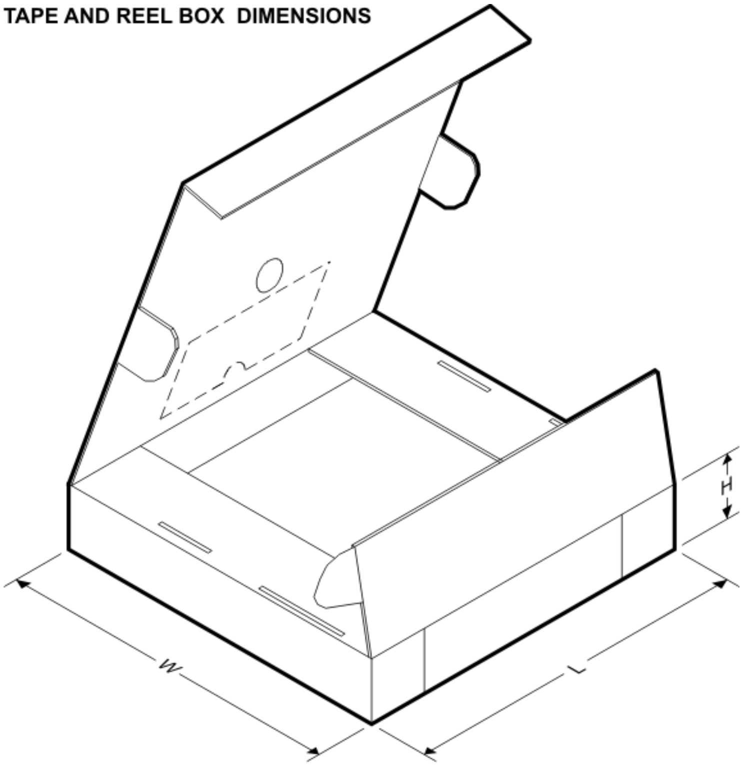
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



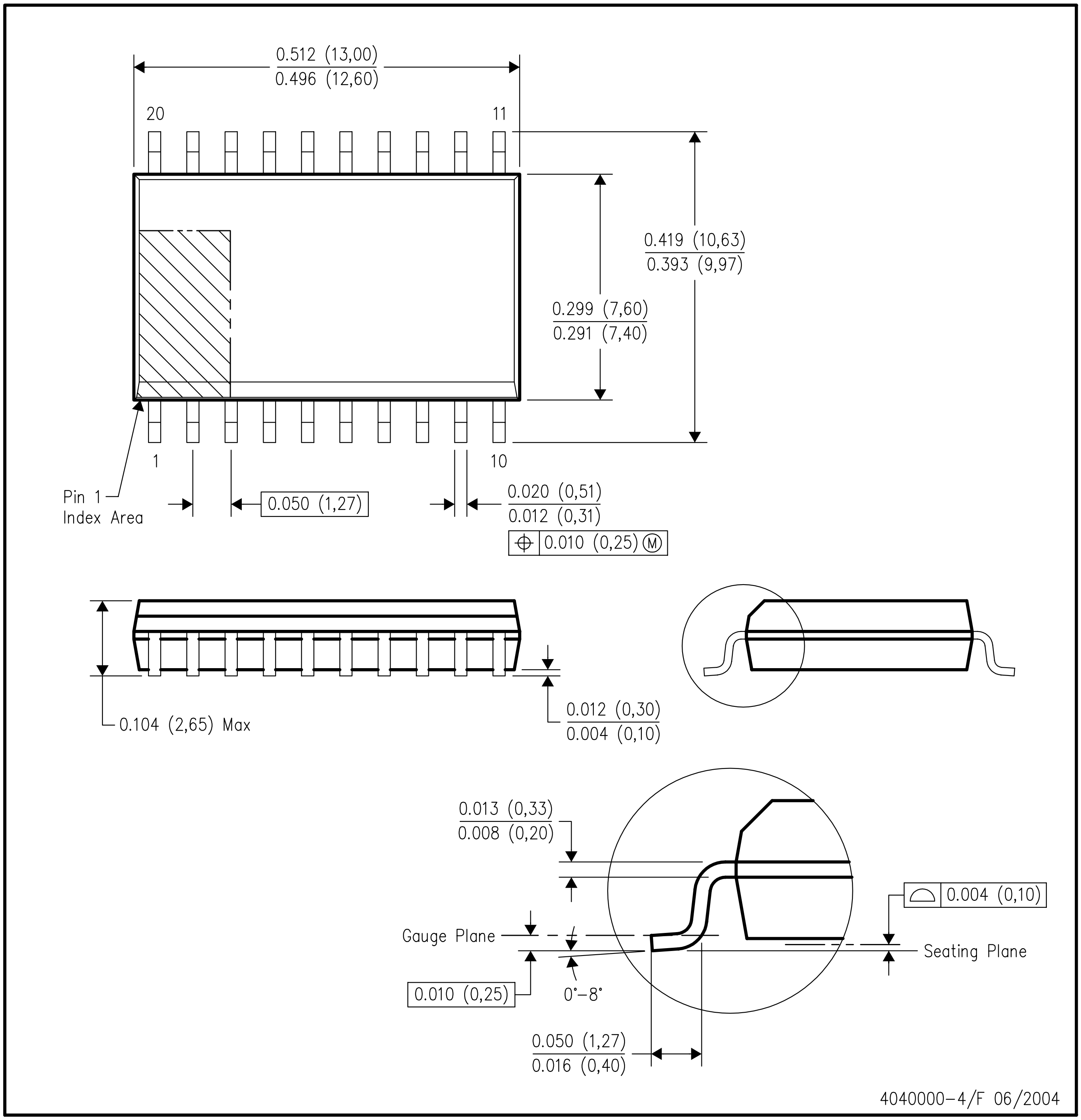
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC170DBR	DB	16	SITE 41	330	16	8.2	6.6	2.5	12	16	Q1
SN65LBC170DWR	DW	20	SITE 41	330	24	10.8	13.0	2.7	12	24	Q1
SN75LBC170DBR	DB	16	SITE 41	330	16	8.2	6.6	2.5	12	16	Q1
SN75LBC170DBRG4	DB	16	SITE 41	330	16	8.2	6.6	2.5	12	16	Q1
SN75LBC170DWR	DW	20	SITE 41	330	24	10.8	13.0	2.7	12	24	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65LBC170DBR	DB	16	SITE 41	346.0	346.0	33.0
SN65LBC170DWR	DW	20	SITE 41	346.0	346.0	41.0
SN75LBC170DBR	DB	16	SITE 41	346.0	346.0	33.0
SN75LBC170DBRG4	DB	16	SITE 41	346.0	346.0	33.0
SN75LBC170DWR	DW	20	SITE 41	346.0	346.0	41.0

DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

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