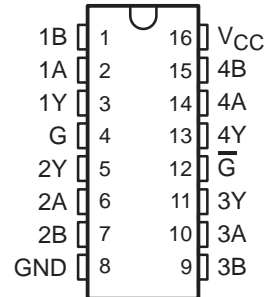


SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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- Meets or Exceeds ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range –7 V to 7 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 k Ω Min
- Operates from Single 5-V Supply
- Low Supply Current Requirement 35 mA Max
- Improved Speed and Power Version of the AM26LS32A

SN75ALS193 . . . D, J OR N PACKAGE
(TOP VIEW)



description

The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. This device meets the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of –7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the 'ALS192 quadruple differential line driver.

The SN75ALS193 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES		OUTPUT Y
	G	\bar{G}	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate,
Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

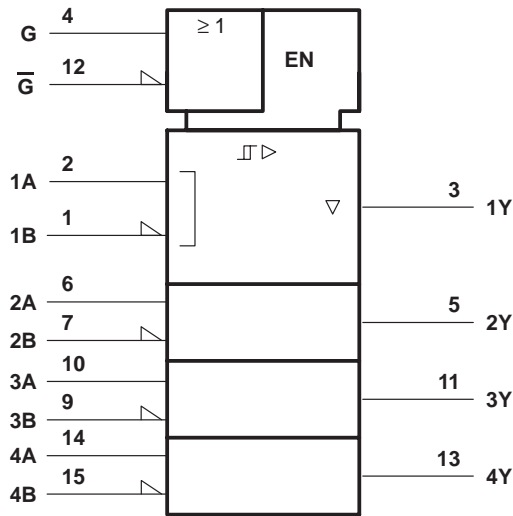
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SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

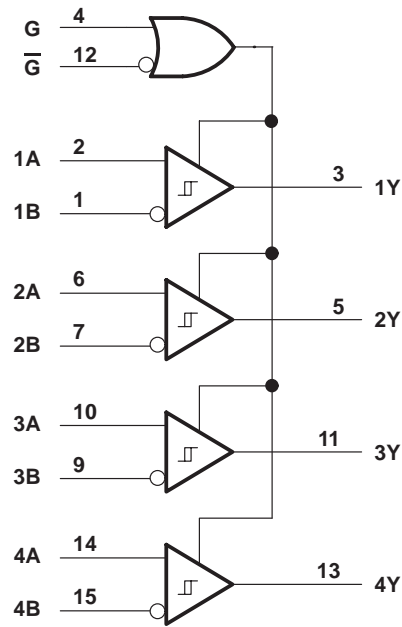
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logic symbol†

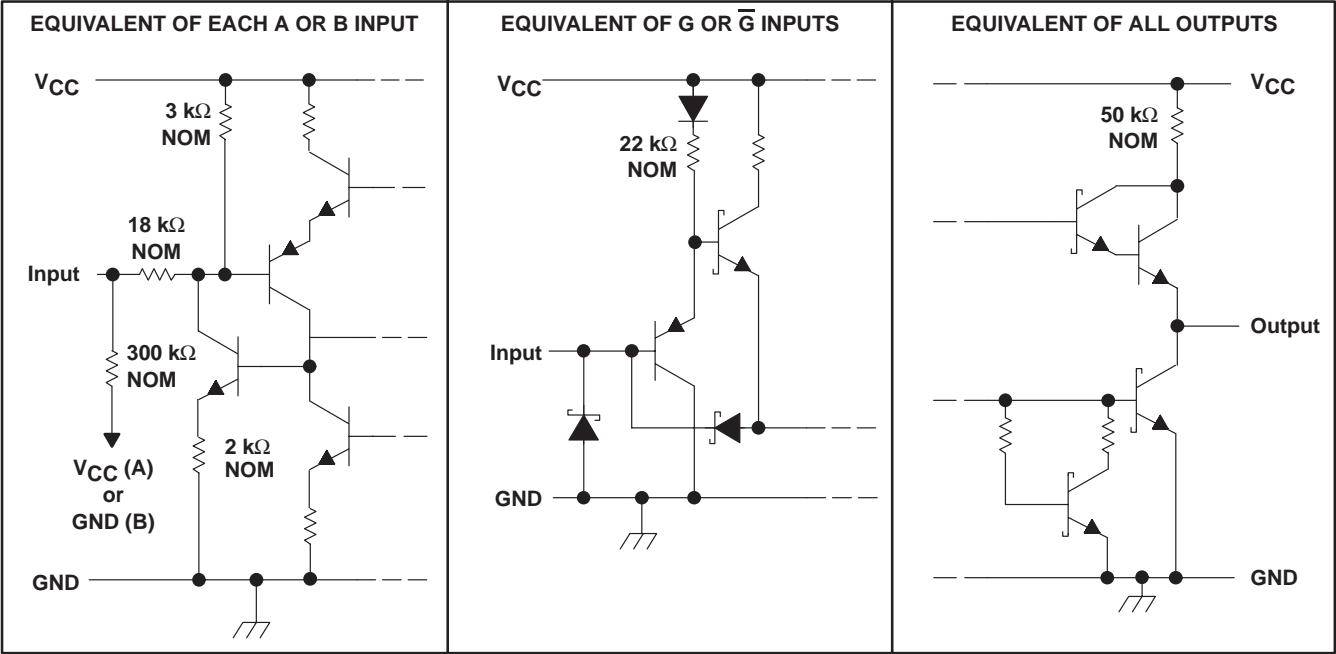


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (A or B)	± 15 V
Differential input voltage, V_{ID} (see Note 2)	± 15 V
Enable input voltage, V_I	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7	V
Differential input voltage, V_{ID}			± 12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

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QUADRUPLE DIFFERENTIAL LINE RECEIVER

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electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IT+} Positive-going input threshold voltage				200	mV
V_{IT-} Negative-going input threshold voltage		-200§			mV
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			120		mV
V_{IK} Enable-input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$, $V_{ID} = 200 \text{ mV}$, See Figure 1	2.5	3.6		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = -200 \text{ mV}$, See Figure 1	$I_{OL} = 8 \text{ mA}$		0.45	V
		$I_{OL} = 16 \text{ mA}$		0.5	
I_{OZ} High-impedance-state output current	$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$		20	μA
		$V_O = 0.4 \text{ V}$		-20	
I_I Line input current	Other input at 0, See Note 3	$V_{CC} = \text{MIN}$, $V_I = 15 \text{ V}$		0.7	mA
		$V_{CC} = \text{MIN}$, $V_I = -15 \text{ V}$		-1.0	
I_{IH} High-level enable-input current	$V_{CC} = \text{MAX}$	$V_{IH} = 2.7 \text{ V}$		20	μA
		$V_{IH} = \text{MAX}$		100	
I_{IL} Low-level enable-input current	$V_{CC} = \text{MAX}$, $V_{IL} = 0.4 \text{ V}$			-100	μA
Input resistance		12	18		k Ω
I_{OS} Short-circuit output current	$V_{CC} = \text{MAX}$, $V_O = 0$, $V_{ID} = 3 \text{ V}$, See Note 4	-15	-78	-130	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, Outputs disabled		22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.

4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$V_{ID} = -2.5 \text{ V to } 2.5 \text{ V}$, $C_L = 15 \text{ pF}$, See Figure 2		15	22	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	22	
t_{PZH} Output enable time to high level	$C_L = 15 \text{ pF}$, See Figure 3		13	25	
t_{PZL} Output enable time to low level			11	25	
t_{PHZ} Output disable time from high level	$C_L = 5 \text{ pF}$, See Figure 3		13	25	
t_{PLZ} Output disable time from low level			15	22	



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PARAMETER MEASUREMENT INFORMATION

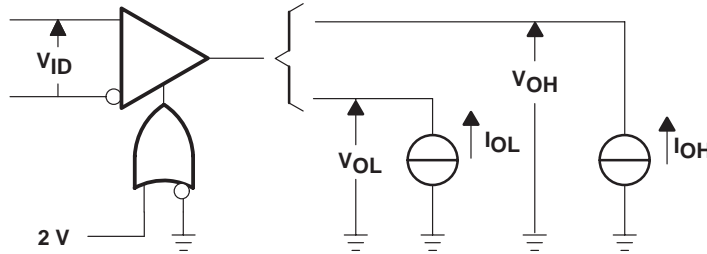
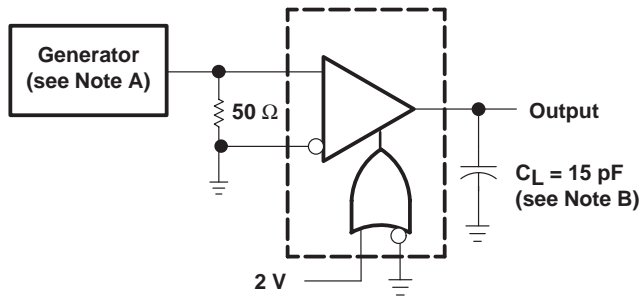
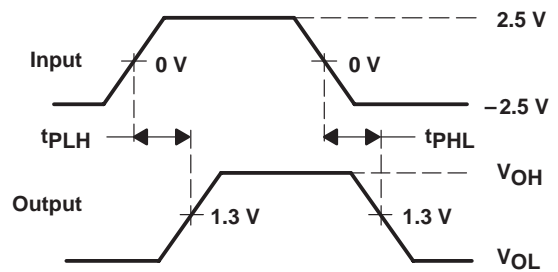


Figure 1. V_{OH} , V_{OL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

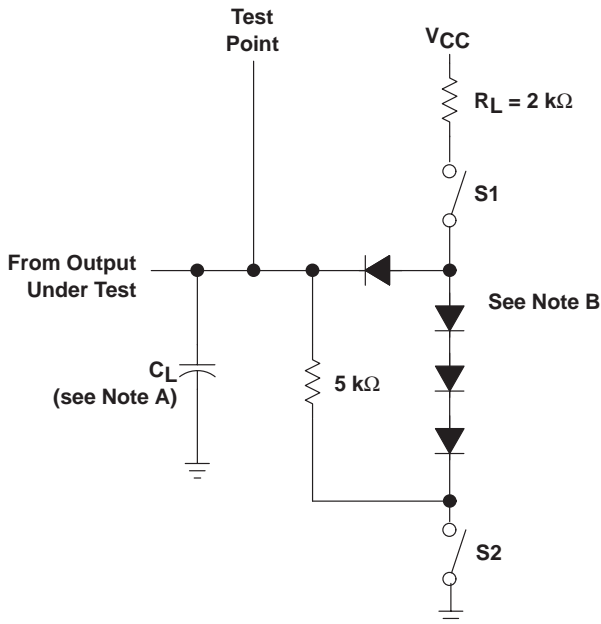
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

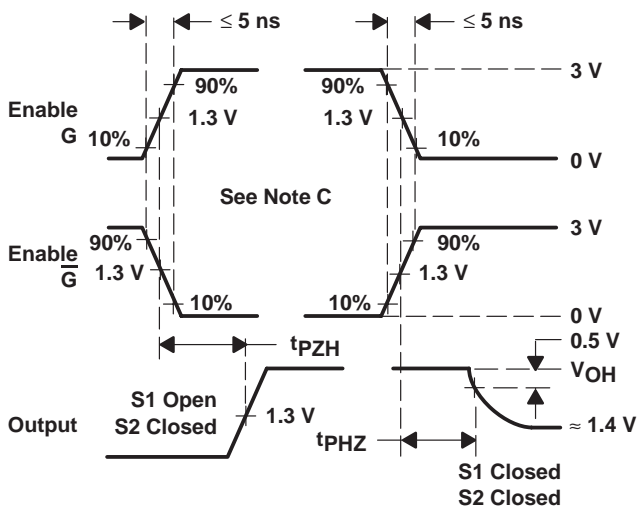
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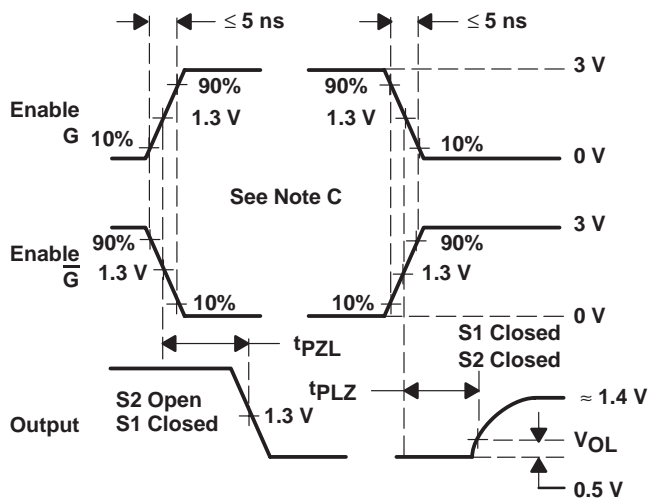
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ} , t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ} , t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with \overline{G} high; \overline{G} is tested with G low.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

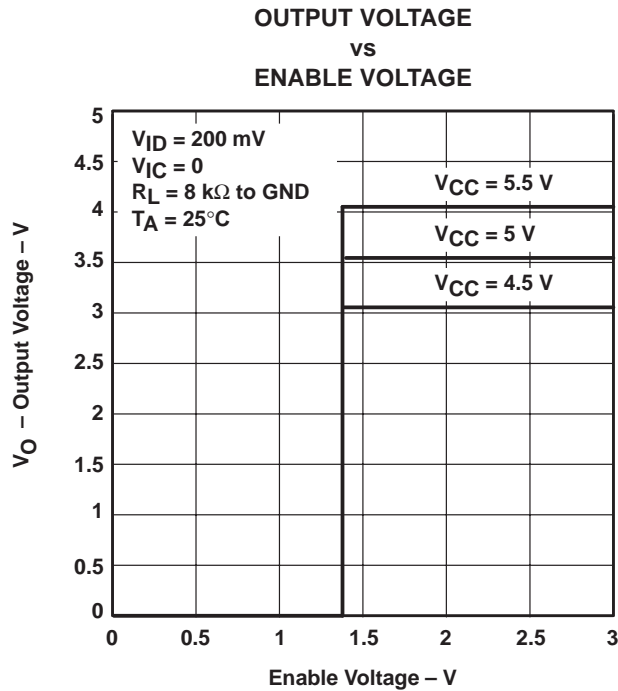


Figure 4

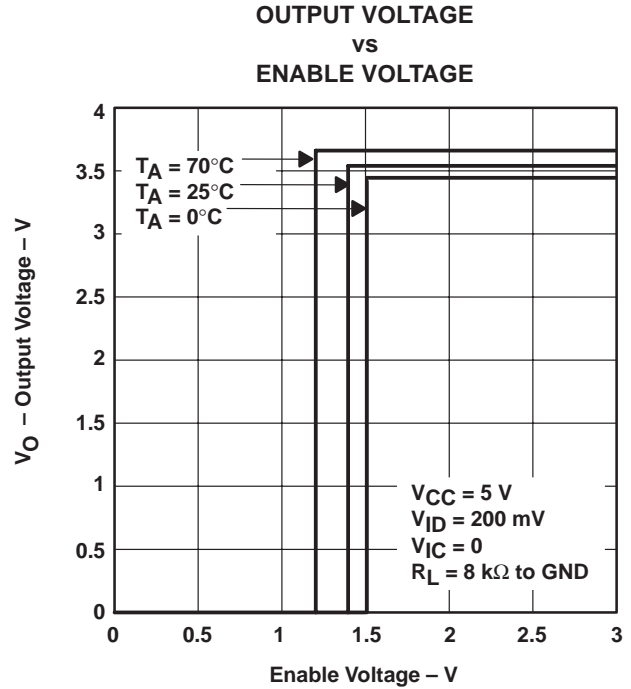


Figure 5

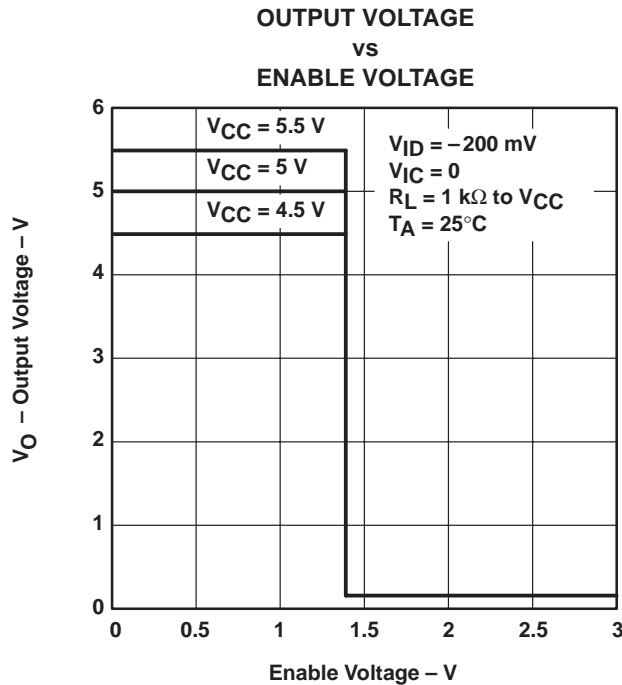


Figure 6

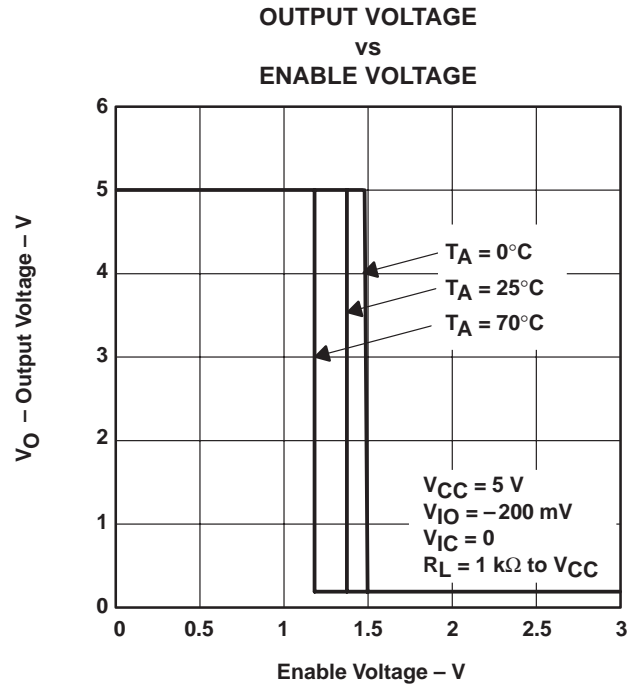


Figure 7

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TYPICAL CHARACTERISTICS

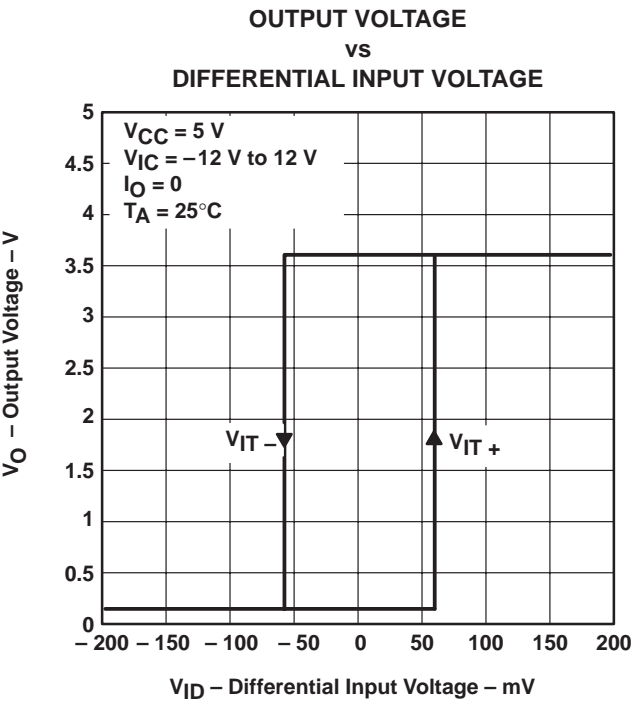


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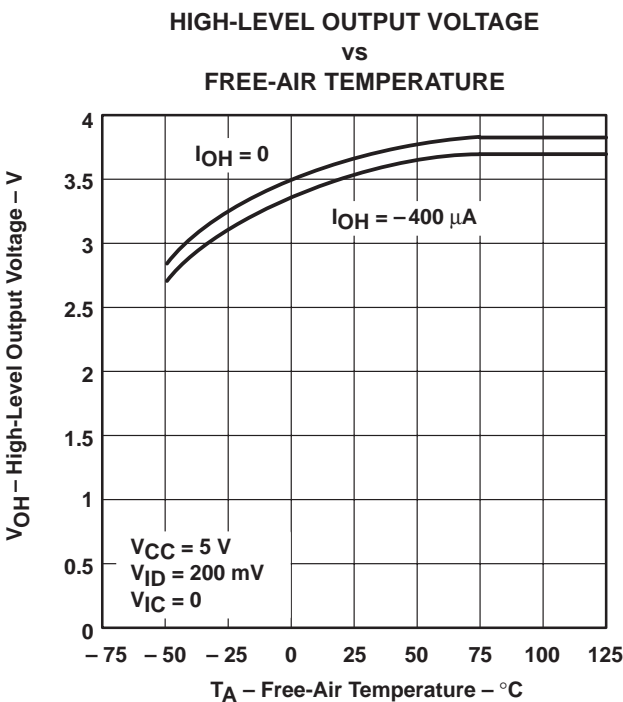


Figure 9

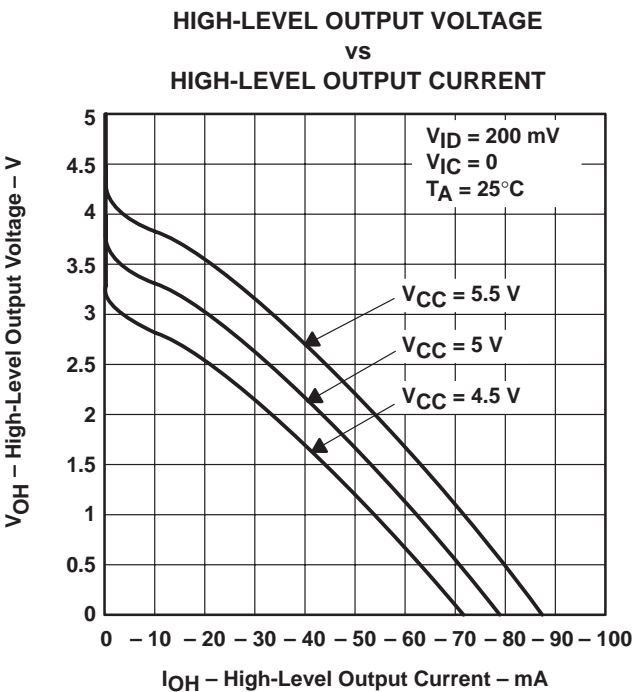


Figure 10

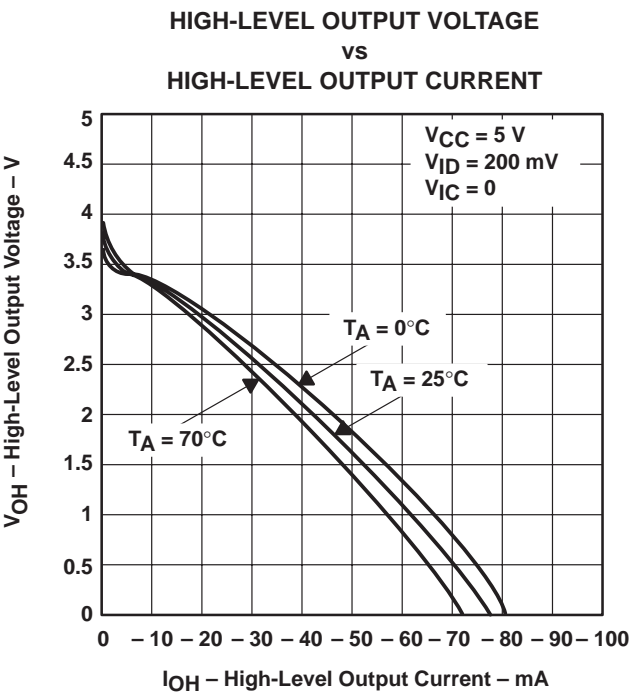


Figure 11

TYPICAL CHARACTERISTICS

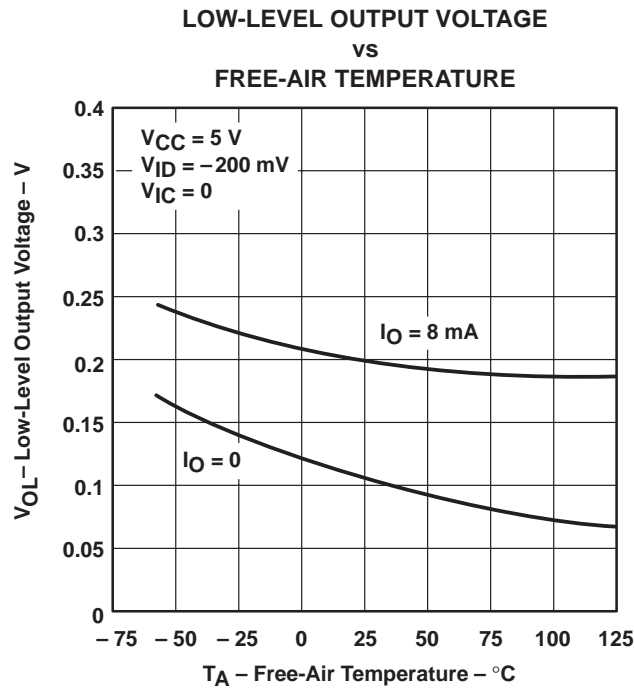


Figure 12

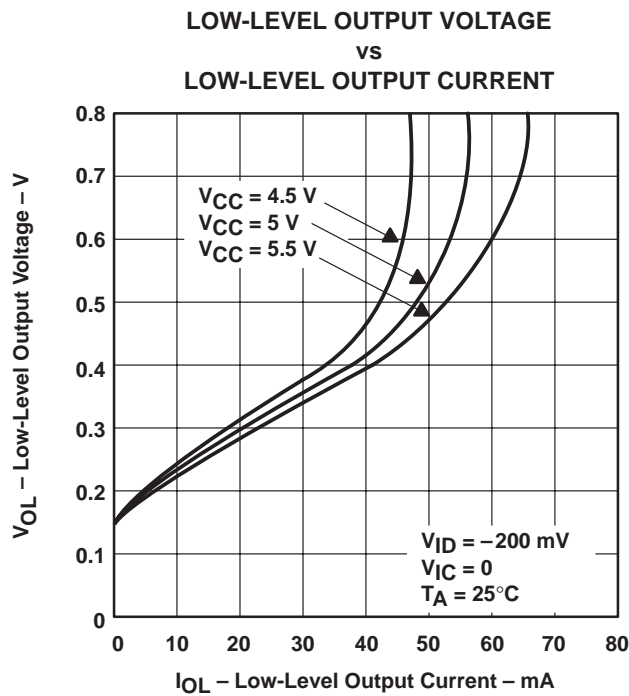


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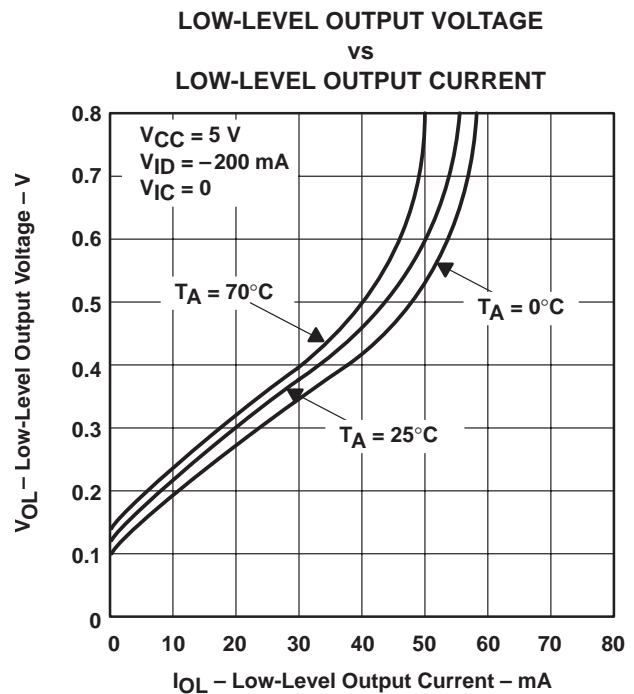


Figure 14

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TYPICAL CHARACTERISTICS

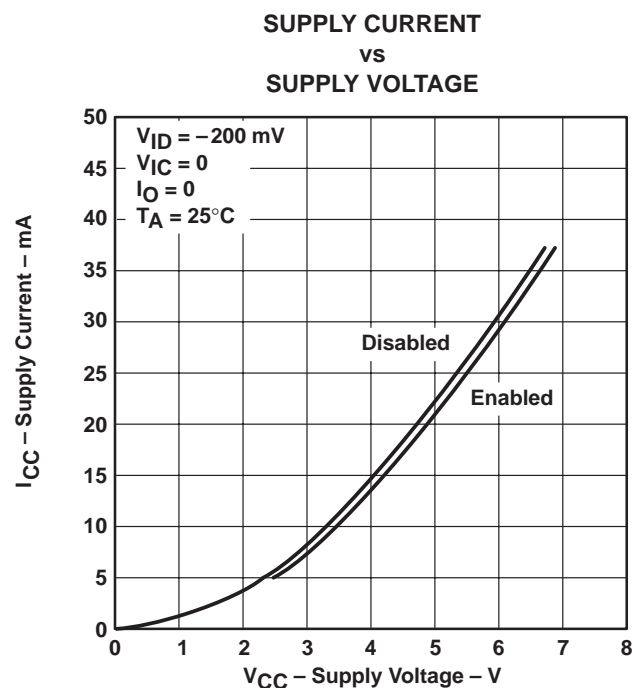


Figure 15

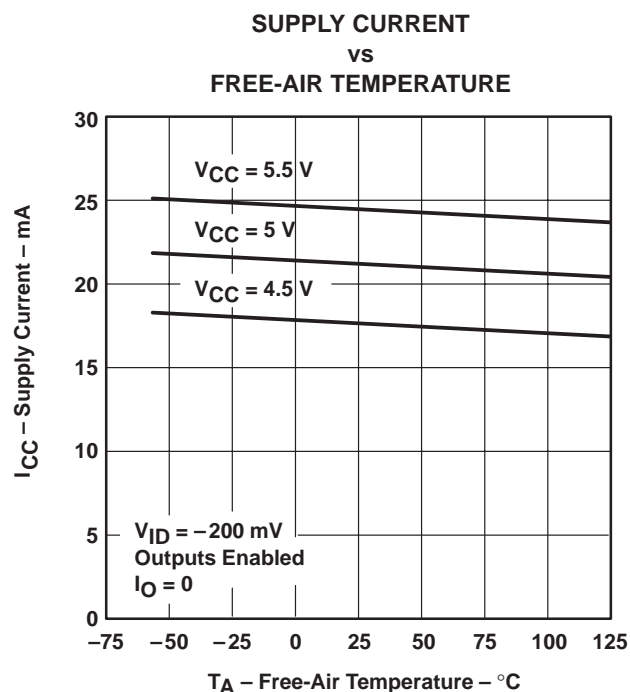


Figure 16

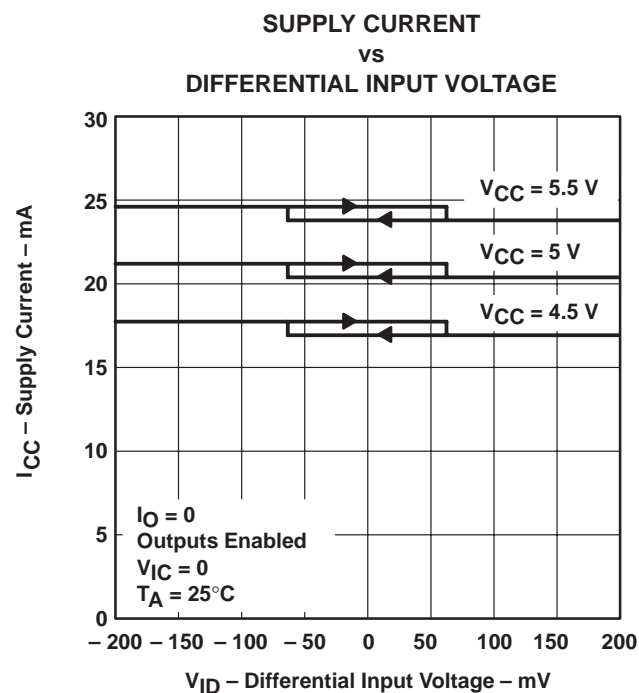


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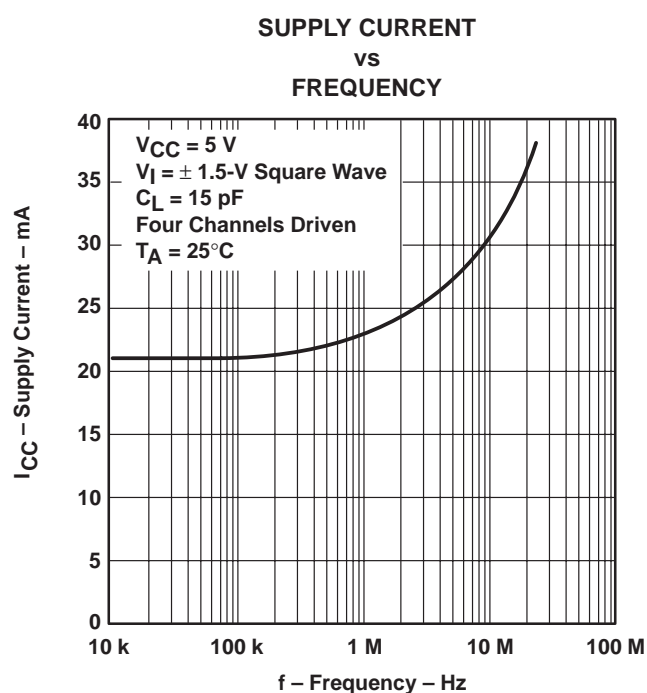


Figure 18

TYPICAL CHARACTERISTICS

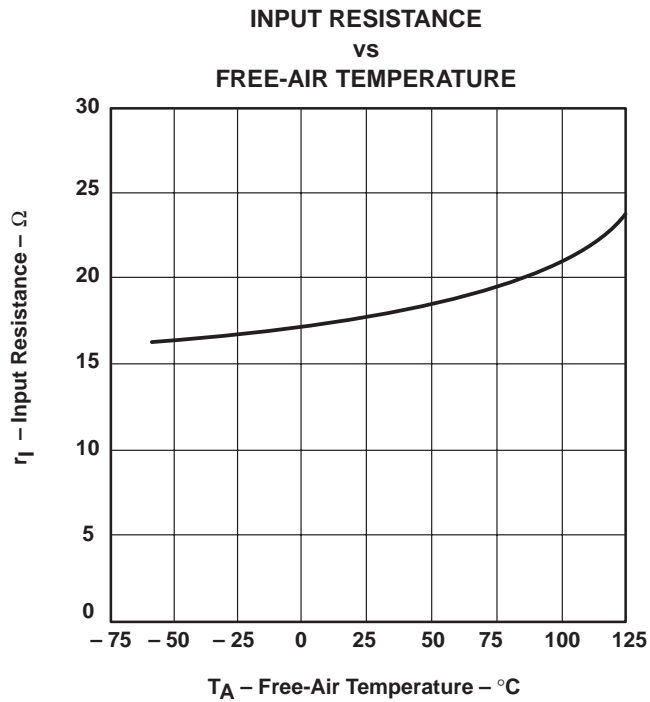


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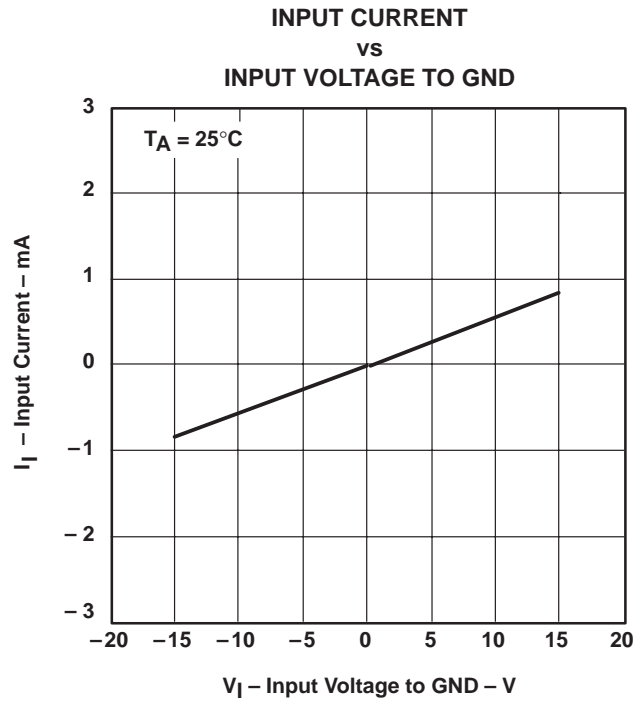


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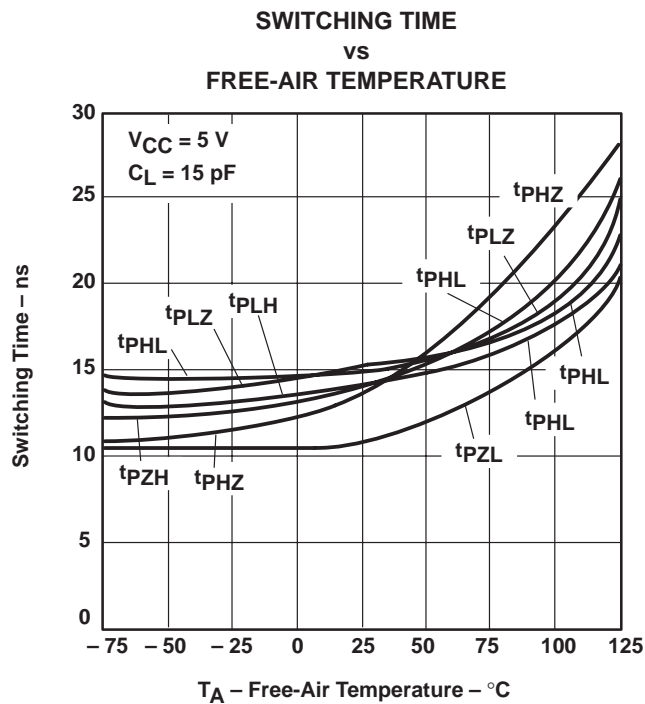


Figure 21

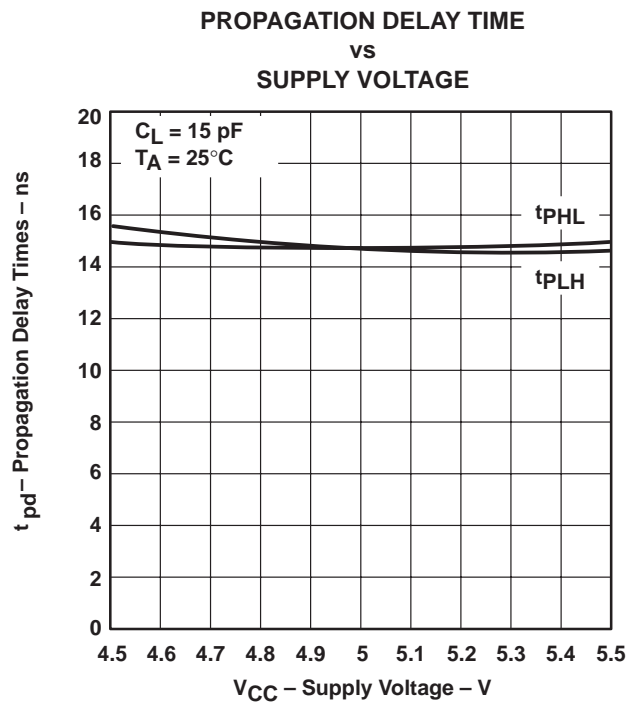


Figure 22

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