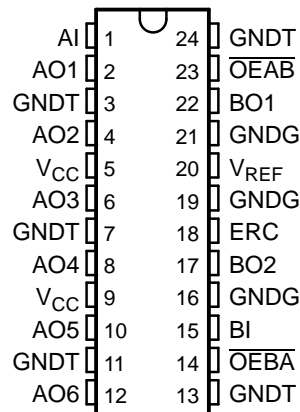


## FEATURES

- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTLP 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I<sub>off</sub> and Power-Up 3-State Support Hot Insertion**
- **Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGV, DW, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74GTLP817 is a medium-drive fanout driver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, and OEC™ circuitry. The improved GTLP OEC circuitry minimizes bus settling time and has been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω. BO1 and BO2 can be tied together to drive an equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP817 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V<sub>TT</sub> = 1.2 V and V<sub>REF</sub> = 0.8 V) or GTLP (V<sub>TT</sub> = 1.5 V and V<sub>REF</sub> = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V<sub>REF</sub> is the B-port differential input reference voltage.

GNDT is the TTL output ground, while GNDG is the GTLP output ground, and both may be separated from each other for a quieter device.



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# SN74GTLP817

## GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E–OCTOBER 1999–REVISED APRIL 2005



### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and  $V_{CC}$  adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load. ERC automatically is selected to the same speed as alternate source 1-to-6 fanout drivers that use pin 18 for 3.3-V or 5-V  $V_{CC}$ .

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ( $\overline{OE}$ ) input should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP817DW	GTLP817
		Tape and reel	SN74GTLP817DWR	
	TSSOP – PW	Tape and reel	SN74GTLP817PWR	GT817
	TVSOP – DGV	Tape and reel	SN74GTLP817DGVR	GT817

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTIONAL DESCRIPTION

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTLP translation and GTLP-to-LVTTL translation in the same package.

The LVTTL-to-GTLP direction is a 1-to-2 fanout driver with a single output enable ( $\overline{OEAB}$ ).

The GTLP-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable ( $\overline{OEBA}$ ).

Data polarity is inverting for both directions.

## FUNCTION TABLES

### OUTPUT CONTROL (A TO B)

INPUTS		OUTPUT BOn	MODE
AI	$\overline{OEAB}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

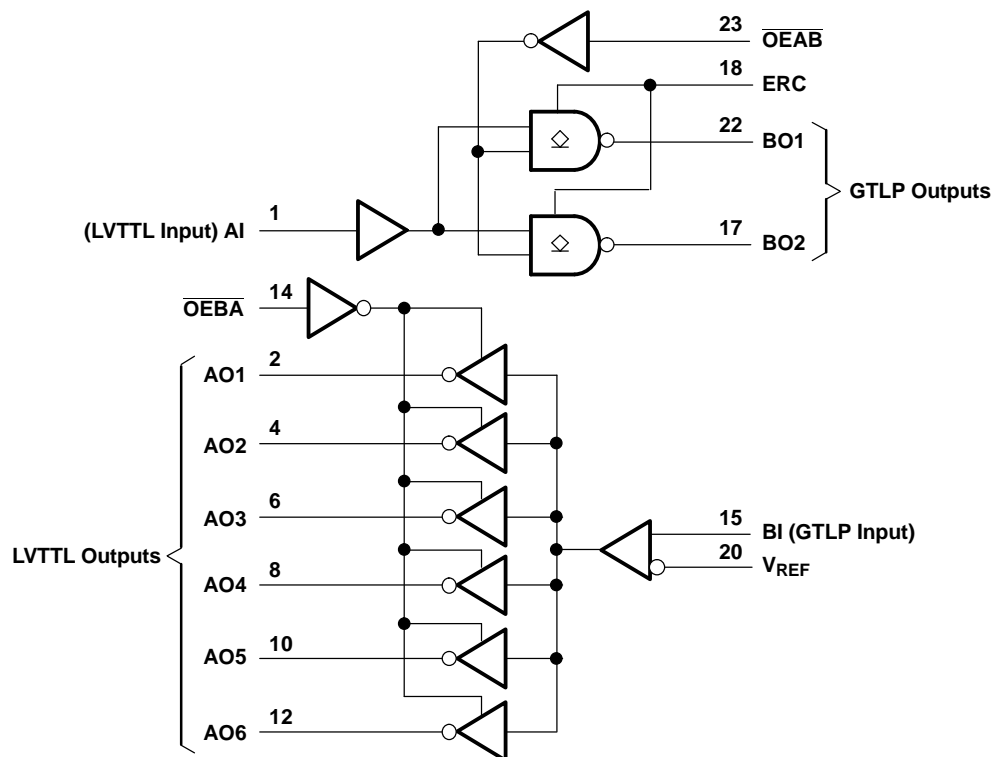
### OUTPUT CONTROL (B TO A)

INPUTS		OUTPUT AOn	MODE
BI	$\overline{OEBA}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

### B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	$V_{CC}$	Slow
L	GND	Fast

### LOGIC DIAGRAM (POSITIVE LOGIC)



# SN74GTLP817

## GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E–OCTOBER 1999–REVISED APRIL 2005

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		–0.5	4.6	V
$ V_{GNDG} - V_{GNDT} $	Ground dc voltage difference			0.3	V
$V_I$	Input voltage range <sup>(2)</sup>	AI port and control inputs	–0.5	7	V
		BI port and $V_{REF}$	–0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	AO port	–0.5	7	V
		BO port	–0.5	4.6	
$I_O$	Current into any output in the low state	AO port		24	mA
		BO port		100	
$I_O$	Current into any A output in the high state <sup>(3)</sup>			24	mA
	Continuous current through each $V_{CC}$ or GND			±100	mA
$I_{IK}$	Input clamp current	$V_I < 0$		–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGV package		86	°C/W
		DW package		46	
		PW package		88	
$T_{stg}$	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions**<sup>(1)(2)(3)(4)</sup>

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3.15	3.3	3.45	V
V <sub>TT</sub>	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V <sub>REF</sub>	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V <sub>I</sub>	Input voltage	BI	V <sub>TT</sub>			V
		AI, $\overline{OE}$	V <sub>CC</sub> 5.5			
V <sub>IH</sub>	High-level input voltage	BI	V <sub>REF</sub> + 0.05			V
		ERC	V <sub>CC</sub> − 0.6	V <sub>CC</sub>	5.5	
		AI, $\overline{OE}$	2			
V <sub>IL</sub>	Low-level input voltage	BI	V <sub>REF</sub> − 0.05			V
		ERC	GND 0.6			
		AI, $\overline{OE}$	0.8			
I <sub>IK</sub>	Input clamp current				−18	mA
I <sub>OH</sub>	High-level output current	AO port			−12	mA
I <sub>OL</sub>	Low-level output current	AO port			12	mA
		BO port			50	
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		20			μs/V
T <sub>A</sub>	Operating free-air temperature		−40		85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Normal connection sequence is GND first and  $V_{CC} = 3.3$  V, I/O, control inputs,  $V_{TT}$ ,  $V_{REF}$  (any order) last.
- (3)  $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded.
- (4)  $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ .

# SN74GTLP817

## GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E – OCTOBER 1999 – REVISED APRIL 2005



### Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.15\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	AO port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ ,	$I_{OH} = -100\text{ }\mu\text{A}$			$V_{CC} - 0.2$	V
			$I_{OH} = -100\text{ }\mu\text{A}$			$V_{CC} - 0.2$	
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -6\text{ mA}$			2.4	
			$I_{OH} = -12\text{ mA}$			2.2	
$V_{OL}$	AO port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$ ,	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
			$I_{OL} = 100\text{ }\mu\text{A}$			0.2	
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 6\text{ mA}$			0.4	
			$I_{OL} = 12\text{ mA}$			0.5	
	BO port	$V_{CC} = 3.15\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	
			$I_{OL} = 40\text{ mA}$			0.5	
			$I_{OL} = 50\text{ mA}$			0.55	
$I_I$	BI, AI, $\overline{OE}$ , ERC	$V_{CC} = 3.45\text{ V}$ ,	$V_I = 0\text{ or } 5.5\text{ V}$			$\pm 5$	$\mu\text{A}$
$I_{OZH}$	AO port	$V_{CC} = 3.45\text{ V}$	$V_O = V_{CC}$			10	$\mu\text{A}$
	BO port		$V_O = 1.5\text{ V}$			5	
$I_{OZL}$	AO port	$V_{CC} = 3.45\text{ V}$	$V_O = \text{GND}$			-10	$\mu\text{A}$
	BO port		$V_O = 5.5\text{ V}$			-5	
$I_{CC}$	AO or BO port	$V_{CC} = 3.45\text{ V}$ , $I_O = 0$ , $V_I$ (AI or control input) = $V_{CC}$ or GND, $V_I$ (BI input) = $V_{TT}$ or GND	Outputs high			10	mA
			Outputs low			10	
			Outputs disabled			10	
$\Delta I_{CC}^{(2)}$	AI, $\overline{OE}$	$V_{CC} = 3.45\text{ V}$ , One A-port or control input at $V_{CC} - 0.6\text{ V}$ , Other A-port or control inputs at $V_{CC}$ or GND				1	mA
$C_i$	AI, $\overline{OE}$ , ERC	$V_I = V_{CC}$ or 0			4	4.4	pF
	BI	$V_I = V_{TT}$ or 0			3.5	3.9	
$C_o$	AO port	$V_O = V_{CC}$ or 0			4	4.5	pF
	BO port	$V_O = V_{TT}$ or 0			5	5.4	

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified LVTTL voltage level, rather than  $V_{CC}$  or GND.

### Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0\text{ to } 5.5\text{ V}$			10	$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to } 1.5\text{ V}$ ,	$V_O = 0.5\text{ V to } 3\text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to } 0$ ,	$V_O = 0.5\text{ V to } 3\text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$

### Hot-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0\text{ to } 1.5\text{ V}$			10	$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to } 1.5\text{ V}$ ,	$V_O = 0.5\text{ V to } 1.5\text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to } 0$ ,	$V_O = 0.5\text{ V to } 1.5\text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$

## Switching Characteristics

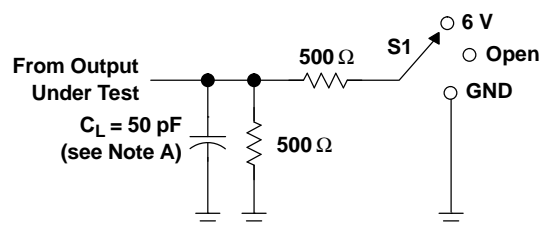
over recommended ranges of supply voltage and operating free-air temperature,  
 $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
t <sub>PLH</sub>	AI	BO	Slow	3		6	ns
t <sub>PHL</sub>				1.8		4.7	
t <sub>PLH</sub>	AI	BO	Fast	2		5	ns
t <sub>PHL</sub>				1.5		4.2	
t <sub>en</sub>	$\overline{OEAB}$	BO	Slow	3		6.1	ns
t <sub>dis</sub>				2		4.7	
t <sub>en</sub>	$\overline{OEAB}$	BO	Fast	2.1		6	ns
t <sub>dis</sub>				1.5		4.7	
t <sub>r</sub>	Rise time, B outputs (20% to 80%)		Slow	2.5		ns	
			Fast	1.4			
t <sub>f</sub>	Fall time, B outputs (80% to 20%)		Slow	1.7		ns	
			Fast	1			
t <sub>PLH</sub>	BI	AO		2.3		6	ns
t <sub>PHL</sub>				1.9		4.7	
t <sub>en</sub>	$\overline{OEBA}$	AO		1.1		6.3	ns
t <sub>dis</sub>				1.2		5	

(1) Slow (ERC =  $V_{CC}$ ) and Fast (ERC = GND)

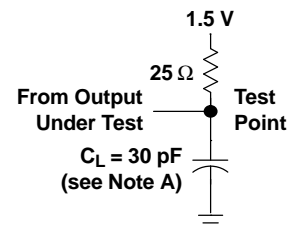
(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION

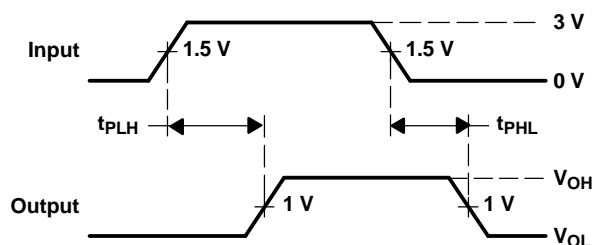


LOAD CIRCUIT FOR AO PORTS

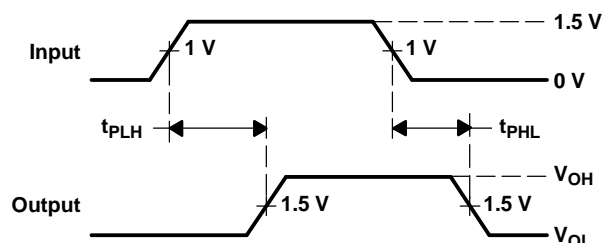
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



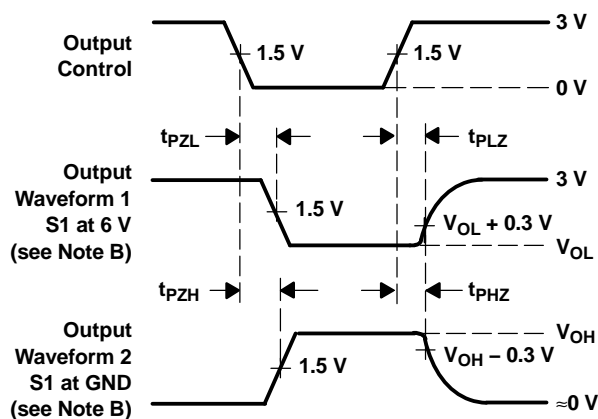
LOAD CIRCUIT FOR BO PORTS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(AI to BO port)



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(BI to AO port)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
(AO ports)

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\approx 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \approx 2 \text{ ns}$ ,  $t_f \approx 2 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**



## Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See [www.ti.com/sc/gtlp](http://www.ti.com/sc/gtlp) for more information.

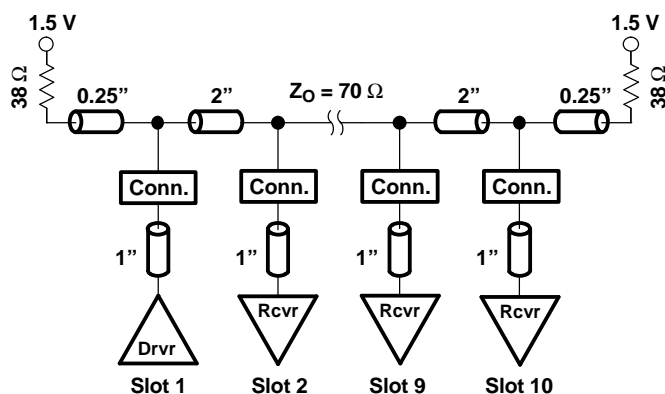


Figure 2. Medium-Drive Test Backplane

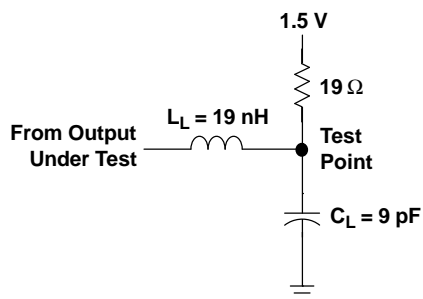


Figure 3. Medium-Drive RLC Network

# SN74GTLP817

## GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E—OCTOBER 1999—REVISED APRIL 2005

### Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,  
 $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE <sup>(1)</sup>	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	AI	BO	Slow	4.4	ns
t <sub>PHL</sub>				4.4	
t <sub>PLH</sub>	AI	BO	Fast	3.2	ns
t <sub>PHL</sub>				3.2	
t <sub>en</sub>	$\overline{OEAB}$	BO	Slow	4	ns
t <sub>dis</sub>				4.4	
t <sub>en</sub>	$\overline{OEAB}$	BO	Fast	2.9	ns
t <sub>dis</sub>				3.1	
t <sub>r</sub>	Rise time, B outputs (20% to 80%)		Slow	1.8	ns
			Fast	1	
t <sub>f</sub>	Fall time, B outputs (80% to 20%)		Slow	2	ns
			Fast	1.6	

(1) Slow (ERC =  $V_{CC}$ ) and Fast (ERC = GND)

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . All values are derived from TI-SPICE models.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74GTLP817DGV	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTLP817PWGR4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

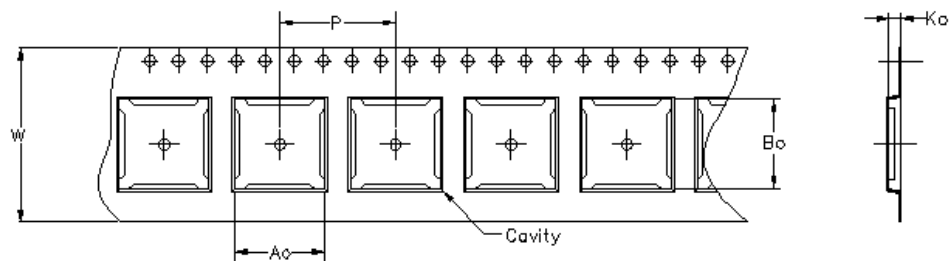
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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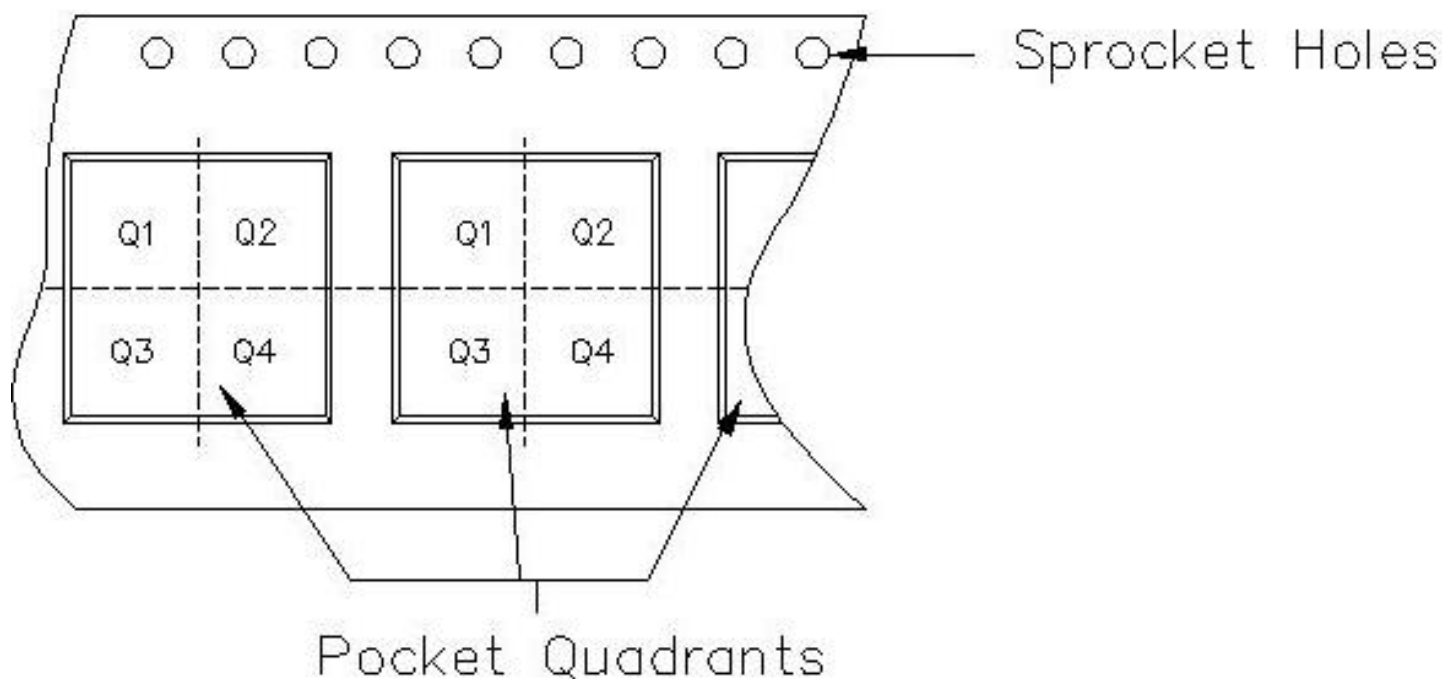
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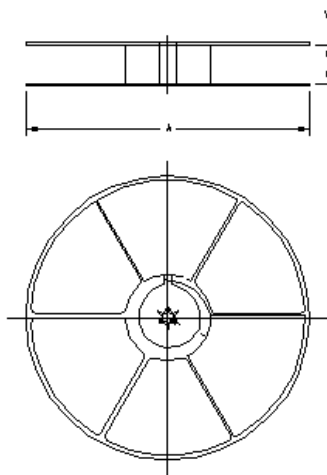
Carrier tape design is defined largely by the component length, width, and thickness.

$A_0$ = Dimension designed to accommodate the component width.
$B_0$ = Dimension designed to accommodate the component length.
$K_0$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



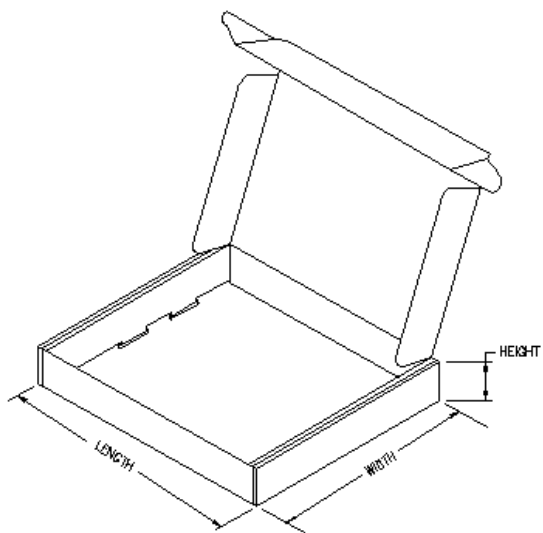
## TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLP817DGVR	DGV	24	MLA	330	12	7.0	5.6	1.6	8	12	Q1
SN74GTLP817DWR	DW	24	TAI	330	24	10.75	15.7	2.7	12	24	Q1
SN74GTLP817PWR	PW	24	MLA	330	16	6.95	8.3	1.6	8	16	Q1



## TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74GTLP817DGVR	DGV	24	MLA	338.1	340.5	20.64
SN74GTLP817DWR	DW	24	TAI	346.0	346.0	41.0
SN74GTLP817PWR	PW	24	MLA	333.2	333.2	28.58



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



## DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - Falls within JEDEC MO-153

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