

## 8-CHANNEL HALF-DUPLEX M-LVDS LINE TRANSCEIVERS

### FEATURES

- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates <sup>(1)</sup> Up to 250 Mbps; Clock Frequencies Up to 125 MHz**
- **Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **–1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise**
- **Bus Pins High Impedance When Driver Disabled or  $V_{CC} \leq 1.5$  V**
- **Independent Enables for each Driver**
- **Bus Pin ESD Protection Exceeds 8 kV**
- **Packaged in 64-Pin TSSOP (DGG)**
- **M-LVDS Bus Power Up/Down Glitch Free**

### APPLICATIONS

- **Parallel Multipoint Data and Clock Transmission Via Backplanes and Cables**
- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**
- **Cellular Base Stations**
- **Central-Office Switches**
- **Network Switches and Routers**

### DESCRIPTION

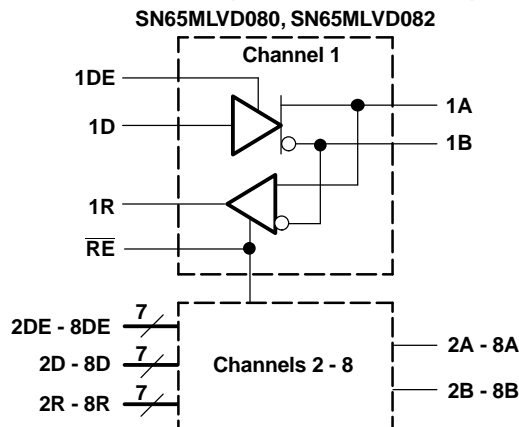
The SN65MLVD080 and SN65MLVD082 provide eight half-duplex transceivers for transmitting and receiving Multipoint-Low-Voltage Differential Signals in full compliance with the TIA/EIA-899 (M-LVDS) standard, which are optimized to operate at signaling rates up to 250 Mbps. The driver outputs have been designed to support multipoint buses presenting loads as low as 30-Ω and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

- (1) The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

The M-LVDS standard defines two types of receivers, designated as Type-1 and Type-2. Type-1 receivers (SN65MLVD080) have thresholds centered about zero with 25 mV of hysteresis to prevent output oscillations with loss of input; Type-2 receivers (SN65MLVD082) implement a failsafe by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns, complying with the M-LVDS standard to provide operation at 250 Mbps while also accommodating stubs on the bus. Receiver outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges. The M-LVDS standard allows for 32 nodes on the bus providing a high-speed replacement for RS-485 where lower common-mode can be tolerated or when higher signaling rates are needed.

The driver logic inputs and the receiver logic outputs are on separate pins rather than tied together as in some transceiver designs. The drivers have separate enables (DE) and the receivers are enabled globally through ( $\overline{RE}$ ). This arrangement of separate logic inputs, logic outputs, and enable pins allows for a listen-while-talking operation. The devices are characterized for operation from –40°C to 85°C.

### LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

PART NUMBER	RECEIVER TYPE	PACKAGE MARKING	PACKAGE/CARRIER
SN65MLVD080DGG	Type 1	MLVD080	64-Pin TSSOP/Tube
SM65MLVD080DGGR	Type 1	MLVD080	64-Pin TSSOP/Tape and Reeled
SN65MLVD082DGG	Type 2	MLVD082	64-Pin TSSOP/Tube
SM65MLVD082DGGR	Type 2	MLVD082	64-Pin TSSOP/Tape and Reeled

## PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DGG	Low-K <sup>(2)</sup>	1204.7 mW	10.5 mW/°C	576 mW
DGG	High-K <sup>(3)</sup>	1839.4 mW	16.0 mW/°C	880 mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

## THERMAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JB}$ Junction-to-board thermal resistance			41.08		°C/W
$\theta_{JC}$ Junction-to-case thermal resistance			6.78		°C/W
Device power dissipation	$V_{CC} = 3.3\text{ V}$ , $DE = V_{CC}$ , $\overline{RE} = \text{GND}$ , $C_L = 15\text{ pF}$ , $R_L = 50\ \Omega$ , 250 Mbps random data on each input		477		mW
	$V_{CC} = 3.6\text{ V}$ , $DE = V_{CC}$ , $\overline{RE} = \text{GND}$ , $C_L = 15\text{ pF}$ , $R_L = 50\ \Omega$ , 250 Mbps data on one input and 125 MHz clock on the others		854 <sup>(1)</sup>		

(1) When all channels are running at a 125-MHz clock frequency, a 250 lfm is required for a low-K board, and 150 lfm is required for a high-K board. In such applications, a TI 1:8 or dual 1:4 M-LVDS buffer is highly recommended, SN65MLVD128 or SN65MLVD129, to fan out clock signals in multiple paths.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

			SN65MLVD080, 082
Supply voltage range <sup>(2)</sup> , $V_{CC}$			–0.5 V to 4 V
Input voltage range	D, DE, $\overline{RE}$		–0.5 V to 4 V
	A, B		–1.8 V to 4 V
Output voltage range	R		–0.3 V to 4 V
	A, or B		–1.8 V to 4 V
Electrostatic discharge	Human Body Model <sup>(3)</sup>	A, B	±8 kV
		All pins	±2 kV
	Charged-Device Model <sup>(4)</sup>	All pins	±1500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range			–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	3	3.3	3.6	V
$V_{IH}$ High-level input voltage	2		$V_{CC}$	V
$V_{IL}$ Low-level input voltage	GND		0.8	V
Voltage at any bus terminal $V_A$ or $V_B$	–1.4		3.8	V
$ V_{ID} $ Magnitude of differential input voltage	0.05		$V_{CC}$	V
$T_A$ Operating free-air temperature	–40		85	°C
Maximum junction temperature			140	°C

## DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>CC</sub> Supply current	Driver only	$\overline{RE}$ and DE at V <sub>CC</sub> , R <sub>L</sub> = 50 Ω, All others open		110	140	mA
	Both disabled	$\overline{RE}$ at V <sub>CC</sub> , DE at 0 V, R <sub>L</sub> = No Load, All others open		5	8	
	Both enabled	$\overline{RE}$ at 0 V, DE at V <sub>CC</sub> , R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, All others open		140	180	
	Receiver only	$\overline{RE}$ at 0 V, DE at 0 V, C <sub>L</sub> = 15 pF, All others open		38	50	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX	UNIT
$ V_{AB} $ Differential output voltage magnitude (A, B)	See Figure 2	480		650	mV
$\Delta V_{AB} $ Change in differential output voltage magnitude between logic states (A, B)		–50		50	mV
$V_{OS(SS)}$ Steady-state common-mode output voltage (A, B)	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$ Change in steady-state common-mode output voltage between logic states (A, B)		–50		50	mV
$V_{OS(PP)}$ Peak-to-peak common-mode output voltage (A, B)				150	mV
$V_{A(OC)}$ Maximum steady-state open-circuit output voltage (A, B)	See Figure 7	0		2.4	V
$V_{B(OC)}$ Maximum steady-state open-circuit output voltage (A, B)		0		2.4	V
$V_{P(H)}$ Voltage overshoot, low-to-high level output (A, B)	See Figure 5			1.2 $V_{SS}$	V
$V_{P(L)}$ Voltage overshoot, high-to-low level output (A, B)		–0.2 $V_{SS}$			V
$I_{IH}$ High-level input current (D, DE)	$V_{IH} = 2\ \text{V to } V_{CC}$			10	$\mu\text{A}$
$I_{IL}$ Low-level input current (D, DE)	$V_{IL} = \text{GND to } 0.8\ \text{V}$			10	$\mu\text{A}$
$ I_{OS} $ Differential short-circuit output current magnitude (A, B)	See Figure 4			24	mA
$C_i$ Input capacitance (D, DE)	$V_i = 0.4 \sin(30E6\pi t) + 0.5\ \text{V}$ <sup>(3)</sup>		5		pF

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) HP4194A impedance analyzer (or equivalent)

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$	Positive-going differential input voltage threshold (A, B)	Type 1			50	mV
		Type 2			150	
$V_{IT-}$	Negative-going differential input voltage threshold (A, B)	Type 1	See Figure 9, Table 1 and Table 2		–50	mV
		Type 2			50	
$V_{HYS}$	Differential input voltage hysteresis, ( $V_{IT+} - V_{IT-}$ ) (A, B)	Type 1			25	mV
		Type 2			0	
$V_{OH}$	High-level output voltage (R)	$I_{OH} = -8\text{ mA}$	2.4			V
$V_{OL}$	Low-level output voltage (R)	$I_{OL} = 8\text{ mA}$			0.4	V
$I_{IH}$	High-level input current ( $\overline{RE}$ )	$V_{IH} = 2\text{ V to }V_{CC}$	–10			$\mu\text{A}$
$I_{IL}$	Low-level input current ( $\overline{RE}$ )	$V_{IL} = \text{GND to }0.8\text{ V}$	–10			$\mu\text{A}$
$I_{OZ}$	High-impedance output current (R)	$V_O = 0\text{ V or }V_{CC}$	–10		15	$\mu\text{A}$

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

## BUS INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_A$	Receiver or transceiver with driver disabled input current	$V_A = 3.8\text{ V}, V_B = 1.2\text{ V}$	0		32	$\mu\text{A}$
		$V_A = 0\text{ V or }2.4\text{ V}, V_B = 1.2\text{ V}$	–20		20	
		$V_A = -1.4\text{ V}, V_B = 1.2\text{ V}$	–32		0	
$I_B$	Receiver or transceiver with driver disabled input current	$V_B = 3.8\text{ V}, V_A = 1.2\text{ V}$	0		32	$\mu\text{A}$
		$V_B = 0\text{ V or }2.4\text{ V}, V_A = 1.2\text{ V}$	–20		20	
		$V_B = -1.4\text{ V}, V_A = 1.2\text{ V}$	–32		0	
$I_{AB}$	Receiver or transceiver with driver disabled differential input current ( $I_A - I_B$ )	$V_A = V_B, 1.4 \leq V_A \leq 3.8\text{ V}$	–4		4	$\mu\text{A}$
$I_{A(OFF)}$	Receiver or transceiver power-off input current	$V_A = 3.8\text{ V}, V_B = 1.2\text{ V}, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$	0		32	$\mu\text{A}$
		$V_A = 0\text{ V or }2.4\text{ V}, V_B = 1.2\text{ V}, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$	–20		20	
		$V_A = -1.4\text{ V}, V_B = 1.2\text{ V}, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$	–32		0	
$I_{B(OFF)}$	Receiver or transceiver power-off input current	$V_B = 3.8\text{ V}, V_A = 1.2\text{ V}, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$	0		32	$\mu\text{A}$
		$V_B = 0\text{ V or }2.4\text{ V}, V_A = 1.2\text{ V}, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$	–20		20	
		$V_B = -1.4\text{ V}, V_A = 1.2\text{ V}, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$	–32		0	
$I_{AB(OFF)}$	Receiver input or transceiver power-off differential input current ( $I_{A(OFF)} - I_{B(OFF)}$ )	$V_A = V_B, 0\text{ V} \leq V_{CC} \leq 1.5\text{ V}, -1.4 \leq V_A \leq 3.8\text{ V}$	–4		4	$\mu\text{A}$
$C_A$	Transceiver with driver disabled input capacitance	$V_A = 0.4 \sin(30E6\pi t) + 0.5\text{ V}^{(2)}, V_B = 1.2\text{ V}$		5		pF
$C_B$	Transceiver with driver disabled input capacitance	$V_B = 0.4 \sin(30E6\pi t) + 0.5\text{ V}^{(2)}, V_A = 1.2\text{ V}$		5		pF
$C_{AB}$	Transceiver with driver disabled differential input capacitance	$V_{AB} = 0.4 \sin(30E6\pi t)\text{ V}^{(2)}$			3	pF
$C_{A/B}$	Transceiver with driver disabled input capacitance balance, ( $C_A/C_B$ )		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	See Figure 5	1	1.5	2.4	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
$t_r$	Differential output signal rise time		1		2	ns
$t_f$	Differential output signal fall time		1		2	ns
$t_{sk(o)}$	Output skew				350	ps
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )			0	150	ps
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>				600	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) <sup>(3)</sup>	100 MHz clock input <sup>(4)</sup>			4	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter, rms				45	ps
$t_{jit(det)}$	Deterministic jitter	200 Mbps 2 <sup>15</sup> -1 PRBS input <sup>(5)</sup>			150	ps
$t_{jit(pp)}$	Peak-to-peak jitter <sup>(2)(6)</sup>				190	ps
$t_{PZH}$	Enable time, high-impedance-to-high-level output	See Figure 6			7	ns
$t_{PZL}$	Enable time, high-impedance-to-low-level output				7	ns
$t_{PHZ}$	Disable time, high-level-to-high-impedance output				7	ns
$t_{PLZ}$	Disable time, low-level-to-high-impedance output				7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2)  $t_{sk(pp)}$  is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4)  $t_r = t_f = 0.5$  ns (10% to 90%), measured over 30 k samples.

(5)  $t_r = t_f = 0.5$  ns (10% to 90%), measured over 100 k samples.

(6) Peak-to-peak jitter includes jitter due to pulse skew ( $t_{sk(p)}$ ).

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$ , See <a href="#">Figure 10</a>	2	4	6	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output		2	4	6	ns
$t_r$	Output signal rise time		1		2.3	ns
$t_f$	Output signal fall time		1		2.3	ns
$t_{sk(o)}$	Output skew				350	ps
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )			50	350	ps
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>				1	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) <sup>(3)</sup>	100 MHz clock input <sup>(4)</sup>			7	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter, rms				110	ps
$t_{jit(det)}$	Deterministic jitter	Type 1			550	ps
		Type 2			480	ps
$t_{jit(pp)}$	Peak-to-peak jitter <sup>(3)(6)</sup>	Type 1			720	ps
		Type 2			660	ps
$t_{PZH}$	Enable time, high-impedance-to-high-level output	$C_L = 15\text{ pF}$ , See <a href="#">Figure 11</a>			30	ns
$t_{PZL}$	Enable time, high-impedance-to-low-level output				30	ns
$t_{PHZ}$	Disable time, high-level-to-high-impedance output				18	ns
$t_{PLZ}$	Disable time, low-level-to-high-impedance output				28	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2)  $t_{sk(pp)}$  is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4)  $V_{ID} = 200\text{ mV}_{pp}$  ('080),  $V_{ID} = 400\text{ mV}_{pp}$  ('082),  $V_{cm} = 1\text{ V}$ ,  $t_r = t_f = 0.5\text{ ns}$  (10% to 90%), measured over 30 k samples.

(5)  $V_{ID} = 200\text{ mV}_{pp}$  ('080),  $V_{ID} = 400\text{ mV}_{pp}$  ('082),  $V_{cm} = 1\text{ V}$ ,  $t_r = t_f = 0.5\text{ ns}$  (10% to 90%), measured over 100 k samples.

(6) Peak-to-peak jitter includes jitter due to pulse skew ( $t_{sk(p)}$ ).

## PARAMETER MEASUREMENT INFORMATION

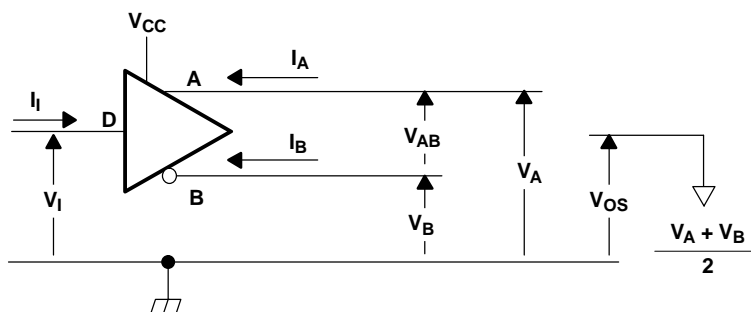
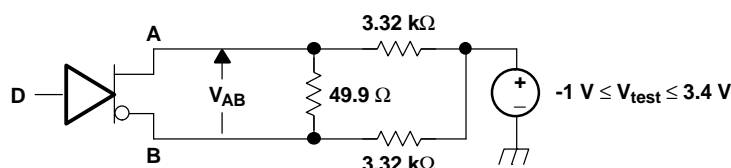
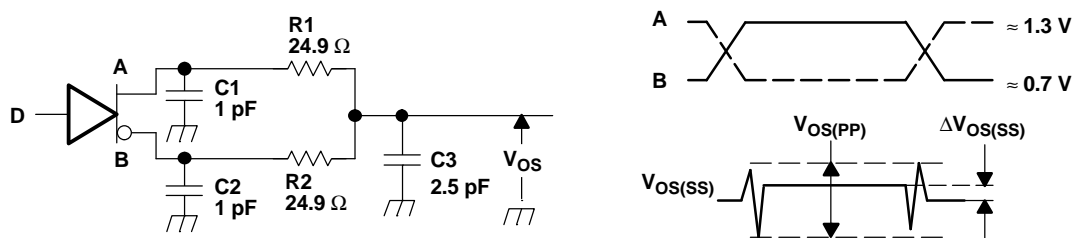


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- R1 and R2 are metal film, surface mount,  $\pm 1\%$ , and located within 2 cm of the D.U.T.
- The measurement of  $V_{OS(PP)}$  is made on test equipment with a  $-3$  dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

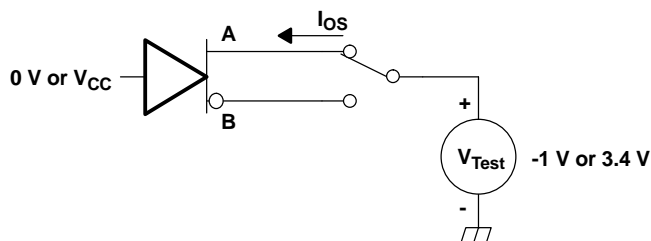
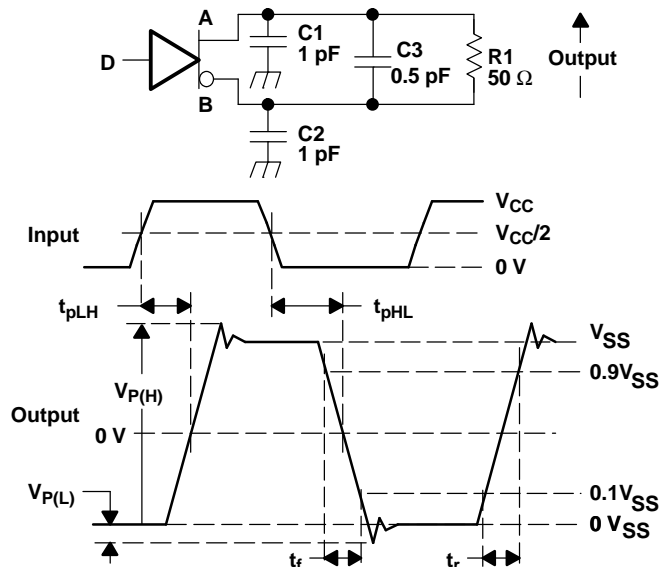


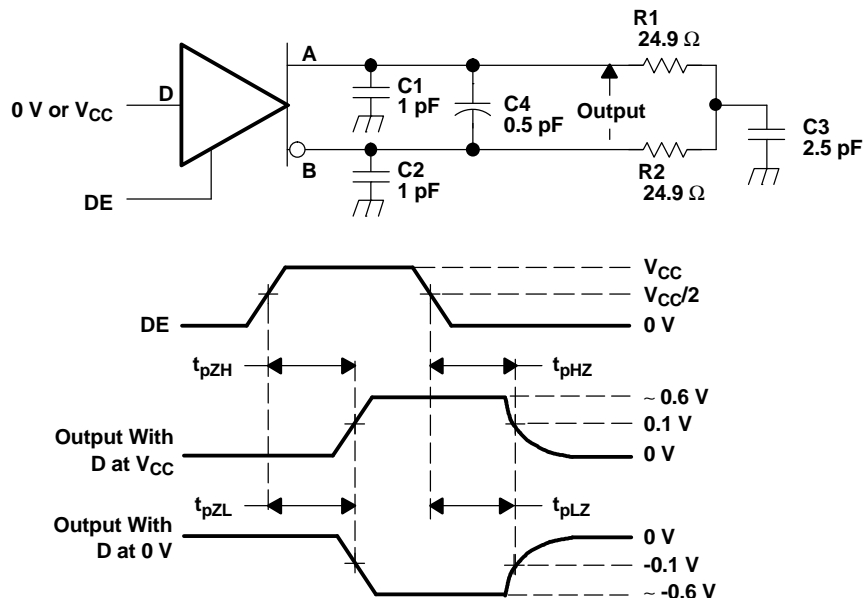
Figure 4. Driver Short-Circuit Test Circuit

## PARAMETER MEASUREMENT INFORMATION (continued)



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- The measurement is made on test equipment with a  $-3$  dB bandwidth of at least 1 GHz.

**Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- The measurement is made on test equipment with a  $-3$  dB bandwidth of at least 1 GHz.

**Figure 6. Driver Enable and Disable Time Circuit and Definitions**



## PARAMETER MEASUREMENT INFORMATION (continued)

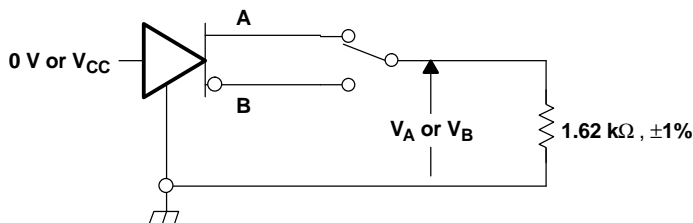
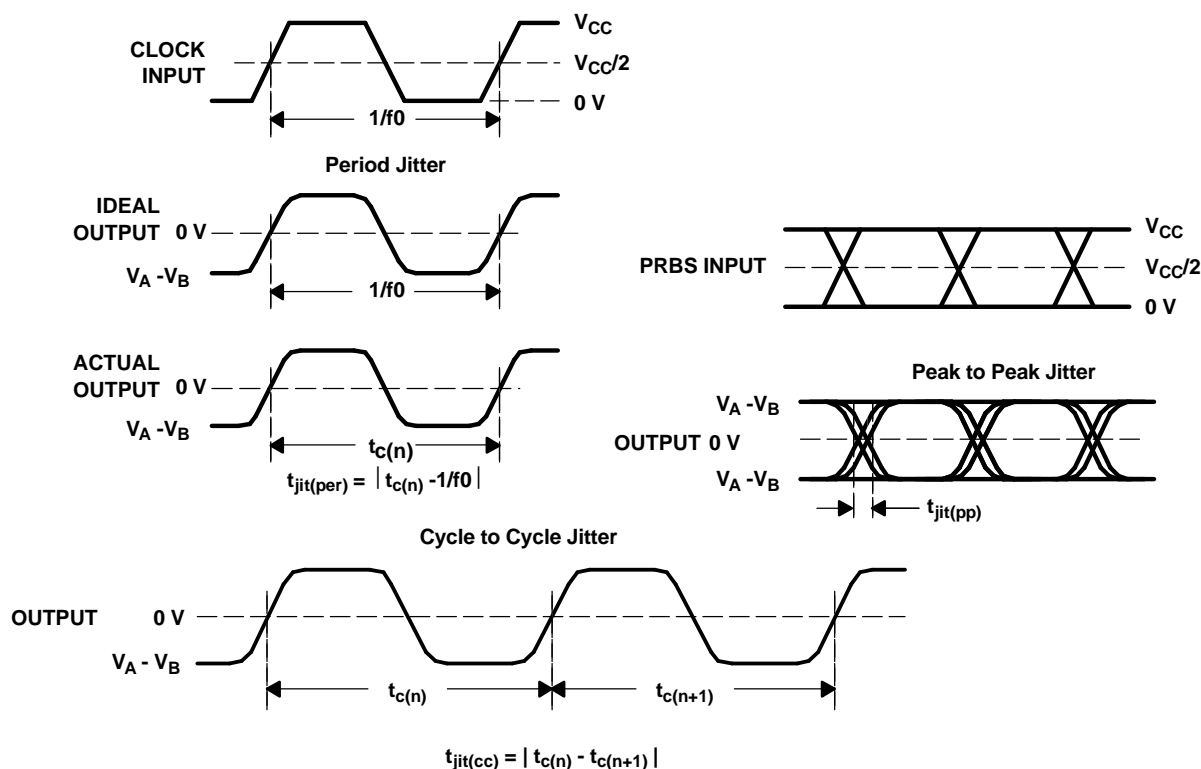


Figure 7. Maximum Steady State Output Voltage



- All input pulses are supplied by an Agilent 8304A Stimulus System with plug-in TBD.
- The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50 ±1% duty cycle clock input.
- Peak-to-peak jitter and deterministic jitter are measured using a 200 Mbps 2<sup>15</sup>–1 PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

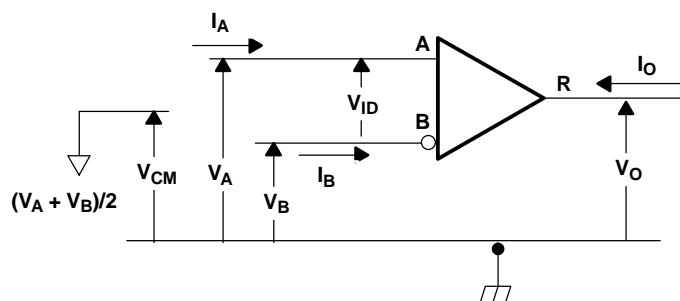


Figure 9. Receiver Voltage and Current Definitions

**Table 1. Type-1 Receiver Input Threshold Test Voltages**

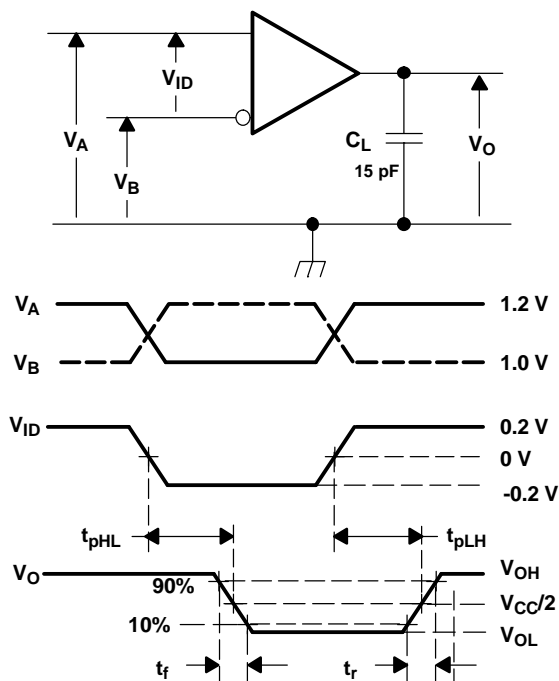
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER OUTPUT <sup>(1)</sup>
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.350	0.050	3.375	H
3.350	3.400	–0.050	3.375	L
–1.350	–1.400	0.050	–1.375	H
–1.400	–1.350	–0.050	–1.375	L

(1) H= high level, L = low level, output state assumes receiver is enabled ( $\overline{RE} = L$ )

**Table 2. Type-2 Receiver Input Threshold Test Voltages**

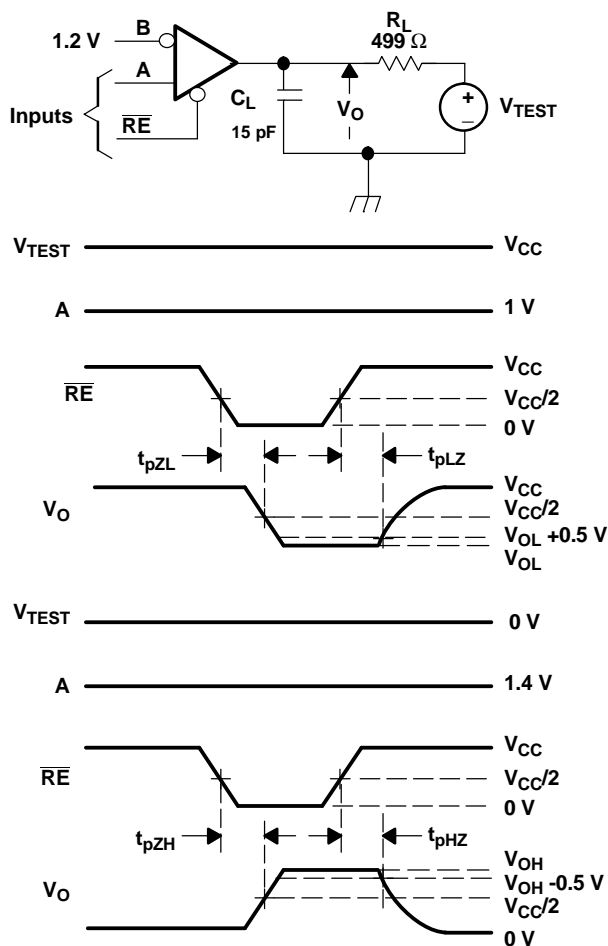
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER OUTPUT <sup>(1)</sup>
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.250	0.150	3.325	H
3.400	3.350	0.050	3.375	L
–1.250	–1.400	0.150	–1.325	H
–1.350	–1.400	0.050	–1.375	L

(1) H= high level, L = low level, output state assumes receiver is enabled ( $\overline{RE} = L$ )



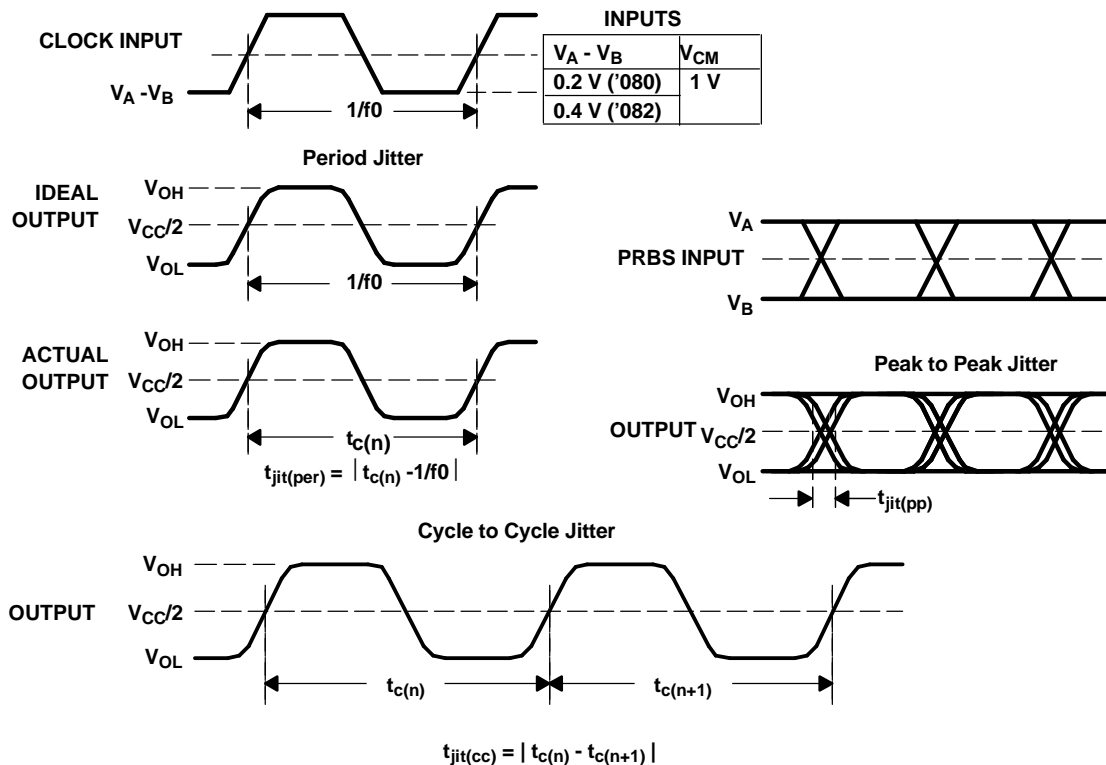
- All input pulses are supplied by a generator having the following characteristics:  $t_f$  or  $t_r \leq 1 \text{ ns}$ , frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .  $C_L$  is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

**Figure 10. Receiver Timing Test Circuit and Waveforms**



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- $R_L$  is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- $C_L$  is the instrumentation and fixture capacitance within 2 cm of the DUT and  $\pm 20\%$ . The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

**Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms**



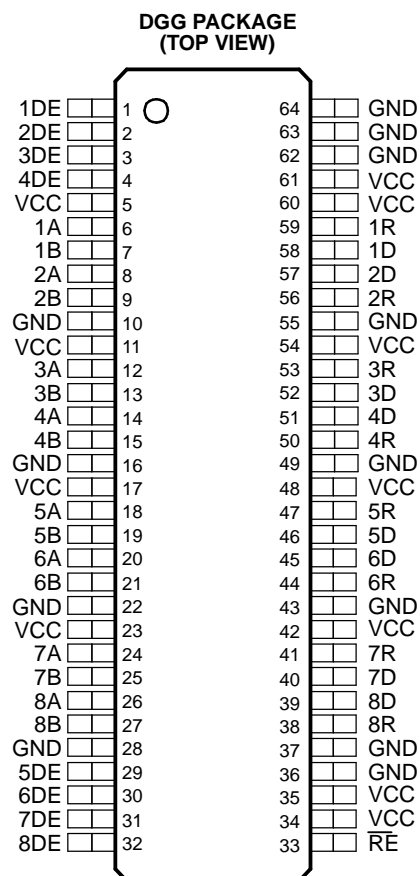
- All input pulses are supplied by an Agilent 8304A Stimulus System with plug-in TBD.
- The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50 ±1% duty cycle clock input.
- Peak-to-peak jitter and deterministic jitter are measured using a 200 Mbps 2<sup>15</sup>–1 PRBS input.

**Figure 12. Receiver Jitter Measurement Waveforms**

**Table 3. Terminal Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
1D–8D	58, 57, 52, 51, 46, 45, 40, 39	Input	Data inputs for drivers
1R–8R	59, 56, 53, 50, 47, 44, 41, 38	Output	Data output for receivers
1A–8A	6, 8, 12, 14, 18, 20, 24, 26	Bus I/O	M-LVDS bus noninverting input/output
1B–8B	7, 9, 13, 15, 19, 21, 25, 27	Bus I/O	M-LVDS bus inverting input/output
GND	10, 16, 22, 28, 36, 37, 43, 49, 55, 62, 63, 64	Power	Circuit ground
V <sub>CC</sub>	5, 11, 17, 23, 34, 35, 42, 48, 54, 60, 61	Power	Supply voltage
$\overline{RE}$	33	Input	Receiver enable, active low, enables all receivers
1DE–8DE	1, 2, 3, 4, 29, 30, 31, 32	Input	Driver enable, active high, individual enables

## PIN ASSIGNMENTS



## DEVICE FUNCTION TABLE

**RECEIVER (080)**

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	RE	R
$V_{ID} \geq 50 \text{ mV}$	L	H
$-50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?
$V_{ID} \leq -50 \text{ mV}$	L	L
X	H	Z
X	Open	Z
Open Circuit	L	?

**RECEIVER (082)**

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	RE	R
$V_{ID} \geq 150 \text{ mV}$	L	H
$50 \text{ mV} < V_{ID} < 150 \text{ mV}$	L	?
$V_{ID} \leq 50 \text{ mV}$	L	L
X	H	Z
X	Open	Z
Open Circuit	L	L

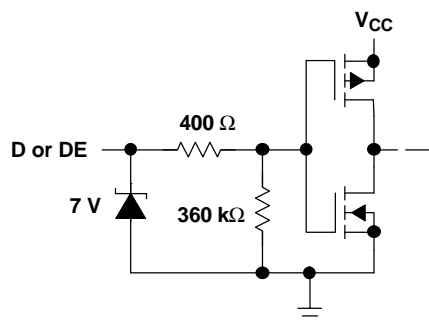
## DRIVERS

INPUT	ENABLE	OUTPUTS	
D	DE	A OR Y	B OR Z
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

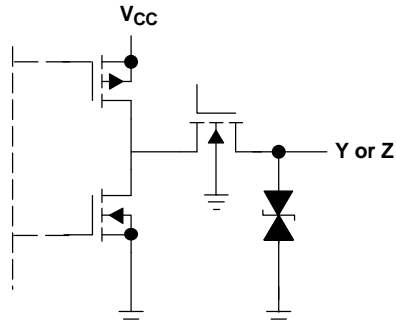
H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

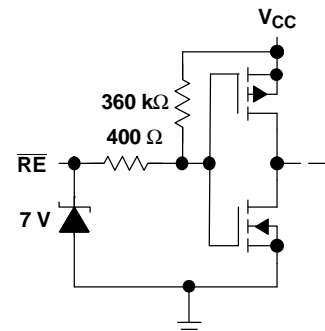
DRIVER INPUT AND DRIVER ENABLE



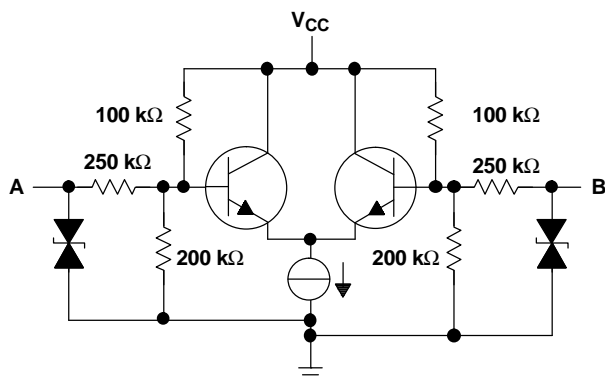
DRIVER OUTPUT



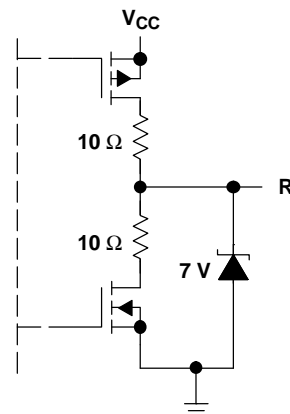
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



## TYPICAL CHARACTERISTICS

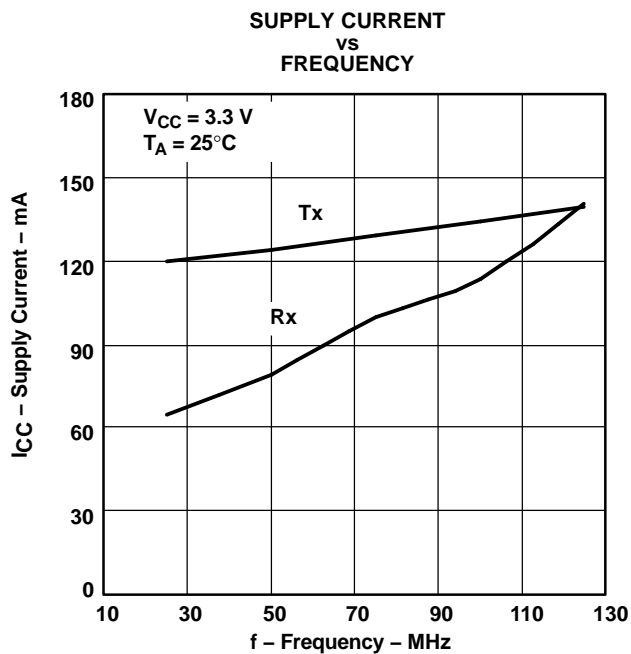


Figure 13.

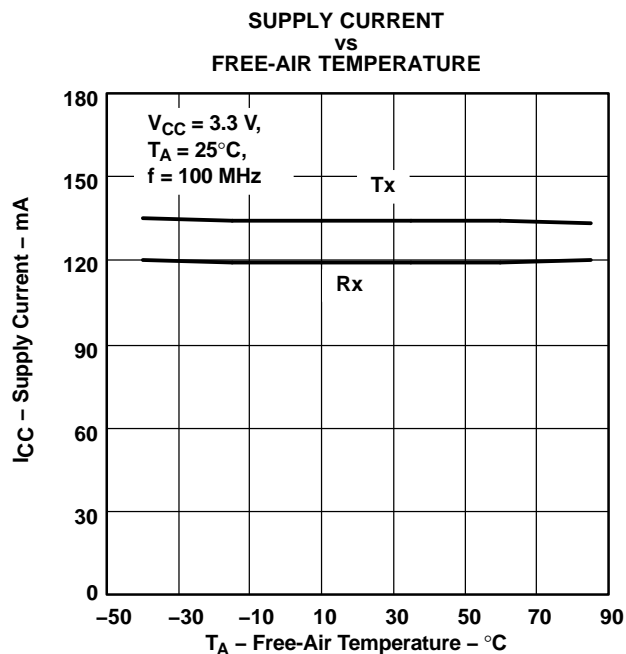


Figure 14.

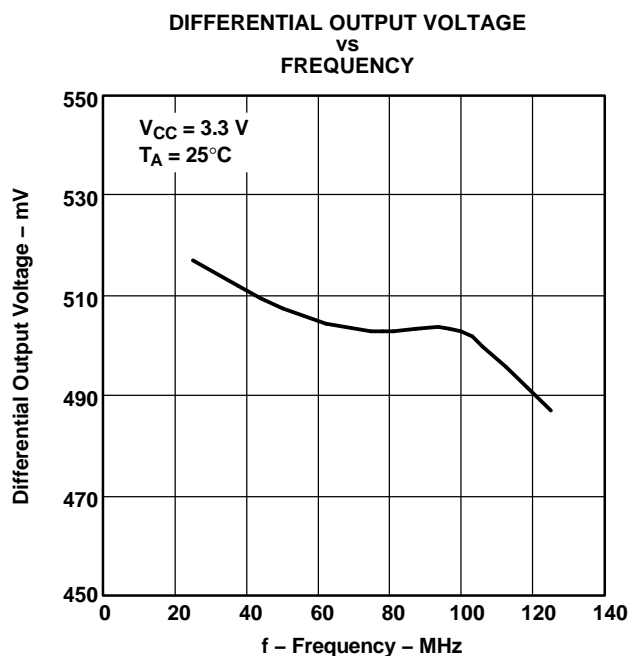


Figure 15.

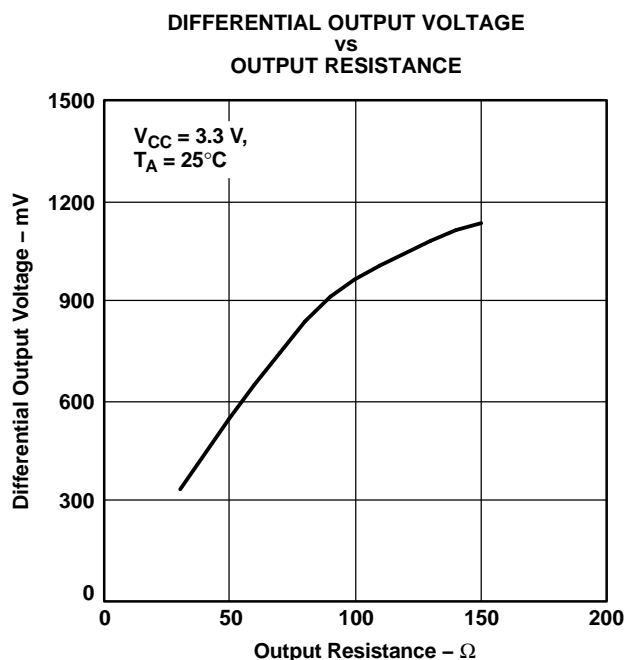
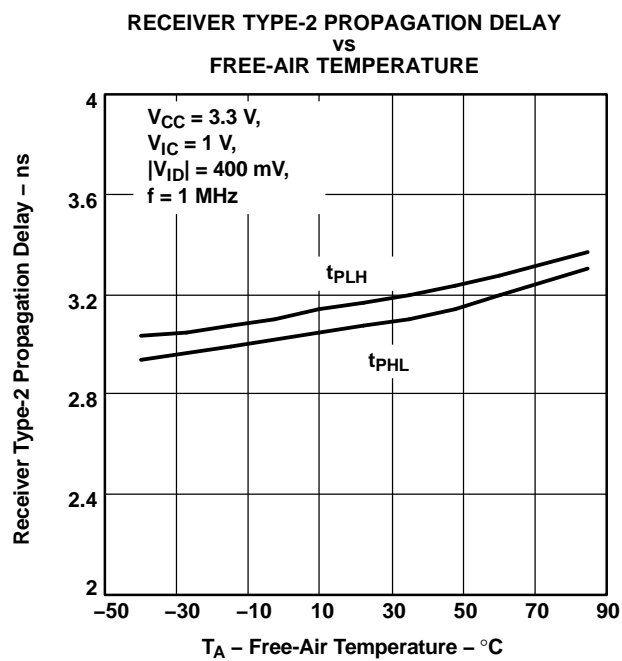
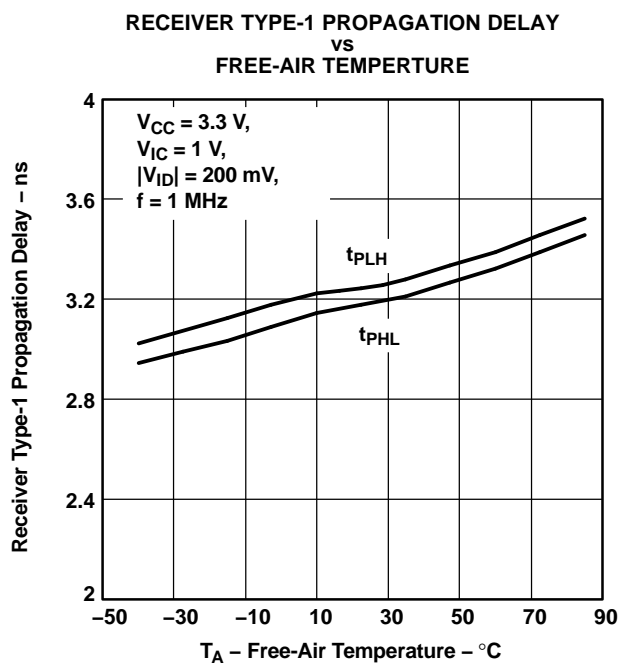
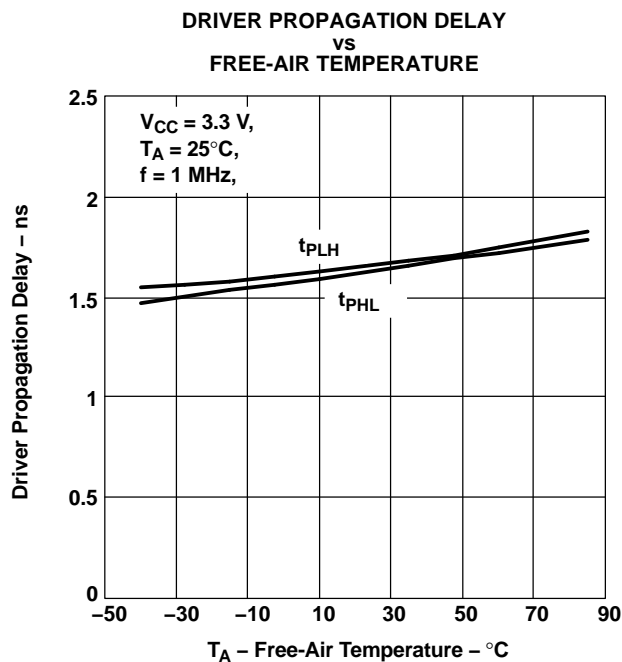
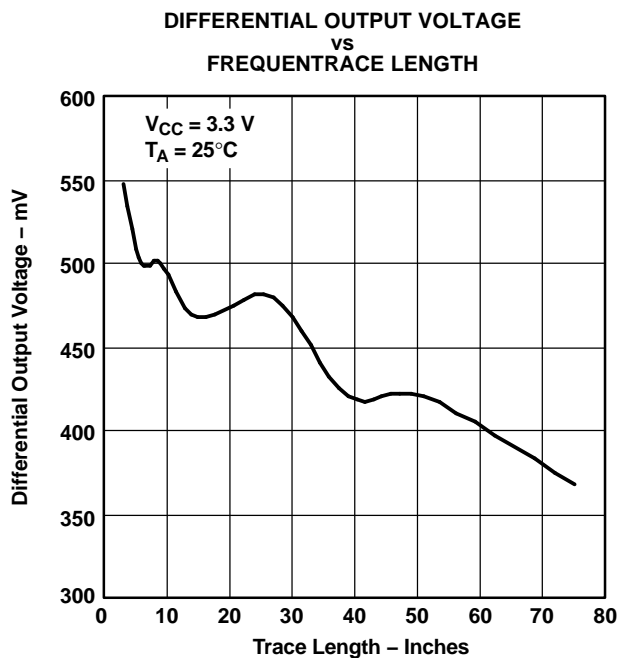


Figure 16.

## TYPICAL CHARACTERISTICS (continued)





## TYPICAL CHARACTERISTICS (continued)

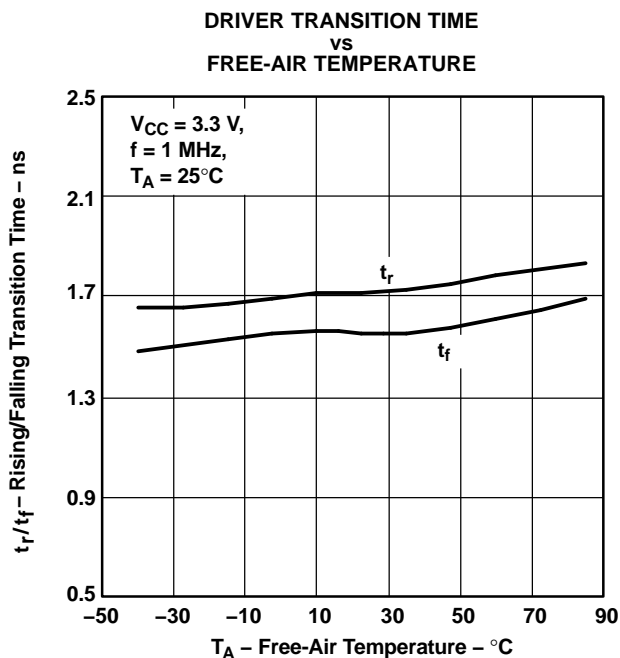


Figure 21.

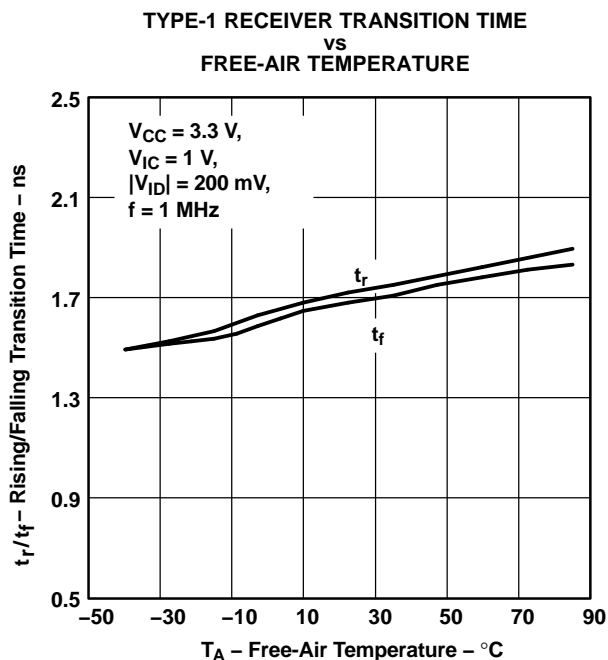


Figure 22.

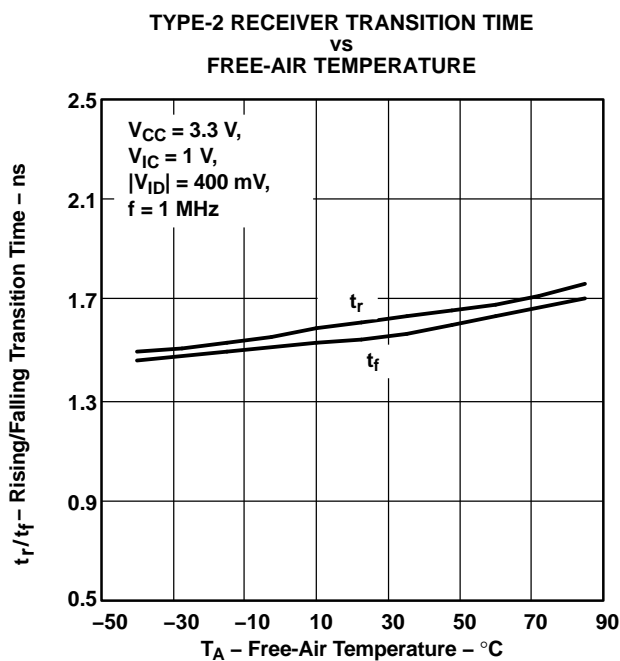


Figure 23.

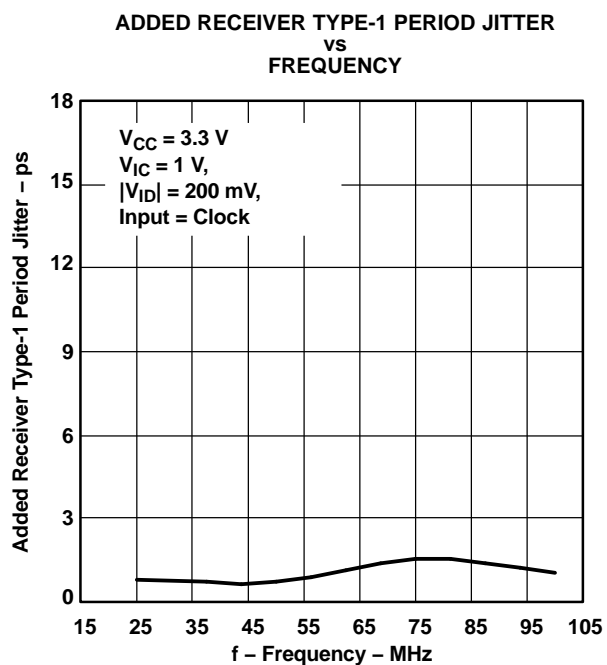


Figure 24.

## TYPICAL CHARACTERISTICS (continued)

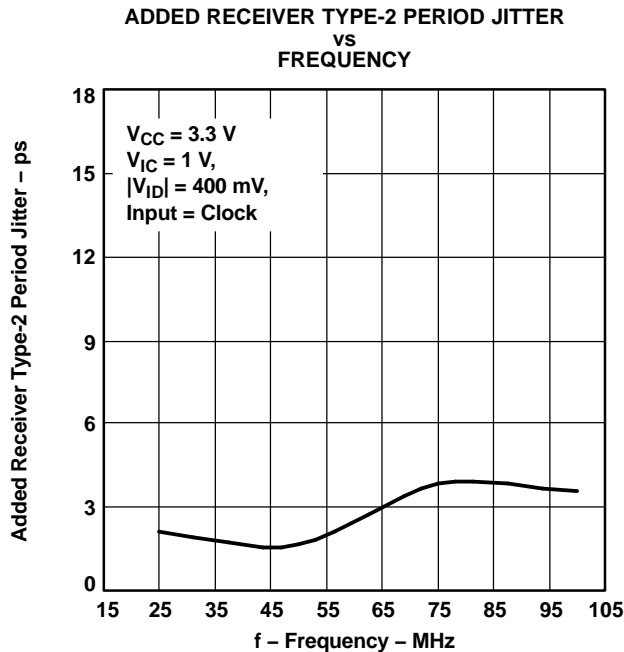


Figure 25.

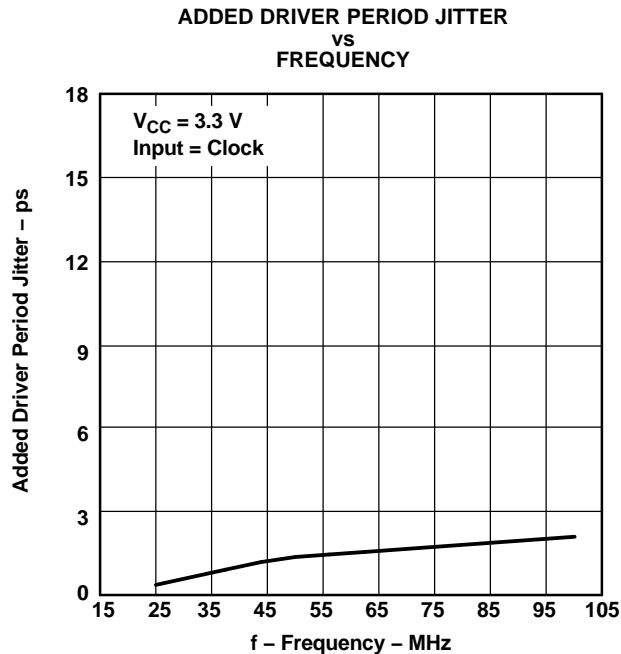


Figure 26.

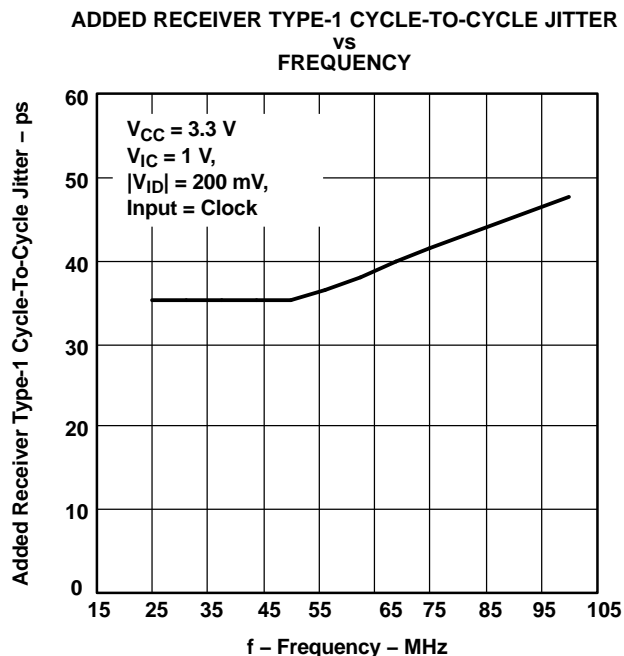


Figure 27.

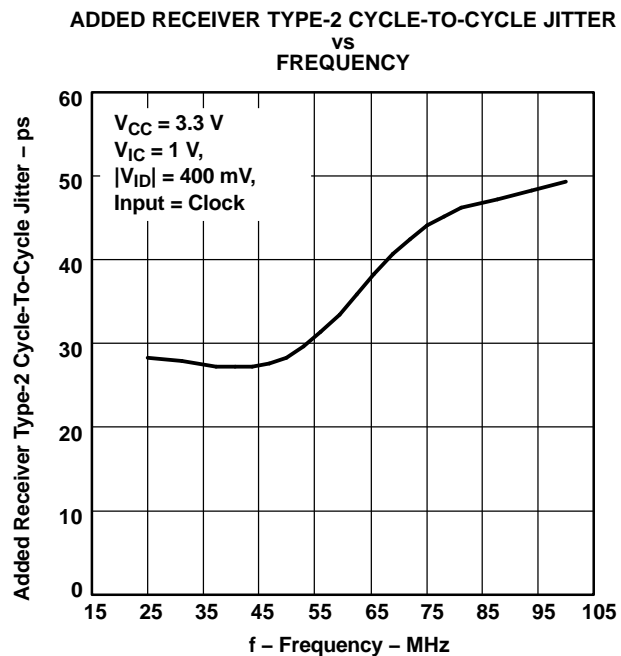


Figure 28.

## TYPICAL CHARACTERISTICS (continued)

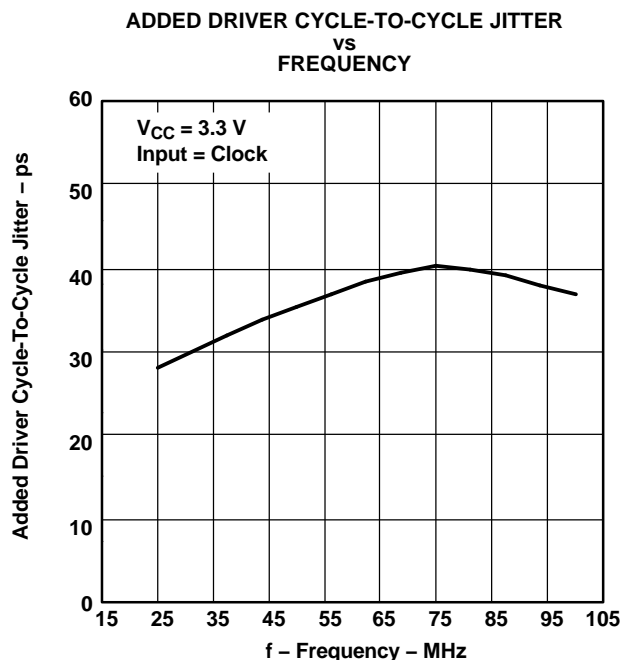


Figure 29.

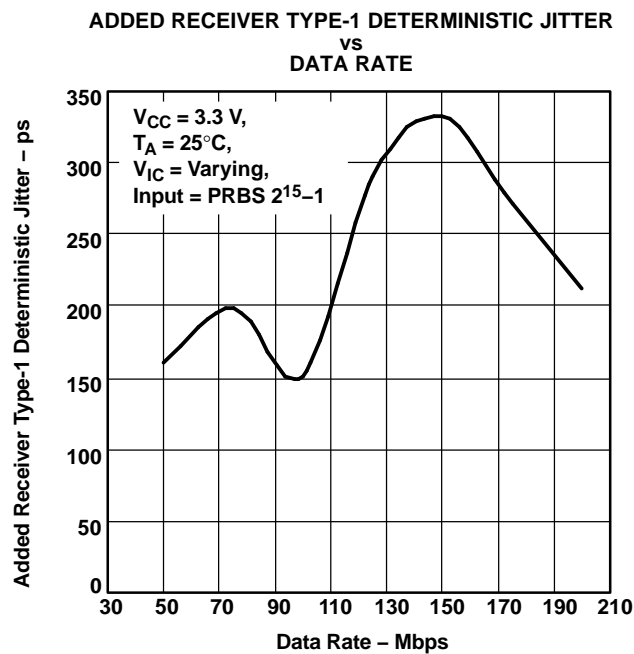


Figure 30.

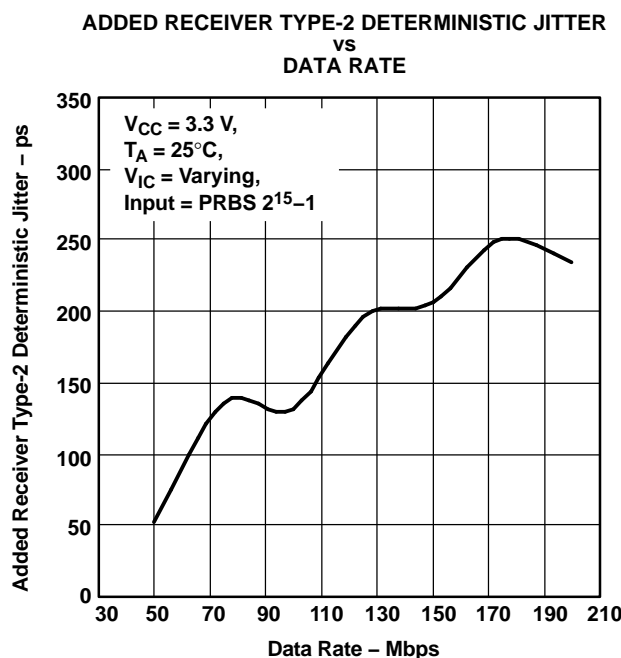


Figure 31.

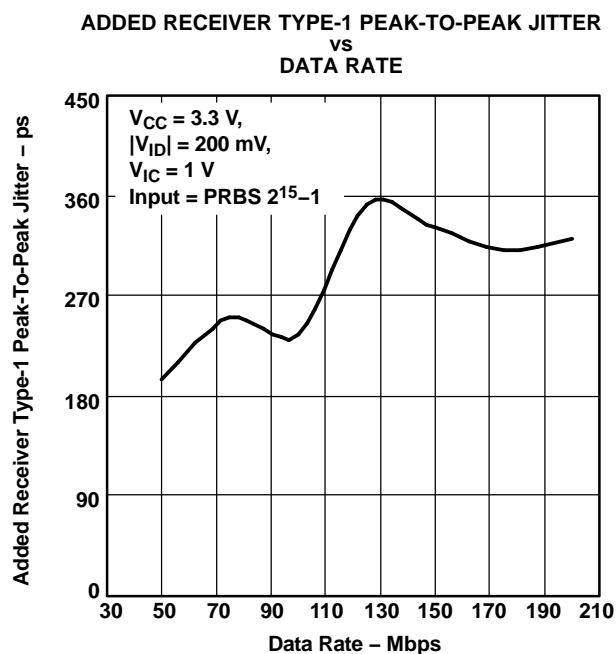


Figure 32.

## TYPICAL CHARACTERISTICS (continued)

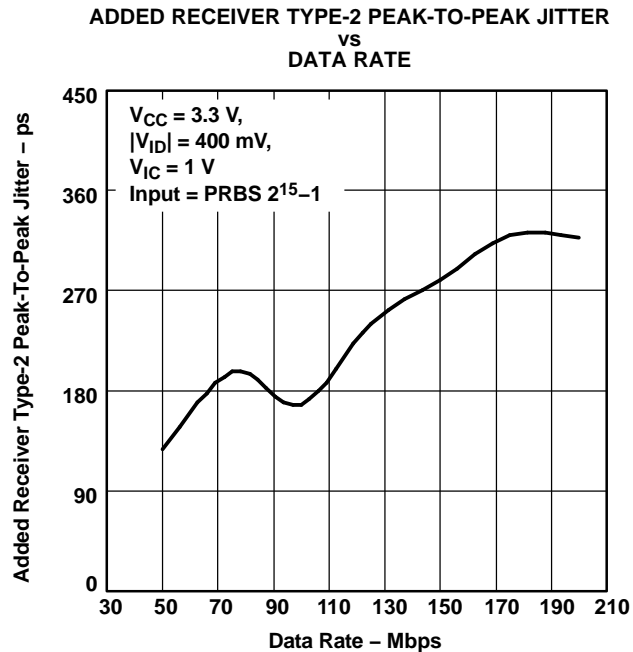


Figure 33.

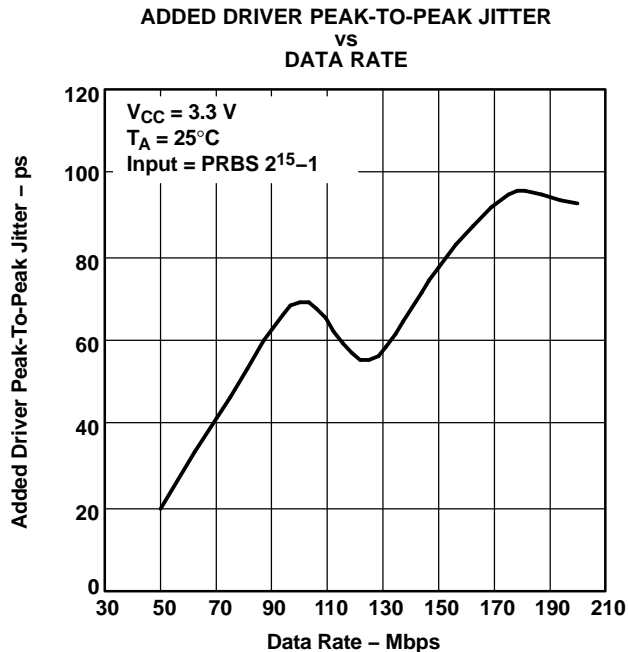


Figure 34.

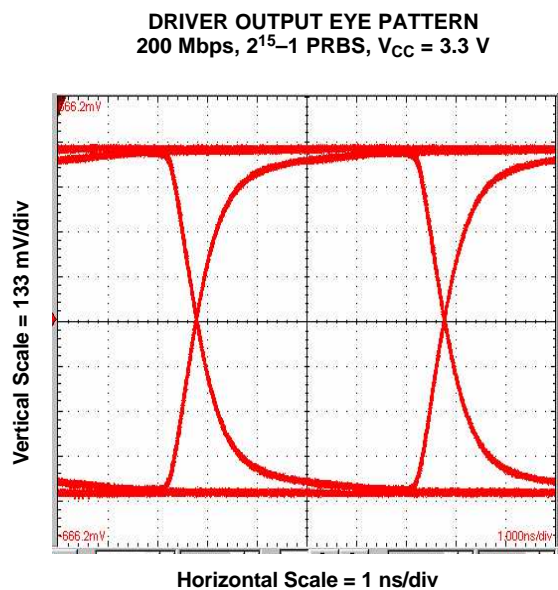


Figure 35.

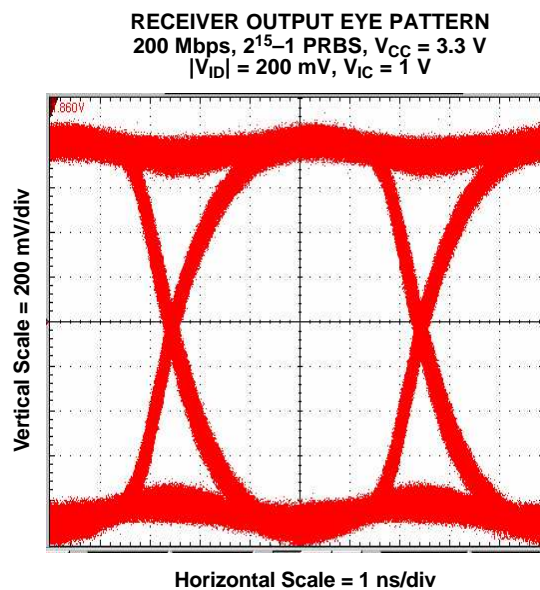


Figure 36.



**APPLICATION INFORMATION (continued)**

$t_{sk(o)Source} = 2.0 \text{ ns}$  – Output skew of data processing unit; any skew between data bits, or clock and data bits

$t_{sk(p-p)DRVR} = 0.6 \text{ ns}$  – Driver part-to-part skew of the SN65MLVD082

$t_{sk(flight)BP} = 0.4 \text{ ns}$  – Skew of propagation delay on the backplane between data and clock

$t_{sk(p-p)RCVR} = 1.0 \text{ ns}$  – Receiver part-to-part skew of the SN65MLVD082

The 238-MHz maximum operating speed calculated above was determined based on data and clock skews only. Another important consideration when calculating the maximum operating speed is output transition time. Transition-time-limited operating speed can be calculated from the following formula:

$$f = 45\% \times \frac{1}{2 \times t_{transition}} \quad (1)$$

Using the typical transition time of the SN65MLVD082 of 1.4 ns, a transition-time-limited operating frequency of 170 MHz can be supported.

In addition to the high operating frequencies of SSSC that can be ensured, the SN65MLVD082 presents other benefits as other M-LVDS bus transceivers can provide:

- Robust system operation due to common mode noise cancellation using a low voltage differential receiver
- Low EMI radiation noise due to differential signaling improves signal integrity through the backplane
- A singly terminated transmission line is easy to design and implement
- Low power consumption in both active and idle modes minimizes thermal concerns on each module

In dense backplane design, these benefits are important for improving the performance of the whole system.

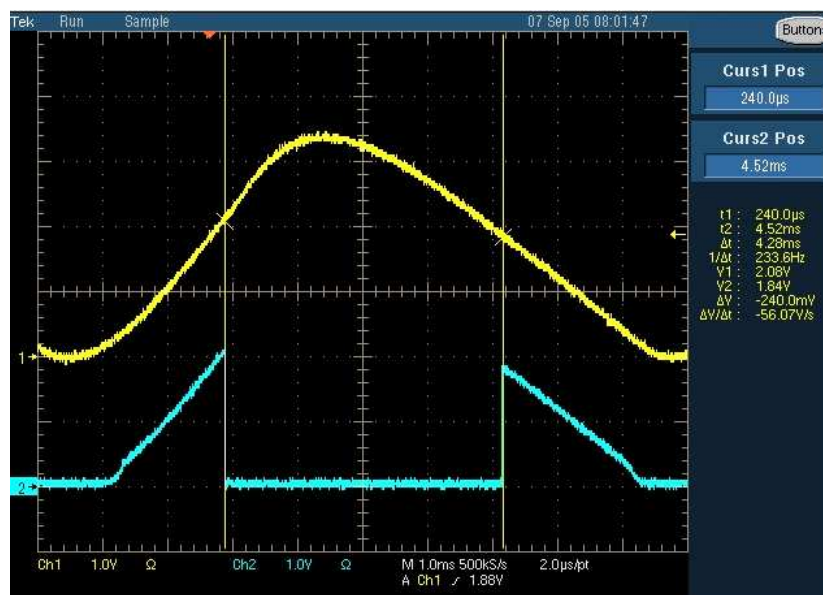
A similar result can be achieved with the SN65MLVD080.

## APPLICATION INFORMATION (continued)

### LIVE INSERTION/GLITCH-FREE POWER UP/DOWN

The SN65MLVD080/082 family of products offered by Texas Instruments provides a glitch-free powerup/down feature that prevents the M-LVDS outputs of the device from turning on during a powerup or powerdown event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and VCC is ramping.

While the M-LVDS interface for these devices is glitch free on powerup/down, the receiver output structure is not. [Figure 38](#) shows the performance of the receiver output pin, R (CHANNEL 2), as Vcc (CHANNEL 1) is ramped.



**Figure 38. M-LVDS Receiver Output: VCC (CHANNEL 1), R Pin (CHANNEL 2)**

The glitch on the R pin is independent of the  $\overline{RE}$  voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until VCC has reached a steady state value.

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65MLVD080DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD080DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD080DGGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD080DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD082DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD082DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD082DGGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD082DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

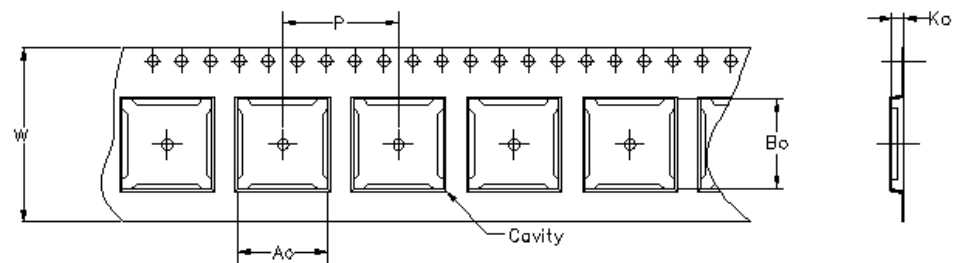
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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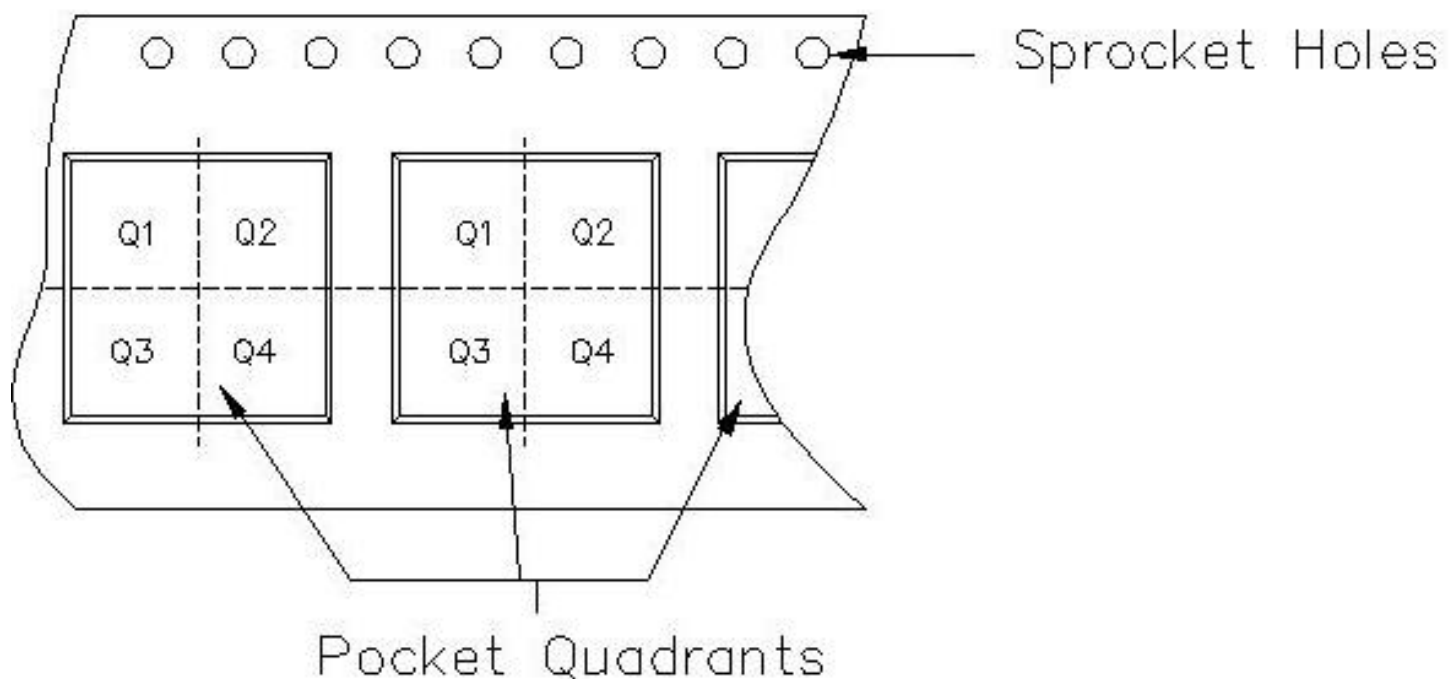
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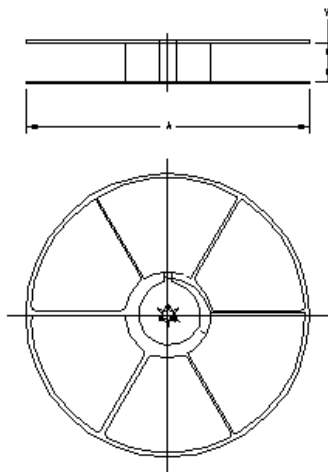
Carrier tape design is defined largely by the component length, width, and thickness.

$A_0$ = Dimension designed to accommodate the component width.
$B_0$ = Dimension designed to accommodate the component length.
$K_0$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



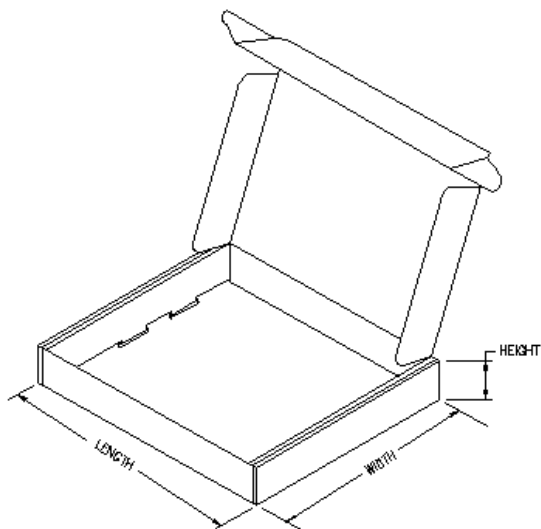
## TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD080DGGR	DGG	64	TAI	330	24	8.4	17.3	1.7	12	24	Q1
SN65MLVD082DGGR	DGG	64	TAI	330	24	8.4	17.3	1.7	12	24	Q1



## TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65MLVD080DGGR	DGG	64	TAI	0.0	0.0	0.0
SN65MLVD082DGGR	DGG	64	TAI	0.0	0.0	0.0



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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