

MULTIPOINT-LVDS LINE DRIVER AND RECEIVER

FEATURES

- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates ⁽¹⁾ Up to 100 Mbps, Clock Frequencies up to 50 MHz**
- **Type-1 Receivers Incorporate 25 mV of Hysteresis (200A, 202A)**
- **Type-2 Receivers Provide an Offset(100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions (204A, 205A)**
- **Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange**
- **Power Up/Down Glitch Free**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **–1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise**
- **Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V**
- **200-Mbps Devices Available (SN65MLVD201, 203, 206, 207)**
- **Bus Pin ESD Protection Exceeds 8 kV**
- **Package in 8-Pin SOIC (200A, 204A) and 14-Pin SOIC (202A, 205A)**
- **Improved Alternatives to the SN65MLVD200, 202, 204, and 205**

APPLICATIONS

- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**
 - **Backplane or Cabled Multipoint Data and Clock Transmission**
 - **Cellular Base Stations**
 - **Central-Office Switches**
 - **Network Switches and Routers**
- (1) The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the nits bps (bits per second).

DESCRIPTION

The SN65MLVD200A, 202A, 204A, and 205A are multipoint-low-voltage differential (M-LVDS) line drivers and receivers, which are optimized to operate at signaling rates up to 100 Mbps. All parts comply with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of –1 V to 3.4 V. The Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type-2 receivers include an offset threshold to provide a known output state under open-circuit, idle-bus, and other fault conditions.

The SN65MLVD200A, 202A, 204A, and 205A have enhancements over their predecessors. Improved features include better controlled slew rate on the driver output to help minimize reflections while improving overall signal integrity (SI) resulting in better jitter performance. Additionally, 8-kV ESD protection on the bus pins for more robustness. The same footprint definition was maintained making for an easy drop-in replacement for a system performance upgrade.

The devices are characterized for operation from –40°C to 85°C.



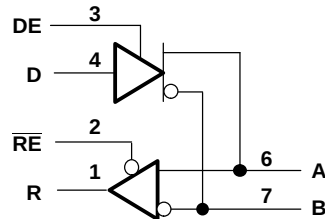
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



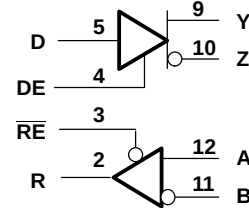
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM (POSITIVE LOGIC)

SN65MLVD200A, SN65MLVD204A



SN65MLVD202A, SN65MLVD205A



ORDERING INFORMATION

PART NUMBER ⁽¹⁾	FOOTPRINT	RECEIVER TYPE	PACKAGE MARKING
SN65MLVD200AD	SN75176	Type 1	MF200A
SM65MLVD202AD	SN75ALS180	Type 1	MLVD202A
SN65MLVD204AD	SN75176	Type 2	MF204A
SM65MLVD205AD	SN75ALS180	Type 2	MLVD205A

(1) Available tape and reeled. To order a tape and reeled part, add the suffix R to the part number (e.g., SN65MLVD200ADR).

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D(8)	532 mW	4.6 mW/ $^\circ\text{C}$	254 mW
D(14)	940 mW	8.2 mW/ $^\circ\text{C}$	450 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

			SN65MLVD200A, 202A, 204A, and 205A
Supply voltage range ⁽²⁾ , V_{CC}			–0.5 V to 4 V
Input voltage range	D, DE, $\overline{RE}$		–0.5 V to 4 V
	A, B (200A, 204A)		–1.8 V to 4 V
	A, B (202A, 205A)		–4 V to 6 V
Output voltage range	R		–0.3 V to 4 V
	Y, Z, A, or B		–1.8 V to 4 V
Electrostatic discharge	Human Body Model ⁽³⁾	A, B, Y, and Z	±8 kV
		All pins	±4 kV
	Charged-Device Model ⁽⁴⁾	All pins	±1500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range			–65 $^\circ\text{C}$ to 150 $^\circ\text{C}$

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
	Voltage at any bus terminal V_A , V_B , V_Y or V_Z	–1.4		3.8	V
$ V_{ID} $	Magnitude of differential input voltage	0.05		V_{CC}	V
R_L	Differential load resistance	30	50		Ω
$1/t_{UI}$	Signaling rate			100	Mbps
T_A	Operating free-air temperature	–40		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{CC}	Supply current	Driver only		13	22	mA
		Both disabled		1	4	
		Both enabled		16	24	
		Receiver only		4	13	
P_D	Device power dissipation	$R_L = 50 \Omega$, Input to D is a 50-MHz 50% duty cycle square wave, DE = high, $\overline{RE} = \text{low}$, $T_A = 85^\circ\text{C}$			94	mW

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
$ V_{AB} $ or $ V_{YZ} $ Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta V_{AB} $ or $\Delta V_{YZ} $ Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OS(SS)}$ Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$ Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$ Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$ or $V_{A(OC)}$ Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{Z(OC)}$ or $V_{B(OC)}$ Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$ Voltage overshoot, low-to-high level output	See Figure 5			1.2 V_{SS}	V
$V_{P(L)}$ Voltage overshoot, high-to-low level output		–0.2 V_{SS}			V
I_{IH} High-level input current (D, DE)	$V_{IH} = 2 \text{ V to } V_{CC}$	0		10	μA
I_{IL} Low-level input current (D, DE)	$V_{IL} = \text{GND to } 0.8 \text{ V}$	0		10	μA
$ I_{OS} $ Differential short-circuit output current magnitude	See Figure 4			24	mA
I_{OZ} High-impedance state output current (driver only)	$-1.4 \text{ V} \leq (V_Y \text{ or } V_Z) \leq 3.8 \text{ V}$, Other output = 1.2 V	–15		10	μA
$I_{O(OFF)}$ Power-off output current	$-1.4 \text{ V} \leq (V_Y \text{ or } V_Z) \leq 3.8 \text{ V}$, Other output = 1.2 V, $0 \text{ V} \leq V_{CC} \leq 1.5 \text{ V}$	–10		10	μA
C_Y or C_Z Output capacitance	$V_I = 0.4 \sin(30E6\pi t) + 0.5 \text{ V}$, ⁽³⁾ Other input at 1.2 V, driver disabled		3		pF
C_{YZ} Differential output capacitance	$V_{AB} = 0.4 \sin(30E6\pi t) \text{ V}$, ⁽³⁾ Driver disabled			2.5	pF
$C_{Y/Z}$ Output capacitance balance, (C_Y/C_Z)		0.99		1.01	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) HP4194A impedance analyzer (or equivalent)

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold	Type 1			50	mV
		Type 2			150	
V _{IT-}	Negative-going differential input voltage threshold	Type 1	See Figure 9, Table 1 and Table 2		-50	mV
		Type 2			50	
V _{HYS}	Differential input voltage hysteresis, (V _{IT+} – V _{IT-})	Type 1			25	mV
		Type 2			0	
V _{OH}	High-level output voltage	I _{OH} = -8 mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA			0.4	V
I _{IH}	High-level input current ($\overline{RE}$)	V _{IH} = 2 V to V _{CC}	-10		0	μA
I _{IL}	Low-level input current ($\overline{RE}$)	V _{IL} = GND to 0.8 V	-10		0	μA
I _{OZ}	High-impedance output current	V _O = 0 V or 3.6 V	-10		15	μA
C _A or C _B	Input capacitance	V _I = 0.4 sin(30E6πt) + 0.5 V, ⁽²⁾ Other input at 1.2 V		3		pF
C _{AB}	Differential input capacitance	V _{AB} = 0.4 sin(30E6πt) V ⁽²⁾			2.5	pF
C _{A/B}	Input capacitance balance, (C _A /C _B)		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

BUS INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _A	Receiver or transceiver with driver disabled input current	V _A = 3.8 V, V _B = 1.2 V,	0		32	μA
		V _A = 0 V or 2.4 V, V _B = 1.2 V	-20		20	
		V _A = -1.4 V, V _B = 1.2 V	-32		0	
I _B	Receiver or transceiver with driver disabled input current	V _B = 3.8 V, V _A = 1.2 V	0		32	μA
		V _B = 0 V or 2.4 V, V _A = 1.2 V	-20		20	
		V _B = -1.4 V, V _A = 1.2 V	-32		0	
I _{AB}	Receiver or transceiver with driver disabled differential input current (I _A – I _B)	V _A = V _B , 1.4 ≤ V _A ≤ 3.8 V	-4		4	μA
I _{A(OFF)}	Receiver or transceiver power-off input current	V _A = 3.8 V, V _B = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	0		32	μA
		V _A = 0 V or 2.4 V, V _B = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-20		20	
		V _A = -1.4 V, V _B = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-32		0	
I _{B(OFF)}	Receiver or transceiver power-off input current	V _B = 3.8 V, V _A = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	0		32	μA
		V _B = 0 V or 2.4 V, V _A = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-20		20	
		V _B = -1.4 V, V _A = 1.2 V, 0 V ≤ V _{CC} ≤ 1.5 V	-32		0	
I _{AB(OFF)}	Receiver input or transceiver power-off differential input current (I _A – I _B)	V _A = V _B , 0 V ≤ V _{CC} ≤ 1.5 V, -1.4 ≤ V _A ≤ 3.8 V	-4		4	μA
C _A	Transceiver with driver disabled input capacitance	V _A = 0.4 sin (30E6πt) + 0.5 V ⁽²⁾ , V _B = 1.2 V		5		pF
C _B	Transceiver with driver disabled input capacitance	V _B = 0.4 sin (30E6πt) + 0.5 V ⁽²⁾ , V _A = 1.2 V		5		pF
C _{AB}	Transceiver with driver disabled differential input capacitance	V _{AB} = 0.4 sin (30E6πt) V ⁽²⁾			3	pF
C _{A/B}	Transceiver with driver disabled input capacitance balance, (C _A /C _B)		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 5	2	2.5	3.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	2.5	3.5	ns
t_r	Differential output signal rise time		2	2.6	3.2	ns
t_f	Differential output signal fall time		2	2.6	3.2	ns
$t_{sk(p)}$	Pulse skew ($t_{pHL} - t_{pLH}$)			30	150	ps
$t_{sk(pp)}$	Part-to-part skew				0.9	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽²⁾	50 MHz clock input ⁽³⁾		2	3	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽²⁾⁽⁴⁾	100 Mbps 2 ¹⁵ -1 PRBS input ⁽⁵⁾		55	150	ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 6		4	7	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			4	7	ns
t_{PZH}	Enable time, high-impedance-to-high-level output			4	7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output			4	7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(3) $t_r = t_f = 0.5$ ns (10% to 90%), measured over 30 k samples.

(4) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

(5) $t_r = t_f = 0.5$ ns (10% to 90%), measured over 100 k samples.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾ (1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, See Figure 10	2	3.6	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	3.6	6	ns
t_r	Output signal rise time		1		2.3	ns
t_f	Output signal fall time		1		2.3	ns
$t_{sk(p)}$	Pulse skew ($t_{pHL} - t_{pLH}$)			100	300	ps
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾			300	500	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽³⁾	50 MHz clock input ⁽⁴⁾		4	7	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽³⁾⁽⁵⁾	100 Mbps 2 ¹⁵ -1 PRBS input ⁽⁶⁾	Type 1	200	700	ps
			Type 2	225	800	ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 11		6	10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			6	10	ns
t_{PZH}	Enable time, high-impedance-to-high-level output			10	15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output			10	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4) $V_{ID} = 200$ mV_{pp} (LVD200A, 202A), $V_{ID} = 400$ mV_{pp} (LVD204A, 205A), $V_{cm} = 1$ V, $t_r = t_f = 0.5$ ns (10% to 90%), measured over 30 k samples.

(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

(6) $V_{ID} = 200$ mV_{pp} (LVD200A, 202A), $V_{ID} = 400$ mV_{pp} (LVD204A, 205A), $V_{cm} = 1$ V, $t_r = t_f = 0.5$ ns (10% to 90%), measured over 100 k samples.

PARAMETER MEASUREMENT INFORMATION

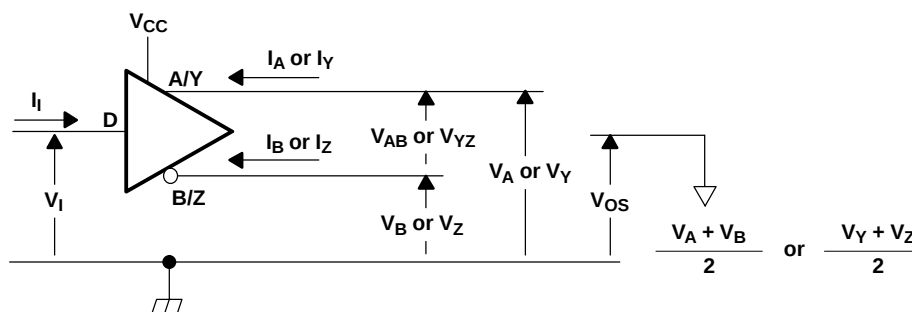
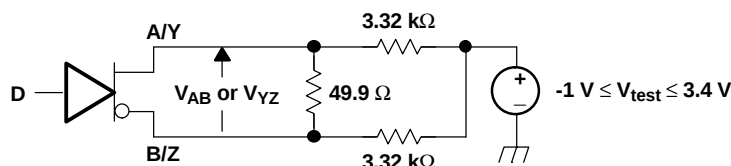
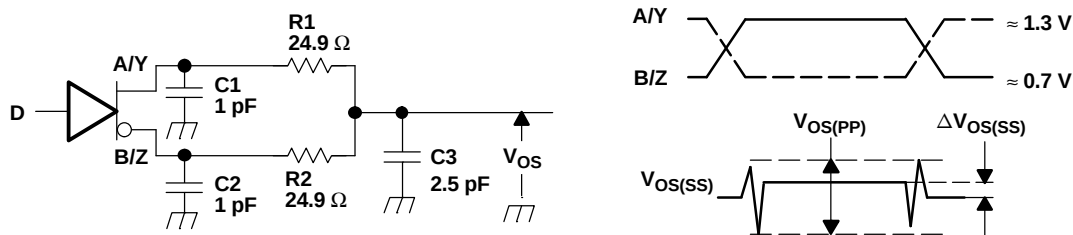


Figure 1. Driver Voltage and Current Definitions



- A. All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- C. R1 and R2 are metal film, surface mount, $\pm 1\%$, and located within 2 cm of the D.U.T.
- D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

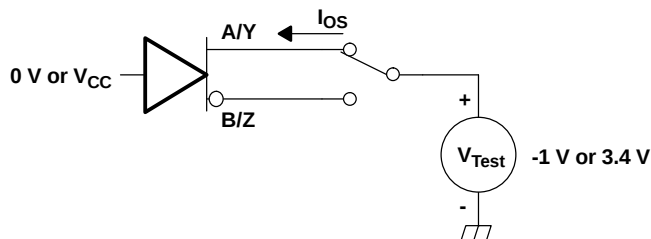
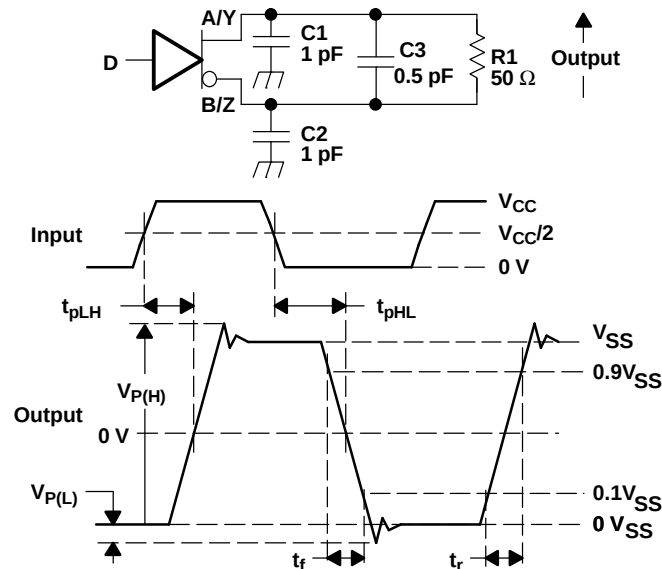


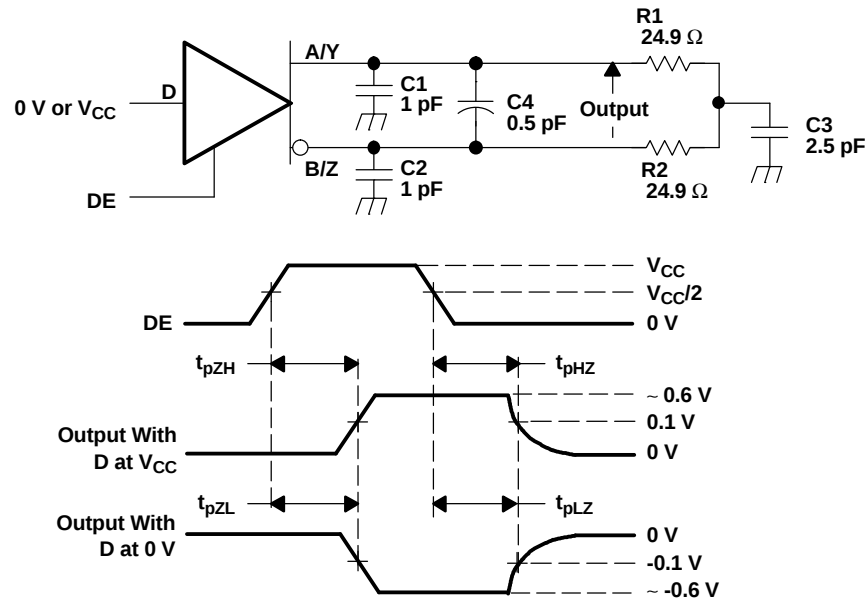
Figure 4. Driver Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.
- R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

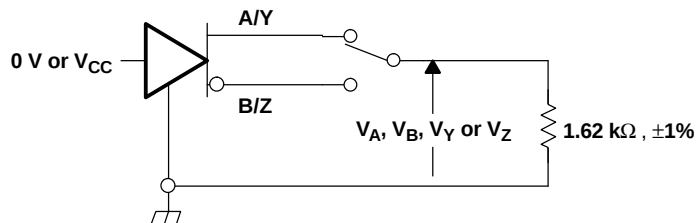
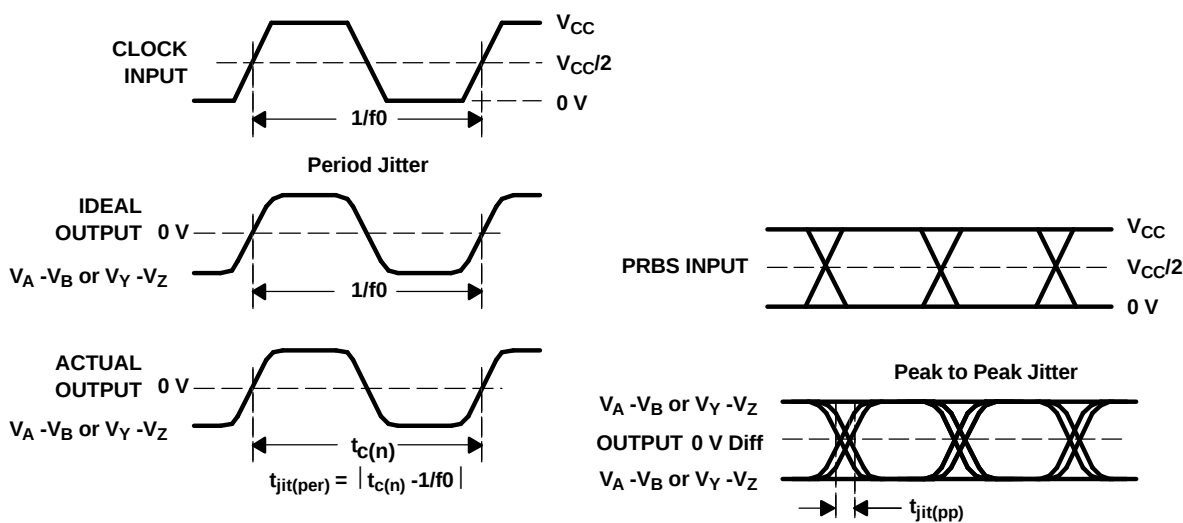


Figure 7. Maximum Steady State Output Voltage



- A. All input pulses are supplied by an Agilent 81250 Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 50 MHz 50 $\pm$ 1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 100Mbps $2^{15}-1$ PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

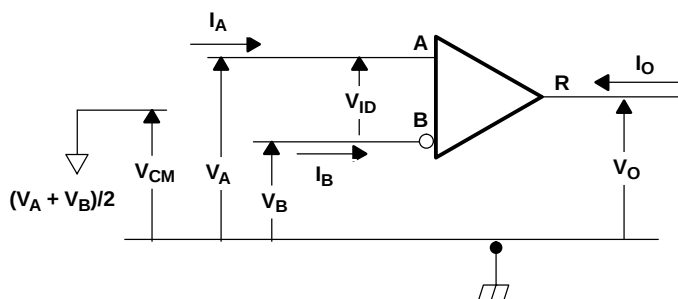


Figure 9. Receiver Voltage and Current Definitions

Table 1. Type-1 Receiver Input Threshold Test Voltages

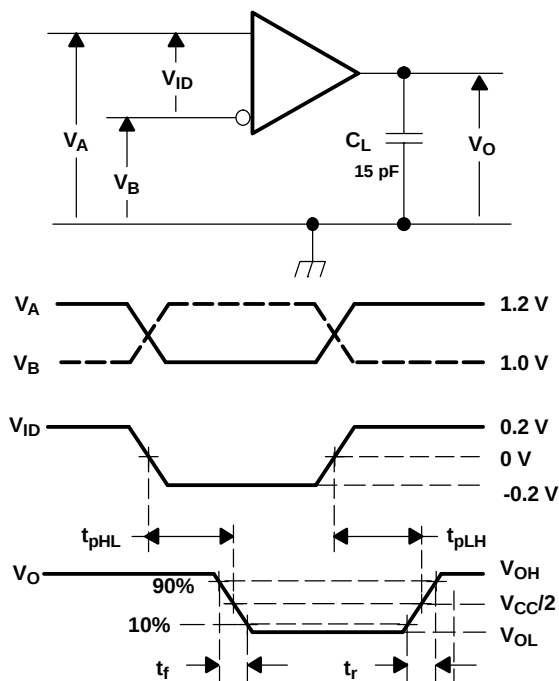
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER (1) OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.425	3.335	0.050	3.4	H
3.375	3.425	–0.050	3.4	L
–0.975	–1.025	0.050	–1	H
–1.025	–0.975	–0.050	–1	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)

Table 2. Type-2 Receiver Input Threshold Test Voltages

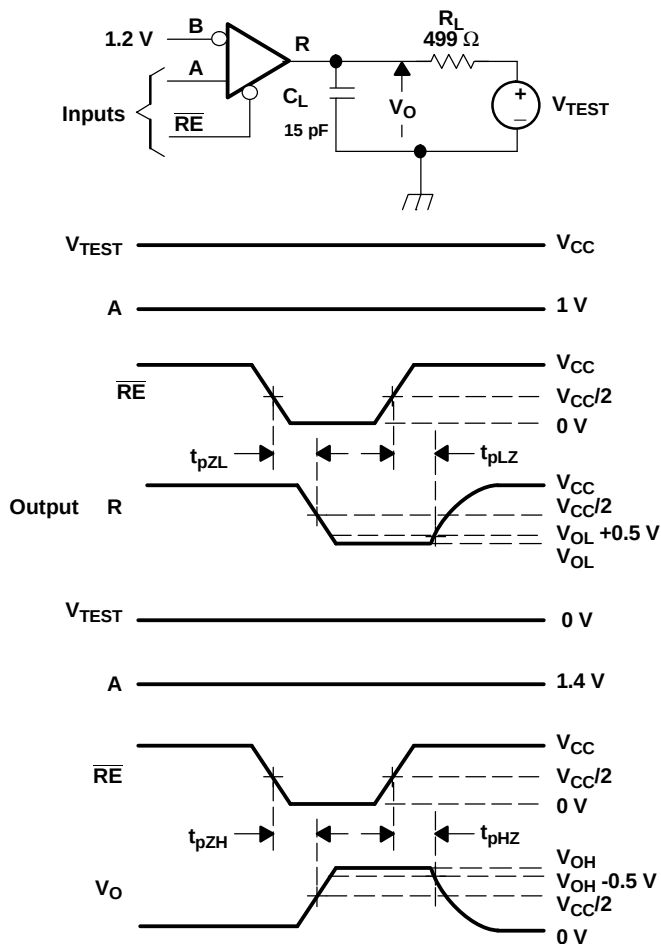
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.475	3.325	0.150	3.4	H
3.425	3.375	0.050	3.4	L
–0.925	–1.075	0.150	–1	H
–0.975	–1.025	0.050	–1	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)



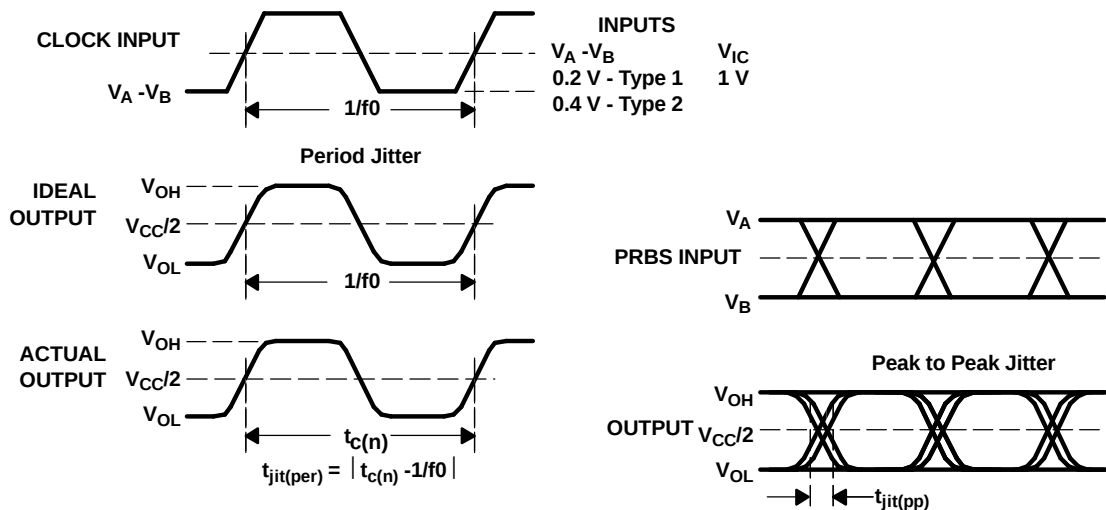
- All input pulses are supplied by a generator having the following characteristics: t_f or $t_r \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 10. Receiver Timing Test Circuit and Waveforms



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and $\pm 20\%$.

Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms

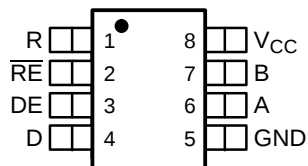


- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 50 MHz 50 $\pm$ 1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 100 Mbps 2^{15} -1 PRBS input.

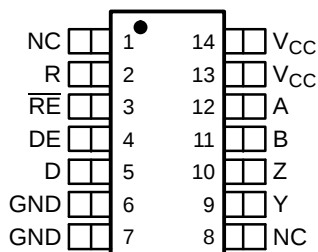
Figure 12. Receiver Jitter Measurement Waveforms

PIN ASSIGNMENTS

SN65MLVD200AD (Marked as MF200A)
SN65MLVD204AD (Marked as MF204A)
(TOP VIEW)



SN65MLVD202AD (Marked as MLVD202A)
SN65MLVD205AD (Marked as MLVD205A)
(TOP VIEW)



NC - No internal connection

DEVICE FUNCTION TABLES

TYPE-1 RECEIVER (200A, 202A)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
-50 mV $< V_{ID} < 50$ mV	L	?
$V_{ID} \leq -50$ mV	L	L
X	H	Z
X	Open	Z
Open Circuit	L	?

TYPE-2 RECEIVER (204A, 205A)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 150$ mV	L	H
50 mV $< V_{ID} < 150$ mV	L	?
$V_{ID} \leq 50$ mV	L	L
X	H	Z
X	Open	Z
Open Circuit	L	L

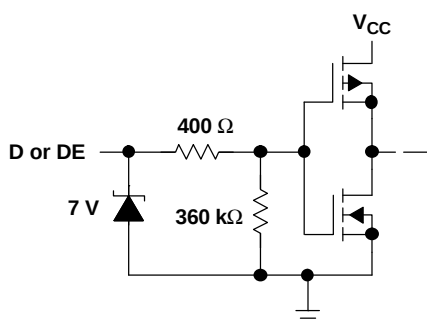
DRIVER

INPUT	ENABLE	OUTPUTS	
		A OR Y	B OR Z
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

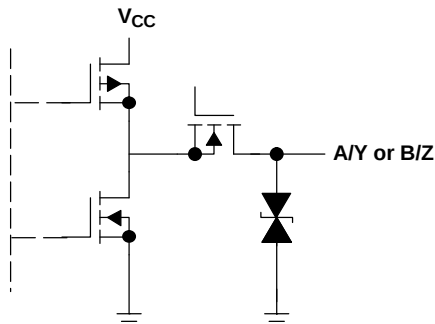
H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

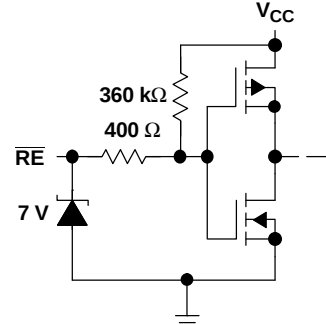
DRIVER INPUT AND DRIVER ENABLE



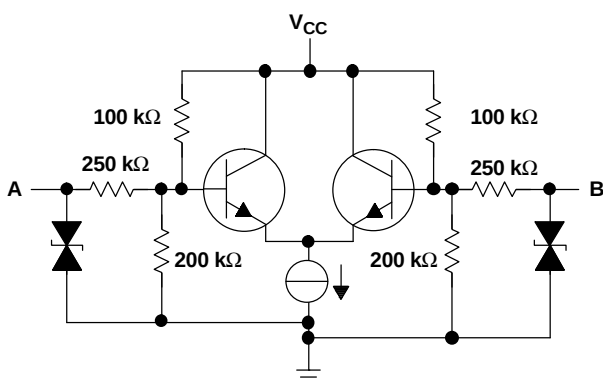
DRIVER OUTPUT



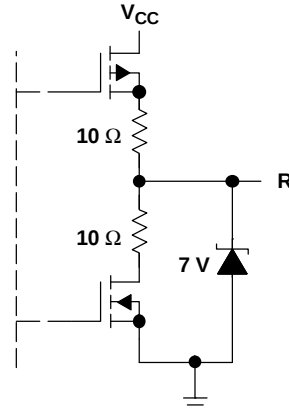
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



TYPICAL CHARACTERISTICS

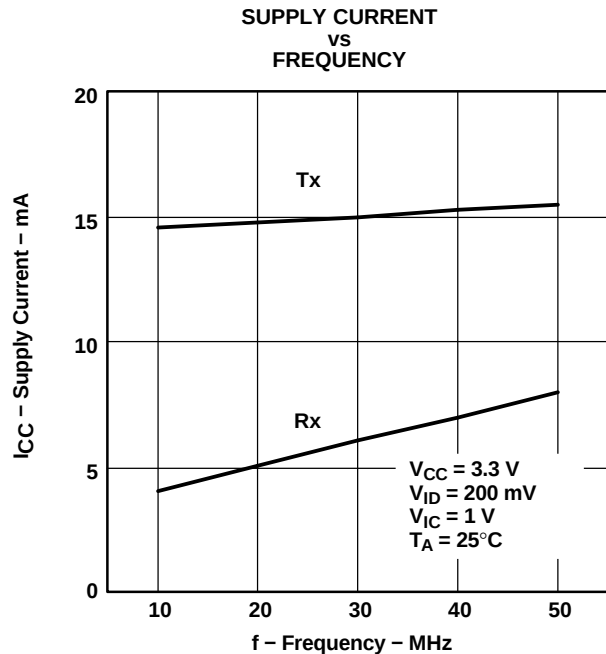


Figure 13.

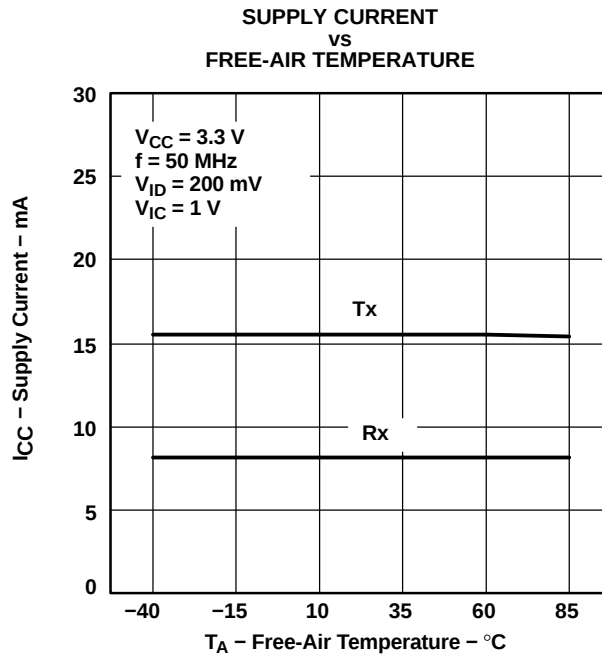


Figure 14.

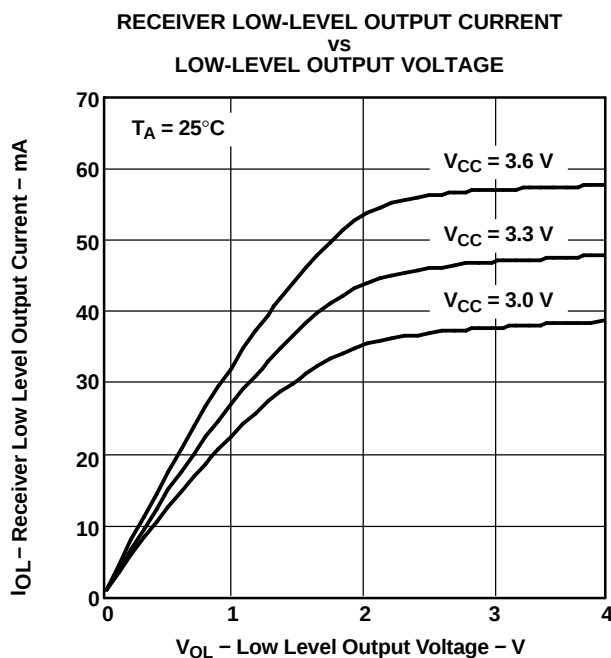


Figure 15.

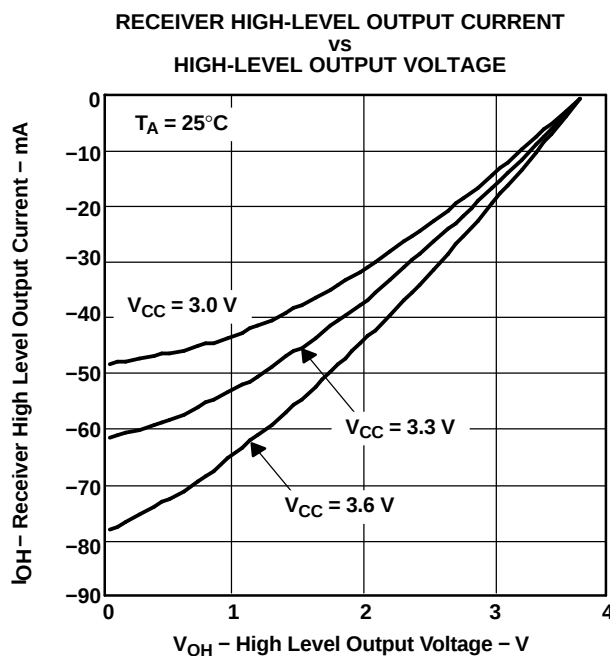


Figure 16.

TYPICAL CHARACTERISTICS (continued)

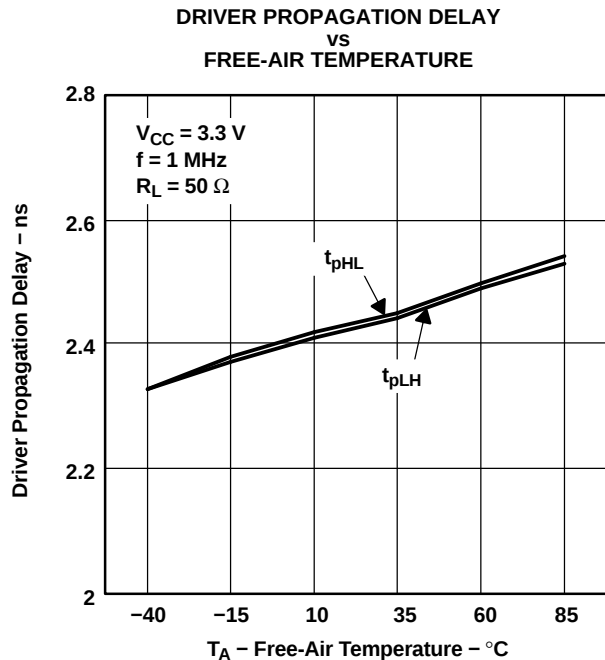


Figure 17.

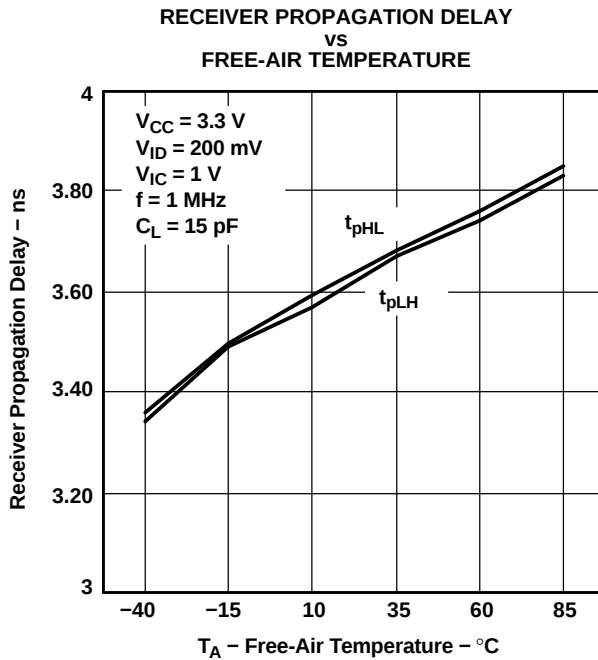


Figure 18.

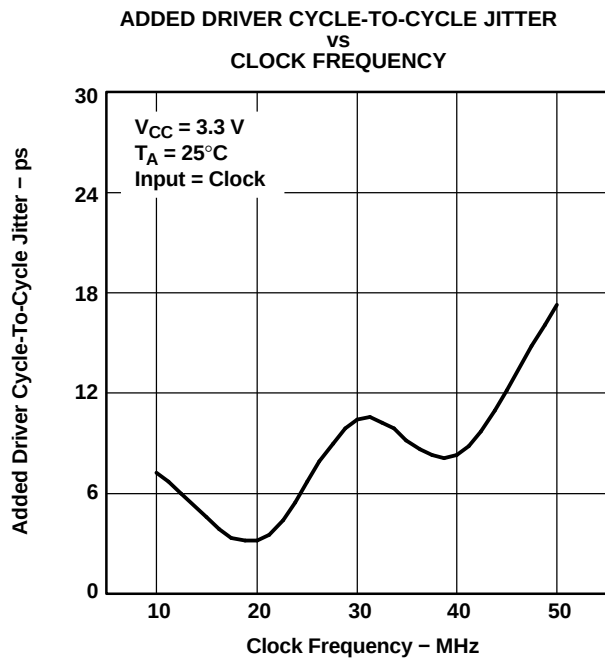


Figure 19.

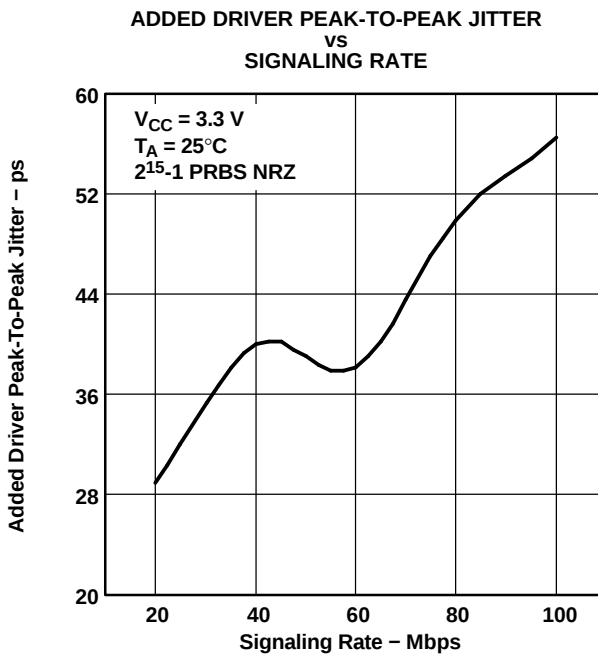


Figure 20.

TYPICAL CHARACTERISTICS (continued)

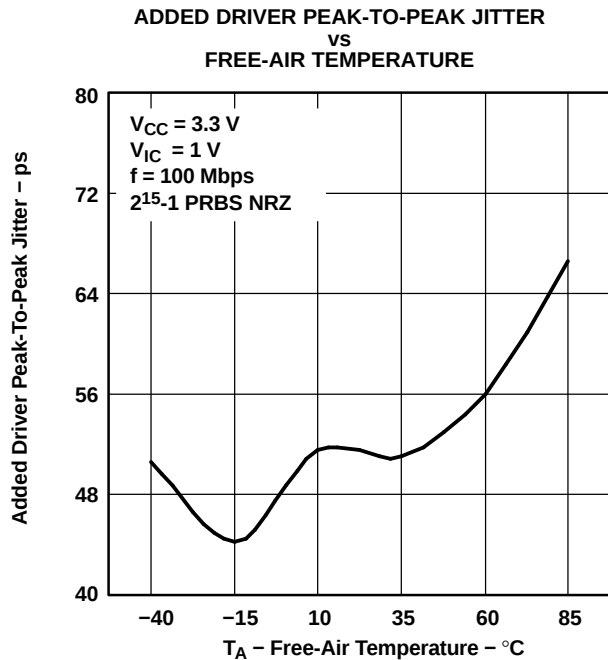


Figure 21.

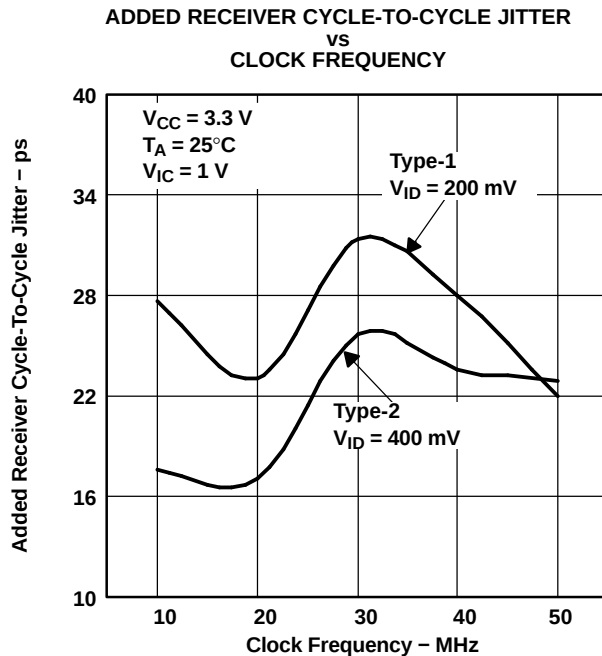


Figure 22.

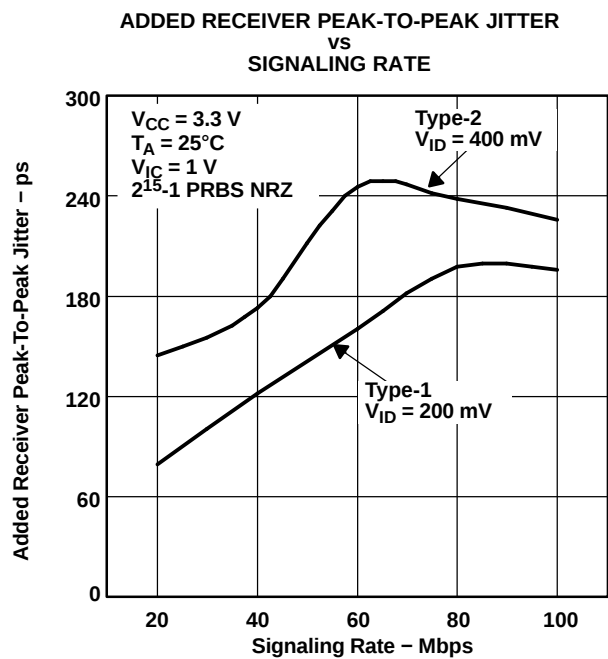


Figure 23.

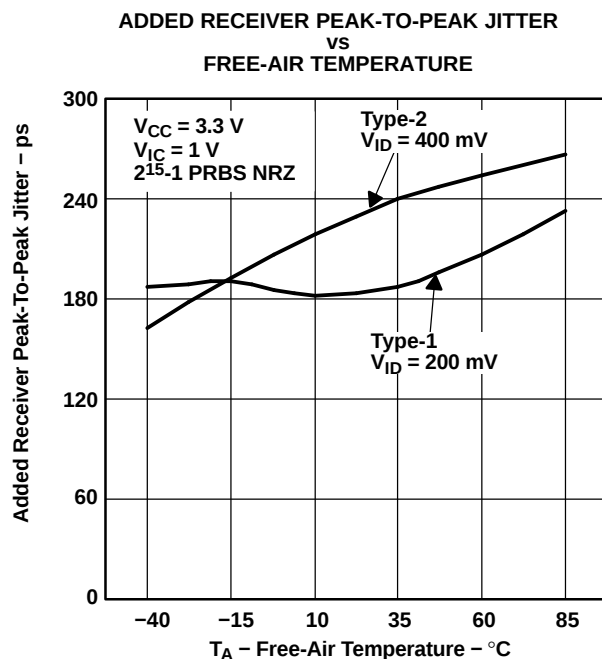


Figure 24.

TYPICAL CHARACTERISTICS (continued)

SN65MLVD200A DRIVER OUTPUT EYE PATTERN

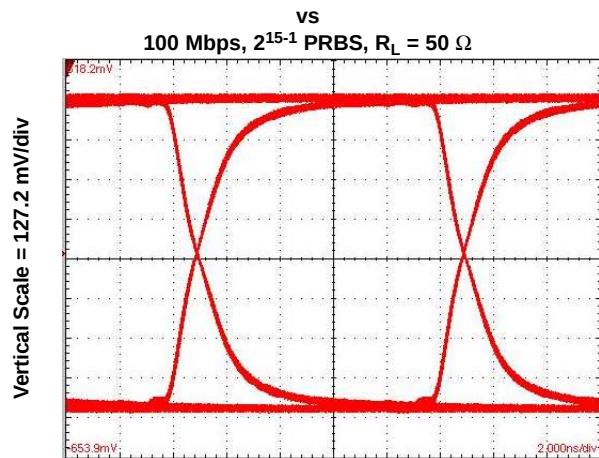


Figure 25.

SN65MLVD200A RECEIVER OUTPUT EYE PATTERN

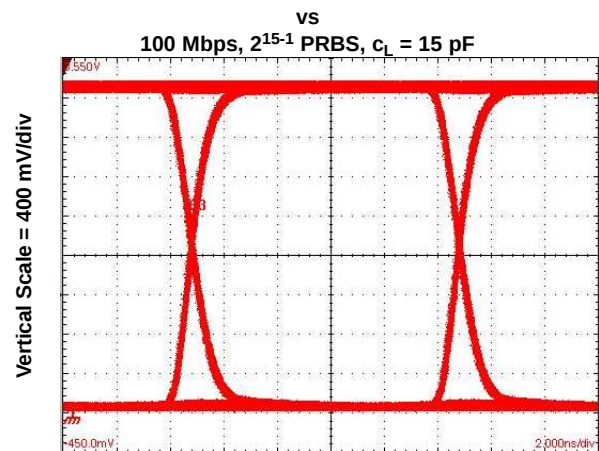


Figure 26.

APPLICATION INFORMATION

COMPARISON OF MLVD TO TIA/EIA-485

Receiver Input Threshold (Failsafe)

The MLVD standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in [Table 3](#) and [Figure 27](#).

Table 3. Receiver Input Voltage Threshold Requirements

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\text{ V} \leq V_{ID} \leq -0.05\text{ V}$	$0.05\text{ V} \leq V_{ID} \leq 2.4\text{ V}$
Type 2	$-2.4\text{ V} \leq V_{ID} \leq 0.05\text{ V}$	$0.15\text{ V} \leq V_{ID} \leq 2.4\text{ V}$

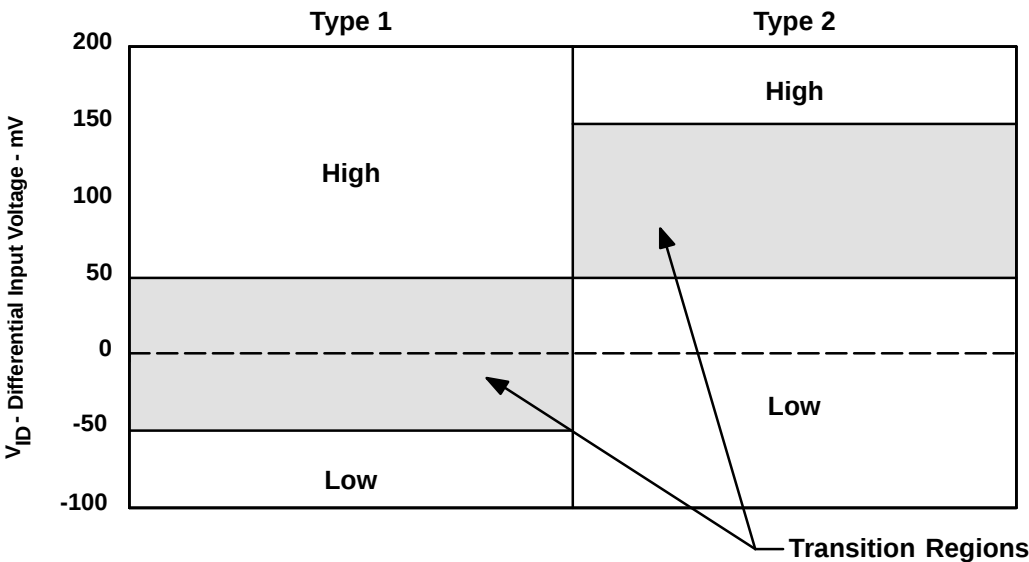


Figure 27. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65MLVD200AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

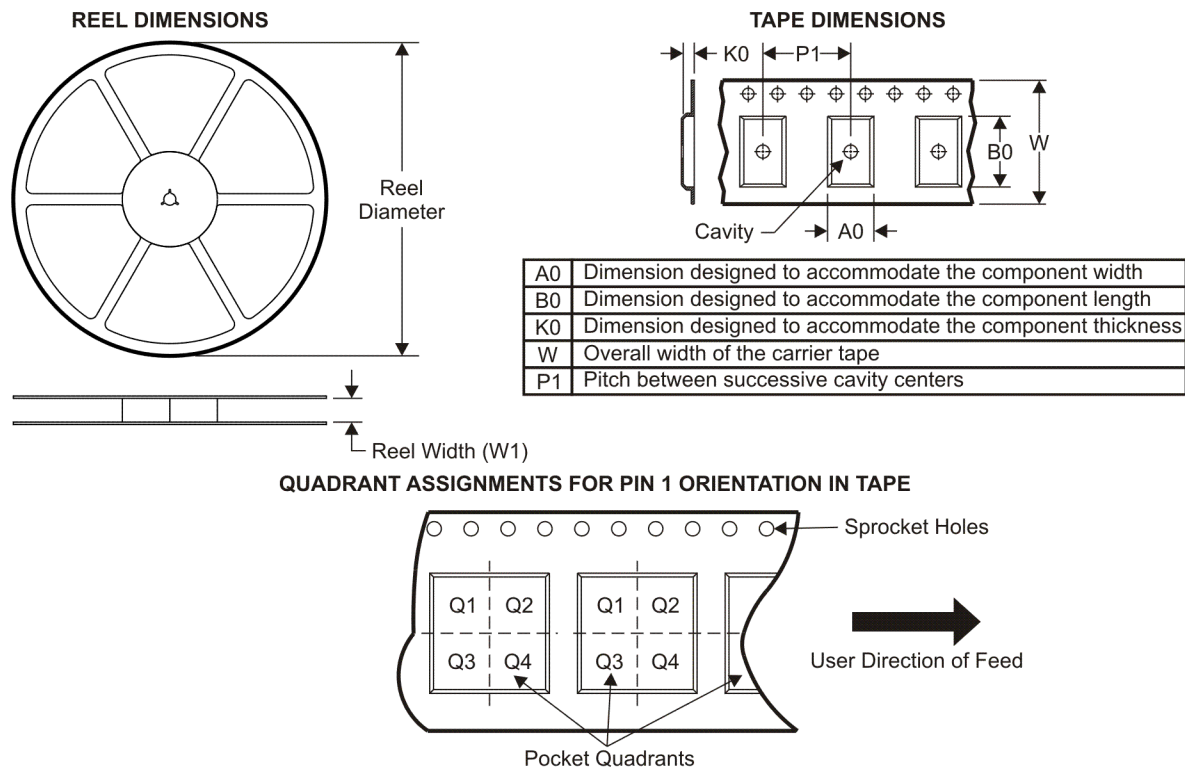
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

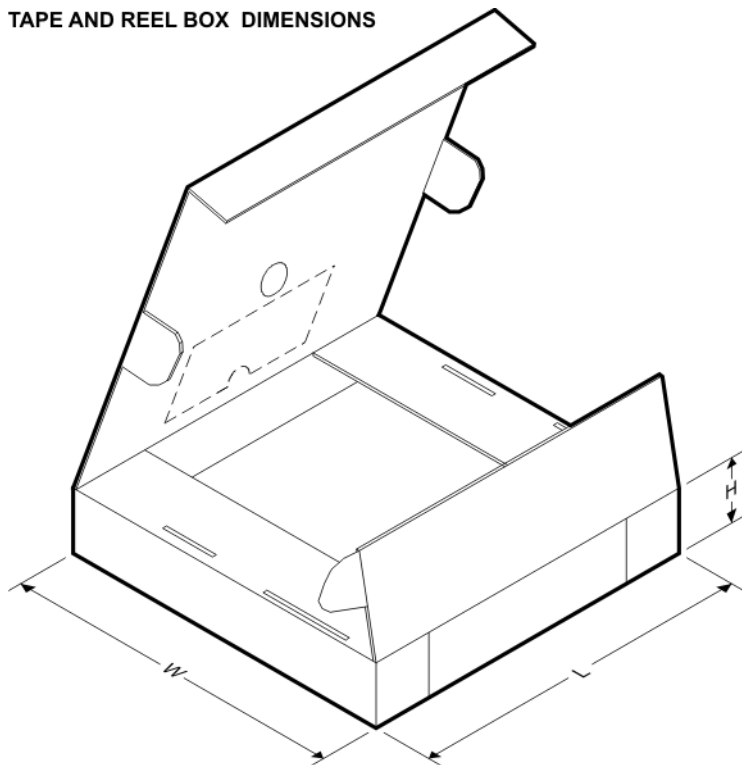
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD200ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD202ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65MLVD204ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD205ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

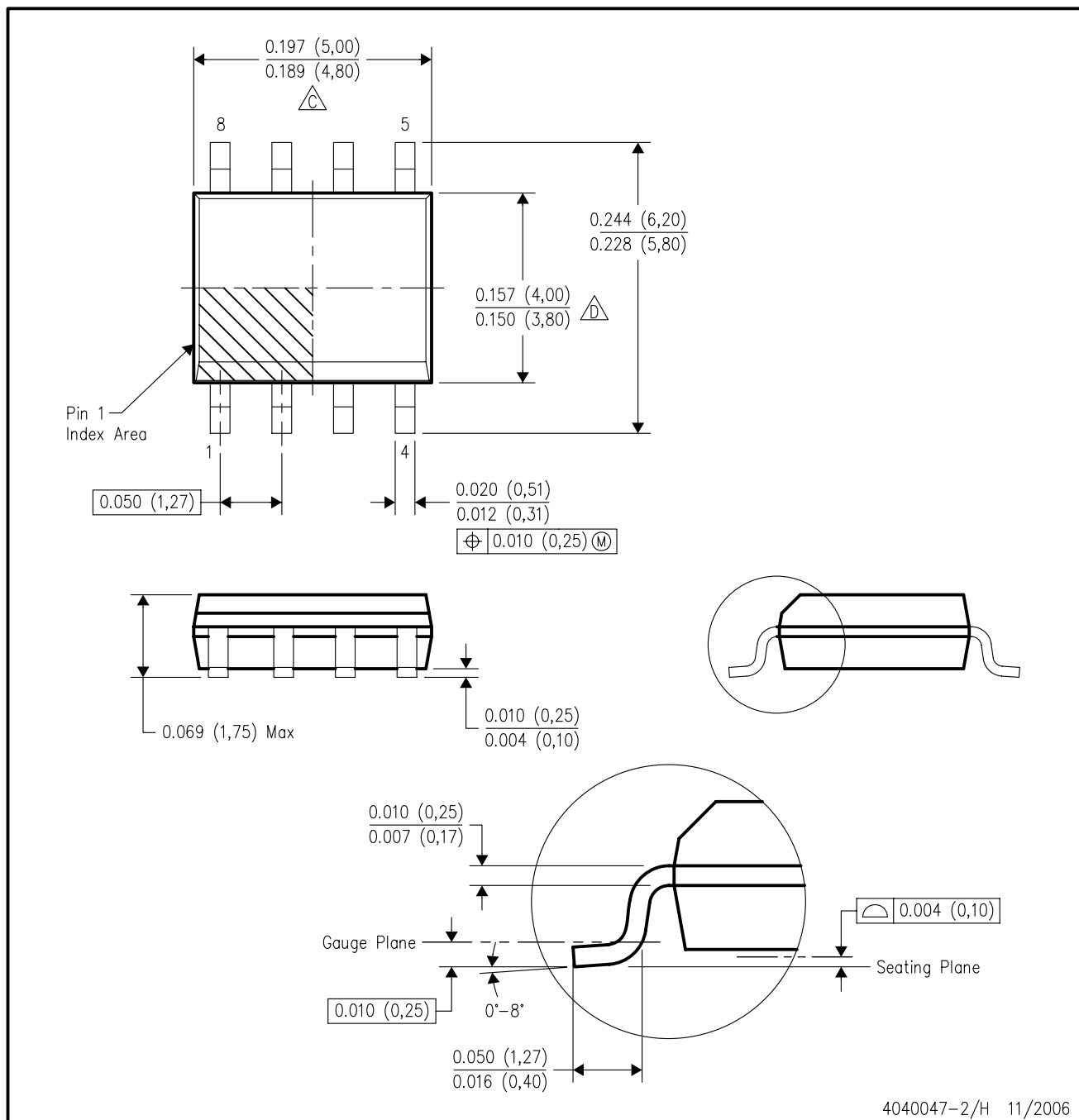


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD200ADR	SOIC	D	8	2500	340.5	338.1	20.6
SN65MLVD202ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN65MLVD204ADR	SOIC	D	8	2500	340.5	338.1	20.6
SN65MLVD205ADR	SOIC	D	14	2500	333.2	345.9	28.6

D (R-PDSO-G8)

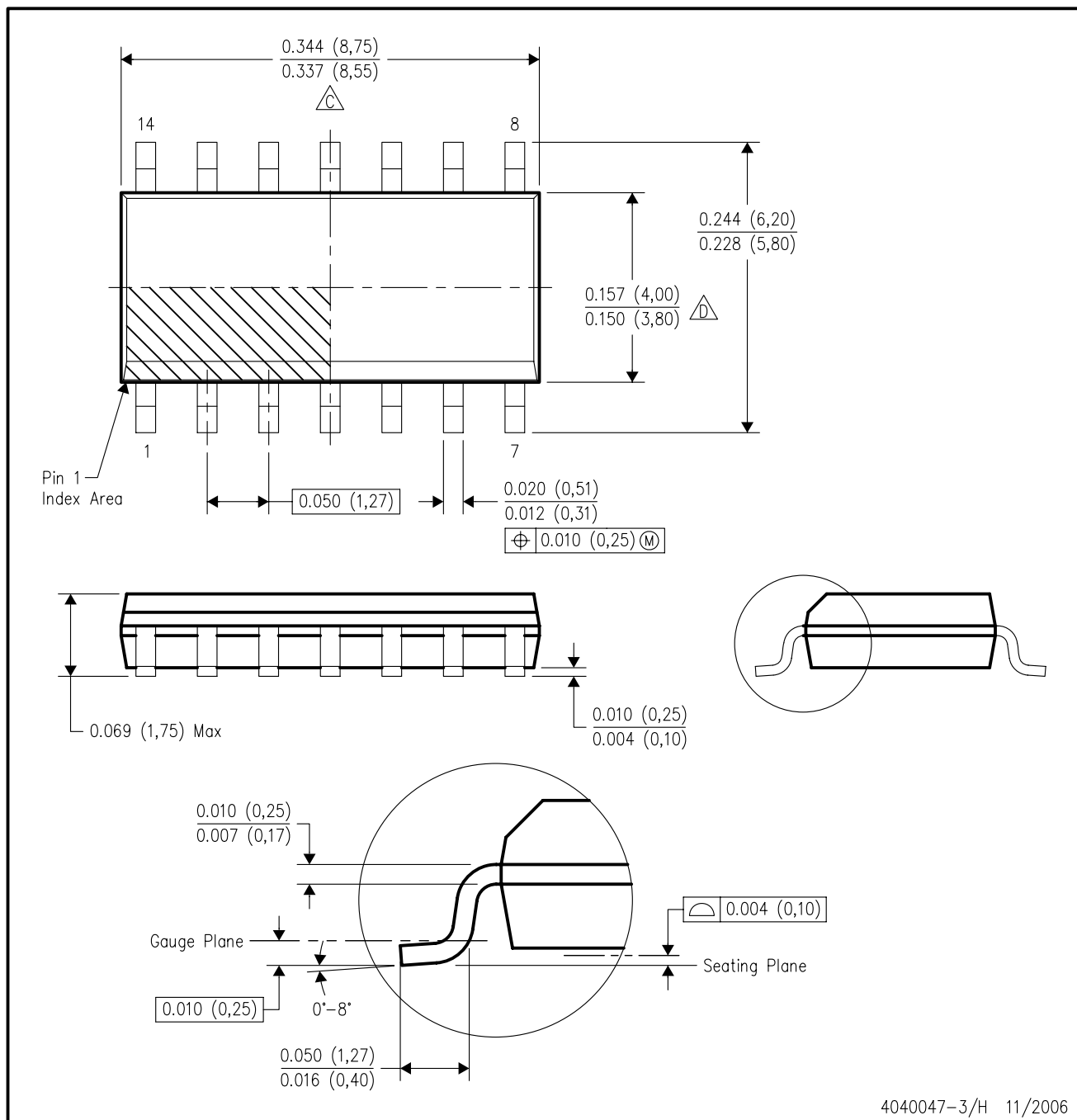
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated