AK4341

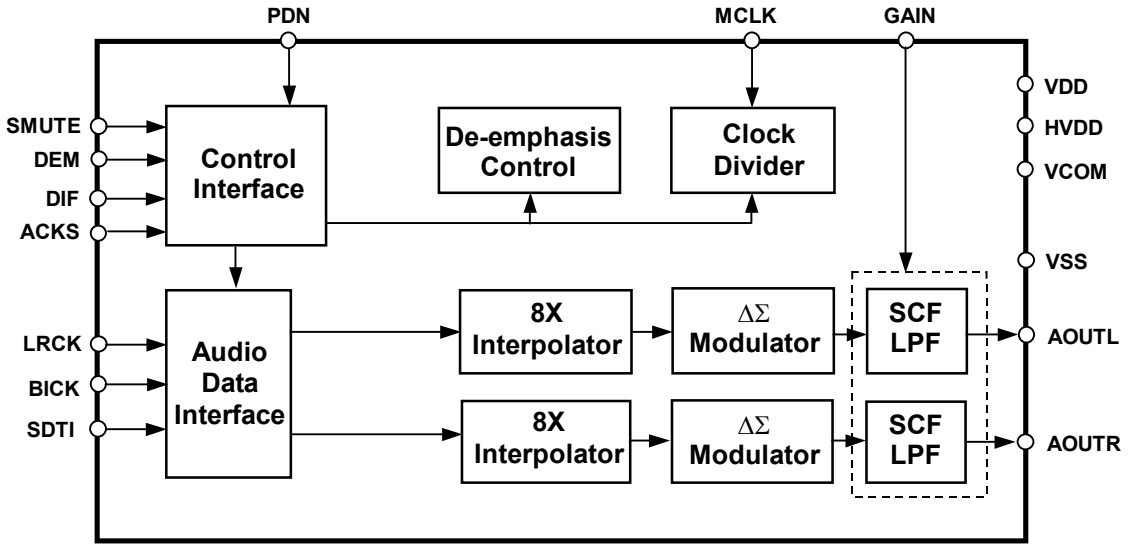
192kHz 24-Bit Stereo ΔΣ DAC with 2Vrms Output

GENERAL DESCRIPTION

The AK4341 is the 24bit DAC with 2Vrms line output for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator, the AK4341 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4341 integrates a combination of SCF and CTF filters increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of applications such as digital STB, DVD, AC-3 receiver system, etc. The AK4341 is offered in a space saving 16pin TSSOP package.

FEATURES

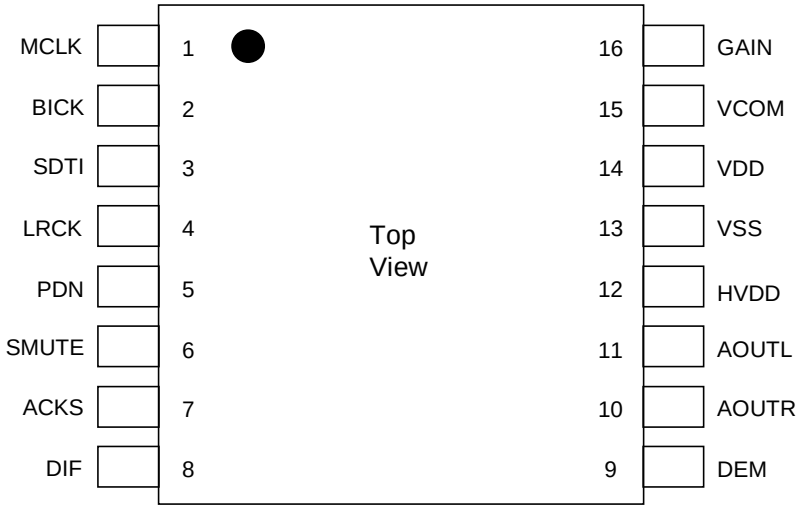
- ☐ **Sampling Rate Ranging from 8kHz to 192kHz**
- ☐ **128 times Oversampling (Normal Speed Mode)**
- ☐ **64 times Oversampling (Double Speed Mode)**
- ☐ **32 times Oversampling (Quad Speed Mode)**
- ☐ **24-Bit 8 times FIR Digital Filter**
- ☐ **SCF with High Tolerance to Clock Jitter**
- ☐ **2nd Order Analog LPF**
- ☐ **Single Ended Output Buffer**
- ☐ **Digital de-emphasis**
- ☐ **Soft mute**
- ☐ **I/F format: 24-Bit MSB justified or I²S**
- ☐ **Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)**
  256fs or 384fs (Double Speed Mode)
  128fs, 192fs (Quad Speed Mode)
- ☐ **THD+N: -86dB**
- ☐ **Dynamic Range: 100dB**
- ☐ **Power supply: 3.0 ~ +3.6V (DAC), +8.55 ~ +12.6V (Output Buffer)**
- ☐ **Ta = -20 to 85°C**
- ☐ **Very Small Package: 16pin TSSOP (6.4mm x 5.0mm)**



■ Ordering Guide

AK4341ET	-20 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4341	Evaluation Board for AK4341	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4341 is in the power-down mode, held in reset and AOUTL/R are held in VCOM. The AK4341 must be reset once upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel control mode "H": Enable, "L": Disable
7	ACKS	I	Auto Setting Mode Pin "L": Manual Setting Mode, "H": Auto Setting Mode
8	DIF	I	Audio Data Interface Format Pin "L": 24bit MSB Justified, "H": I2S
9	DEM	I	De-emphasis Enable Pin "H": Enable, "L": Disable
10	AOUTR	O	Rch Analog Output Pin When PDN pin = "L", outputs VCOM voltage.
11	AOUTL	O	Lch Analog Output Pin When PDN pin = "L", outputs VCOM voltage.
12	HVDD	-	Output Buffer Power Supply Pin Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	DAC Power Supply Pin
15	VCOM	O	DAC Common Voltage Pin Normally connected to VSS with a 10μF electrolytic cap. Outputs VCOM VDD voltage either PDN pin = "L" or "H".
16	GAIN	I	Gain Control Pin. "H": +6dB, "L": 0dB, open: +12dB. When PDN="H", the Gain pin is connected to VDD and VSS with 50kΩ resisters and held to VDD/2 when open. When PDN="L", connected to VSS with 50kΩ resister.

Note: All input pins except for the GAIN pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	DAC	VDD	-0.3	+6.0	V
	Output Buffer	HVDD	-0.3	+14	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Input Voltage		VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	DAC	VDD	+3.0	+3.3	+3.6	V
	Output Buffer	HVDD	+8.55	+9.0	+12.6	V

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; VDD = +3.3V, HVDD = +9.0V; fs = 44.1kHz; BICK = 64fs; Signal Frequency = 1kHz;
24bit Input Data; Measurement frequency = 20Hz ~ 20kHz; R_L ≥5kΩ, GAIN =0dB; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				24	Bits
Dynamic Characteristics (Note 2)					
THD+N (0dBFS)	fs=44.1kHz, BW=20kHz		-86	-80	dB
	fs=96kHz, BW=40kHz		-86	-	dB
	fs=192kHz, BW=40kHz		-86	-	dB
Dynamic Range (-60dBFS with A-weighted. Note 3)		94	100		dB
S/N (A-weighted. Note 4)		94	100		dB
Interchannel Isolation (1kHz)		-	90		dB
Interchannel Gain Mismatch			0.3	-	dB
DC Accuracy					
Gain Drift			100	-	ppm/°C
Output Voltage (Note 5)		1.85	2	2.15	Vrms
Load Capacitance (Note 6)				25	pF
Load Resistance		5			kΩ
Power Supplies					
Power Supply Current: (Note 7)					
Normal Operation (PDN pin = "H", fs≤96kHz)					
VDD			10	-	mA
HVDD			7	-	mA
Normal Operation (PDN pin = "H", fs=192kHz)					
VDD			12	18	mA
HVDD			7	11	mA
Power-Down Mode (PDN pin = "L", Note 8)					
VDD			10	100	μA
HVDD			10	100	μA

Note 2. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
Note 3. 98dB at 16bit data
Note 4. S/N does not depend on input bit length.
Note 5. Full-scale voltage (0dB). Output voltage is proportional to the voltage of VDD,
AOUT (typ.@0dB, GAIN =0dB) = 2Vrms × VDD/3.3.
Note 6. In case of driving capacitive load, inset the resister between output pin and the capacitive load.
Note 7. The current into VDD pin or HVDD pin
Note 8. All digital inputs including clock pins (MCLK, BICK and LRCK) are fixed to VSS or VDD, and GAIN pin is fixed to VSS or open.

FILTER CHARACTERISTICS

(Ta = 25°C; VDD = +3.0 ~ +3.6V, HVDD = +8.55 ~ +12.6V; fs = 44.1kHz; DEM = OFF, GAIN =0dB)

Parameter			Symbol	min	typ	max	Units
Digital filter (DEM = OFF)							
Passband	±0.05dB (Note 9)		PB	0		20.0	kHz
	–6.0dB			-	22.05	-	kHz
Stopband (Note 9)			SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay (Note 10)			GD	-	19.3	-	1/fs
De-emphasis Filter (DEM = ON)							
De-emphasis Error	fs = 32kHz			-	-	–1.5/0	dB
(Relative to 0Hz)	fs = 44.1kHz			-	-	–0.2/+0.2	dB
	fs = 48kHz			-	-	0/+0.6	dB
Digital Filter + LPF (DEM = OFF)							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	± 0.05	-	dB
	40.0kHz	fs=96kHz	FR	-	± 0.05	-	dB
	80.0kHz	fs=192kHz	FR	-	± 0.05	-	dB

Note 9. The passband and stopband frequencies scale with fs(system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

DC CHARACTERISTICS

(Ta = 25°C; VDD = +3.0 ~ +3.6V, HVDD = +8.55 ~ +12.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (except for GAIN pin)	VIH	70%VDD	-	-	V
Low-Level Input Voltage (except for GAIN pin)	VIL	-	-	30%VDD	V
High-Level Input Voltage (for GAIN pin)	VIH	90%VDD	-	-	V
Low-Level Input Voltage (for GAIN pin)	VIL	-	-	10%VDD	V
Open (for GAIN pin. Note 11)	open	-	VDD/2	-	V
Input Leakage Current (Note 12)	Iin	-	-	± 10	μA

Note 11. GAIN pin is biased to VDD and VSS via50kΩ (typ) resisters internally.

Note 12. Except for the GAIN pin

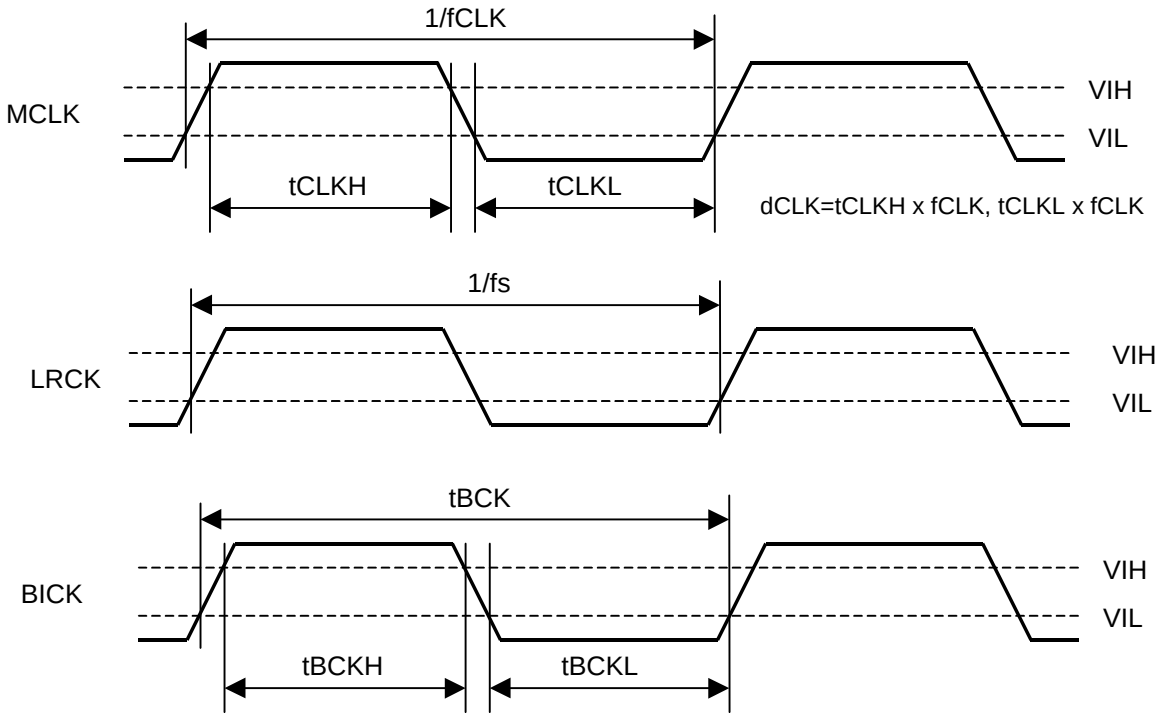
SWITCHING CHARACTERISTICS

(Ta = 25°C; VDD = +3.0 ~ +3.6V, HVDD = +8.55 ~ +12.6V)

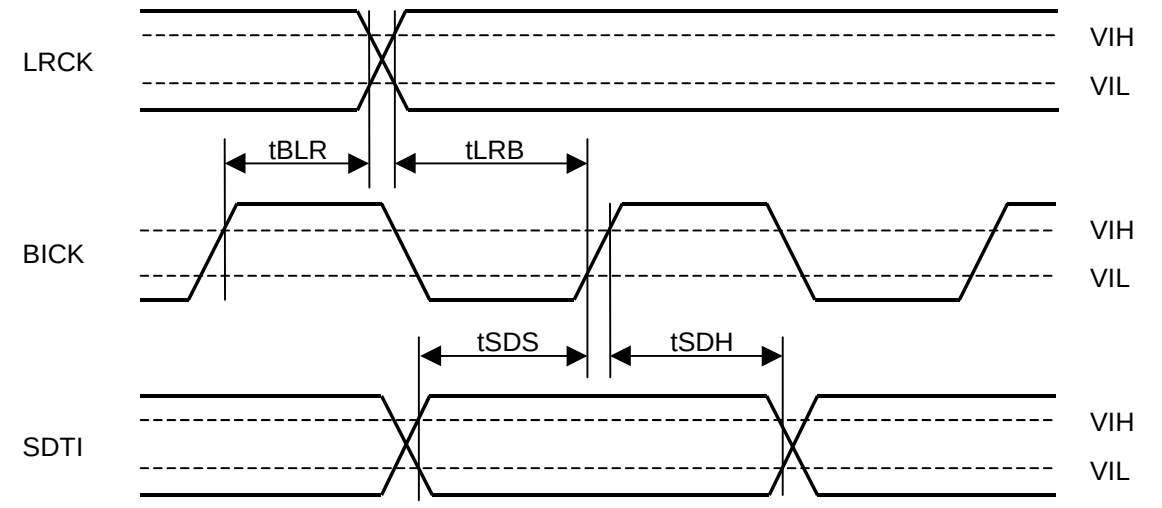
Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	32		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
Audio Interface Timing					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			ns
Double Speed Mode	tBCK	1/64fsd			ns
Quad Speed Mode	tBCK	1/64fsq			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK "↑" to LRCK Edge (Note 13)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 13)	tLRB	20			ns
SDTI Hold Time	tSDH	20			ns
SDTI Setup Time	tSDS	20			ns
Reset Timing					
RSTN Pulse Width (Note 14)	tRST	150			ns

Note 13. BICK rising edge must not occur at the same time as LRCK edge.
Note 14. The AK4341 can be reset by bringing PDN pin = "L".

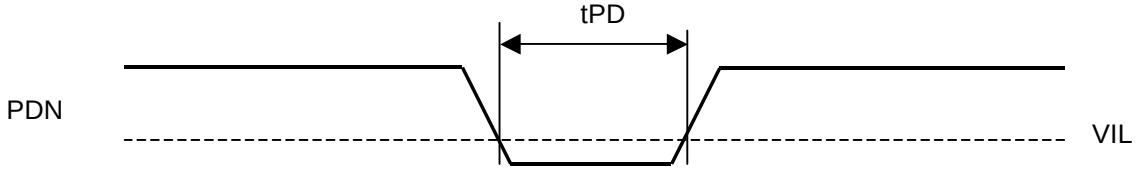
■ Timing Diagram



Clock Timing



Serial Interface Timing



Power-down Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4341, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS pin = "L", Normal Speed Mode), the frequency of MCLK is set automatically. In Auto Setting Mode (ACKS pin = "H"), MCLK frequency is detected automatically and then the internal master clock becomes the appropriate frequency (Table 1).

The AK4341 is automatically placed in the power save mode when MCLK stops in the normal operation mode (PDN pin = "H"), and the analog output becomes the VCOM voltage. After MCLK is input again, the AK4341 is powered up. After exiting reset at power-up etc., the AK4341 is in the power-down mode until MCLK and LRCK are input.

ACKS pin	LRCK	MCLK (MHz)							Sampling Speed
	fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
H	32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
	44.1kHz	-	-	-	-	22.5792	33.8688	-	
	48.0kHz	-	-	-	-	24.5760	36.8640	-	
	88.2kHz	-	-	22.5792	33.8688	-	-	-	Double
	96.0kHz	-	-	24.5760	36.8640	-	-	-	
	176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
	192.0kHz	24.5760	36.8640	-	-	-	-	-	
L	32.0kHz	-	-	8.1920	12.2880	16.3840	24.5760	36.8640	Normal
	44.1kHz	-	-	11.2896	16.9344	22.5792	33.8688	-	
	48.0kHz	-	-	12.2880	18.4320	24.5760	36.8640	-	

Table 1. ACKS pin setting and system clock example

■ Audio Serial Interface Format

The Audio data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF pin can selects two serial data modes as shown in Table 2. In all modes the serial data is MSB-first, 2's compliment format and latched on the rising edge of BICK.

Mode	DIF	SDTI Format	BICK	Figure
0	L	24bit MSB justified	≥48fs	Figure 1
1	H	24bit I^2S	≥48fs	Figure 2

Table 2. Audio Data Formats

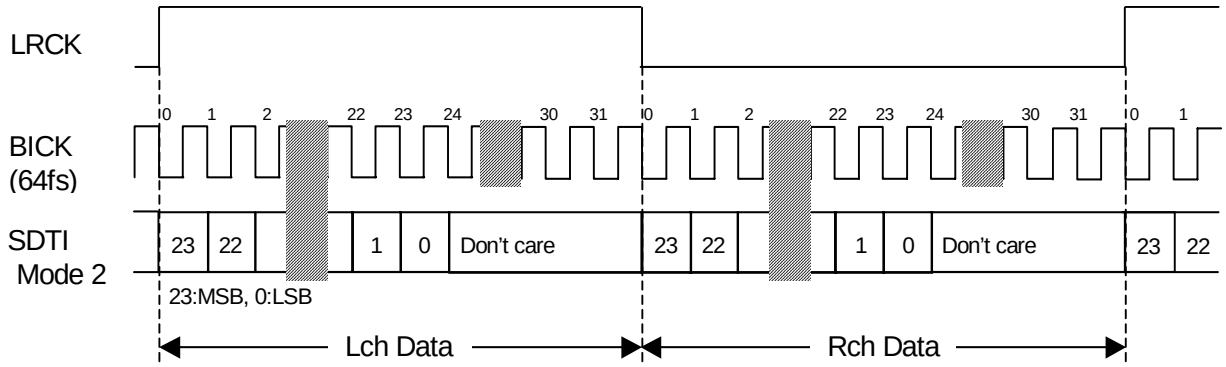


Figure 1. Mode 0 Timing

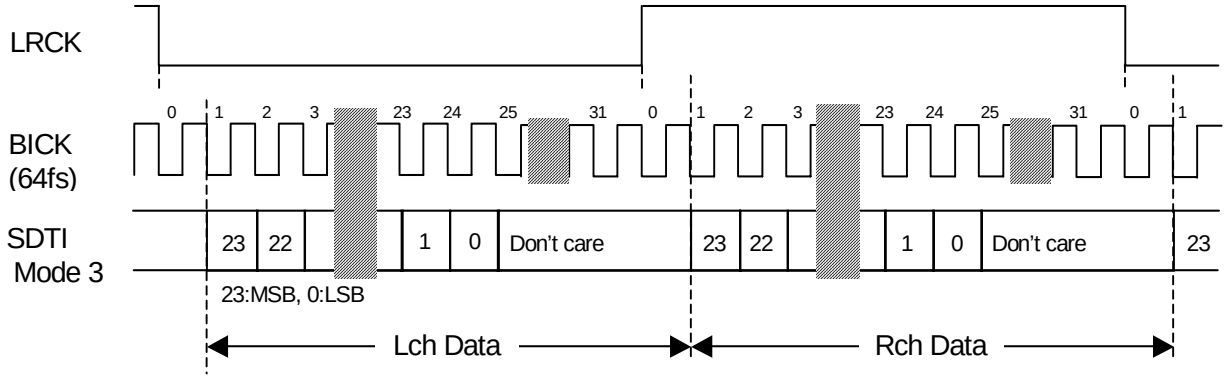


Figure 2. Mode 1 Timing

■ De-emphasis Filter

A digital de-emphasis filter is built-in (tc = 50/15μs). DEM pin is internal pull-down pin. Setting DEM pin "H" enables the digital de-emphasis filter. Refer to the section of "FILTER CHARACTERISTICS" regarding the gain error when the de-emphasis filter is enabled. De-emphasis filter is off when double/quad speed mode.

DEM pin	De-emphasis Filter
H	ON
L	OFF

Table 3. De-emphasis Filter Control (Normal Speed Mode)

■ Output Gain Setting

Outputs level of AOUTL/AOUTR pin can be selected by GAIN pin.

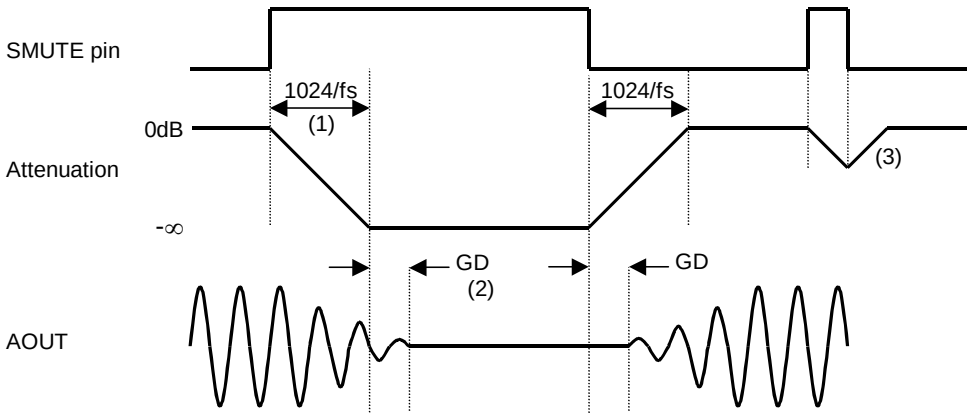
GAIN pin	GAIN	Input Level	Output Level (VDD=3.3V)	
L	0dB	0dBFS	2Vrms (typ)	
H	+6.0dB	-6dBFS	2Vrms (typ)	(Note 15)
open	+12dB	-12dBFS	2Vrms (typ)	(Note 15)

Note 15. Output level of AOUTL/AOUTR pin clips if it exceeds 2Vrms.
The input data should be 2Vrms or less as the output level.

Table 4. Output Level Setting

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When the SMUTE pin goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When the SMUTE pin is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within the 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:
(1) 1020LRCK cycles (1020/fs) at input data is attenuated to -∞.
(2) The analog output corresponding to the digital input has a group delay, GD.
(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

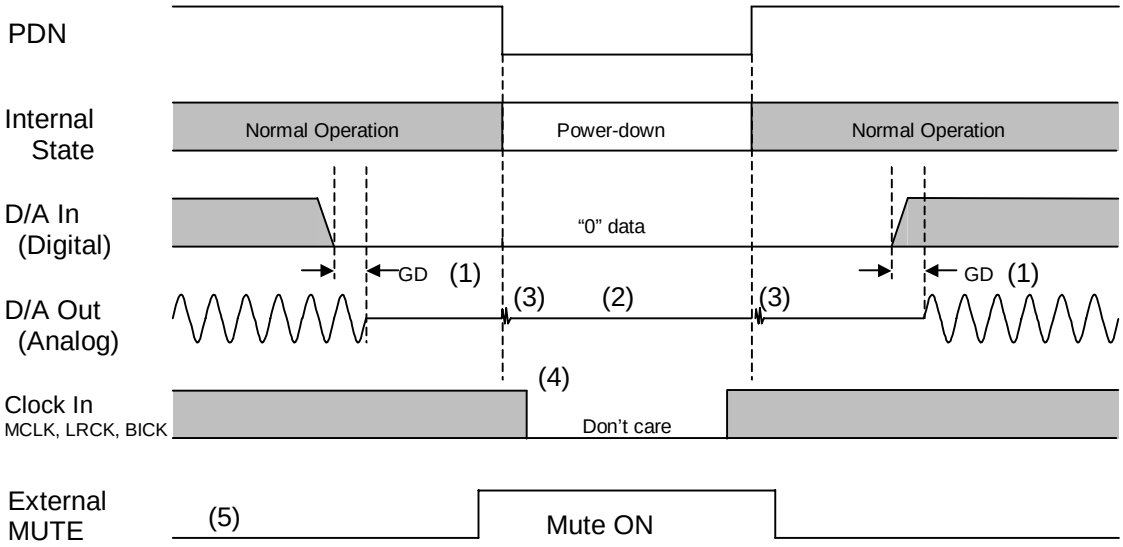
Figure 3. Soft Mute

■ System Reset

The AK4341 must be reset once by bringing PDN pin = "L" upon power-up. The AK4341 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4341 is in the power-down mode until LRCK are input.

■ Power-down

The AK4341 is placed in the power-down mode by bringing PDN pin “L” and the analog outputs are VCOM voltage (VDD). Figure 4 shows an example of the system timing at the power-down and power-up.



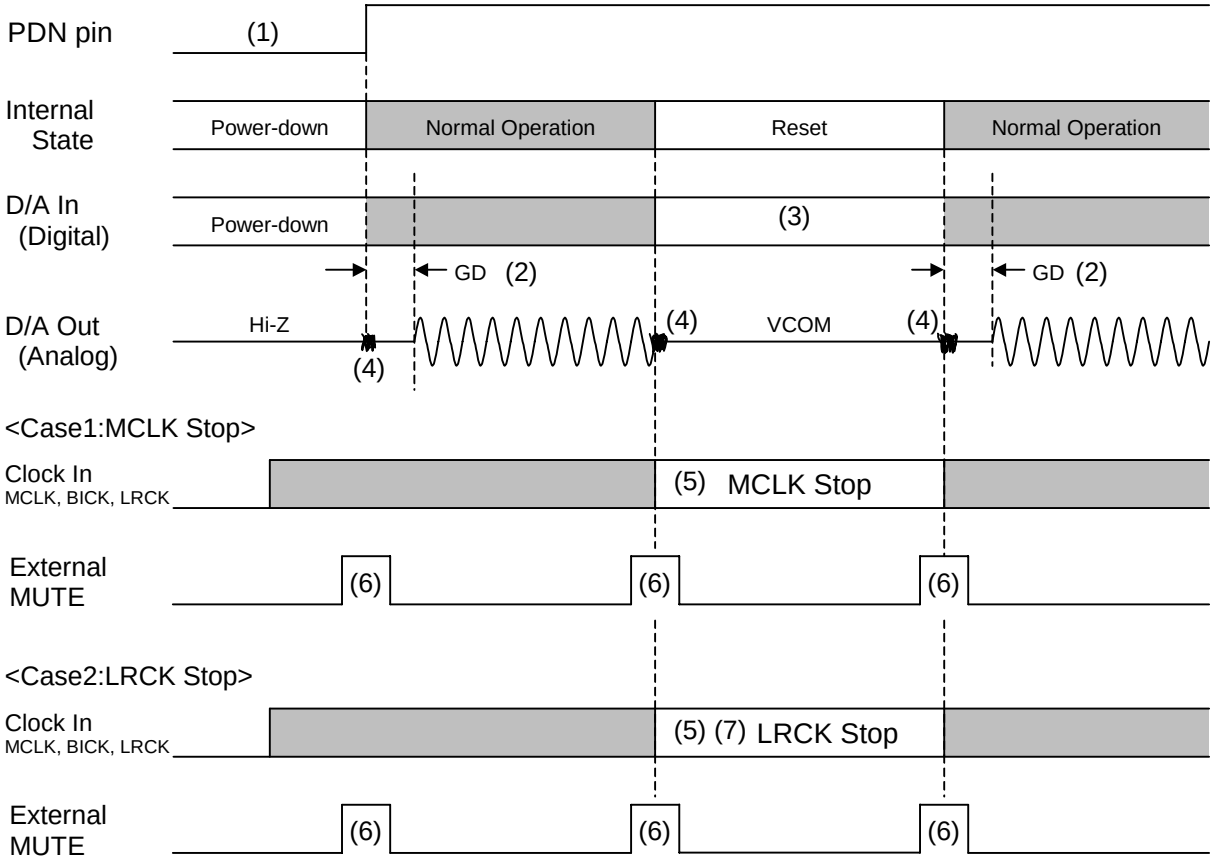
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are VCOM level (VDD) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = “L”).
(5) Please mute the analog output externally if the click noise (3) influences system application.
The timing example is shown in this figure.

Figure 4. Power-down/up Sequence Example

■ Reset Function

When the MCLK or LRCK stops during the normal operation (PDN pin ="H"), the AK4341 is placed in the reset mode and its analog outputs are set to VCOM voltage (VDD). When the MCLK and LRCK are restarted, the AK4341 return to the normal operation mode. The BICK can be stopped when MCLK or LRCK is stopped but shouldn't be stopped when MCLK and LRCK are supplied.



Notes:

(1) PDN pin should be "L" for 150ns or more after power-on.
(2) The analog output corresponding to digital input has the group delay (GD).
(3) Digital data can be stopped. The click noise after the MCLK and LRCK are input again can be reduced by inputting the "0" data during this period.
(4) Click noise occurs within 20usec and 20usec +(3~4LRCK) after the edges("↑ ↓") of the PDN pin and MCLK starting. The noises also occur when MCLK or LRCK is stopped and within 20usec after stopping.
(5) Clocks (MCLK, BICK, LRCK) can be stopped in the reset mode (MCLK or LRCK is stopped).
(6) Mute externally if the click noises (4) cause problem.
(7) The AK4341 detects the stop of LRCK by the ratio MCLK/LRCK > 2048. If the LRCK is input, when LRCK is stopping, then the AK4341 exits the reset mode.

Figure 5. Reset Timing Example

SYSTEM DESIGN

Figure 6 shows the system connection diagram. An evaluation board (AKD4341) is available in order to allow an easy study on the layout of a surrounding circuit.

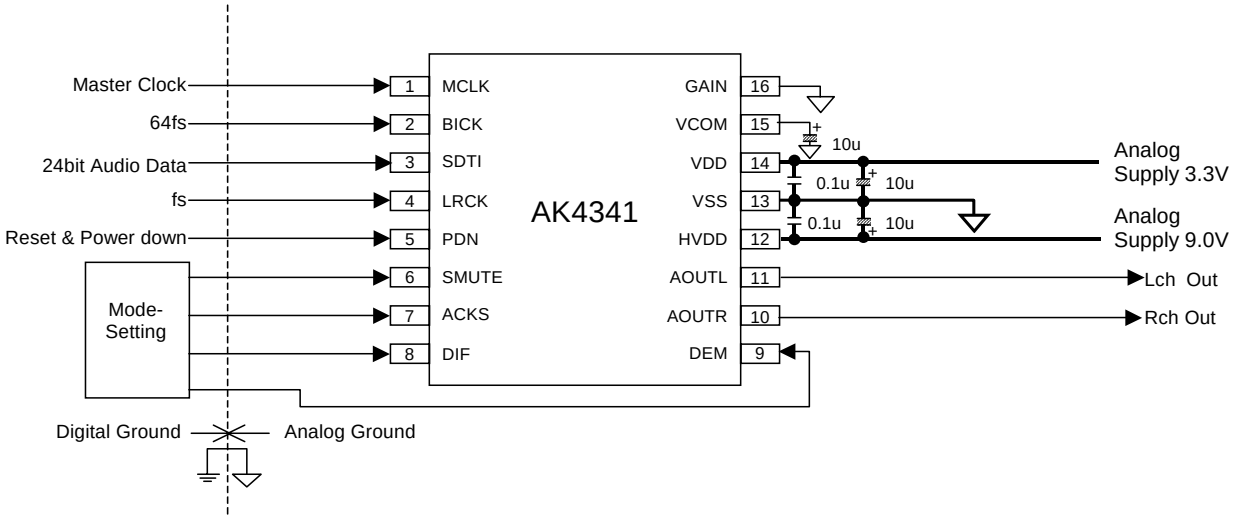


Figure 6. Typical Connection Diagram (GAIN = 0dB)

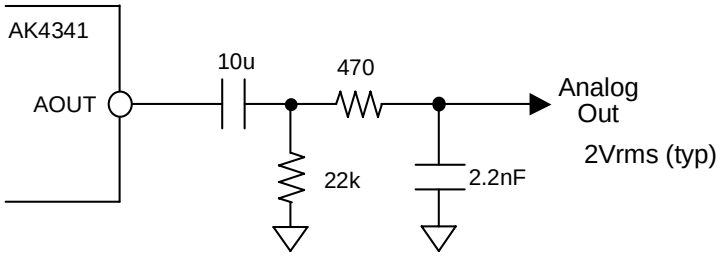
1. Grounding and Power Supply Decoupling

VDD, HVDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to VDD and HVDD as possible. The differential voltage between VDD and VSS pins set the analog output range. **The power-up sequence between VDD and HVDD is not critical.**

2. Analog Outputs

The analog outputs are single-ended and centered around the VDD voltage. The output signal range is typically 2Vrms (typ @VDD=3.3V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VDD voltage for 000000H (@24bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VDD + a few mV. Figure 7 shows an example of the external LPF with 2Vrms (typ) output.

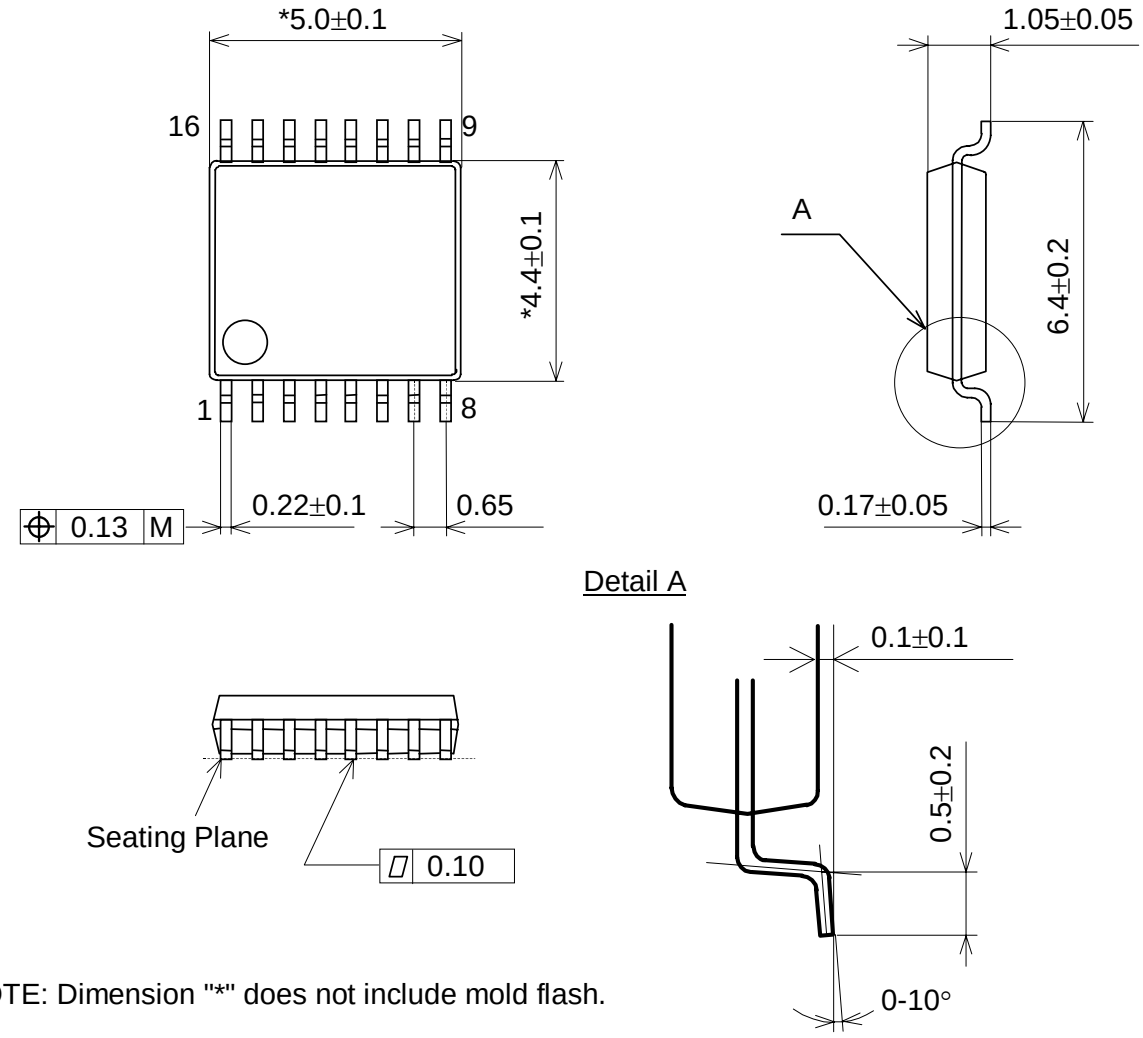


(fc = 154kHz, gain = -0.28dB @ 40kHz, gain = -1.04dB @ 80kHz)

Figure 7. External 1st order LPF Circuit Example

PACKAGE

16pin TSSOP (Unit: mm)

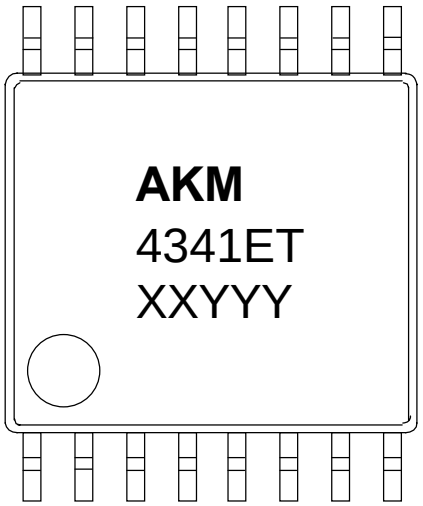


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4341ET
4) Asahi Kasei Logo

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/10/30	00	First Edition		
07/03/26	01	Error correction	1	FEATURE I/F format: 24bit MSB justified, 24/16 bit LSB justified or I2S → 24bit MSB justified or I2S
			3	PIN/FUNCTION No.8 "L": Left Justified → 24 bit MSB Justified
			9	AUDIO SERIAL INTERFACE The DIF pin can select four serial data modes as shown in Table 2 → The DIF pin can select two serial data modes as shown in Table 2