# AK4388

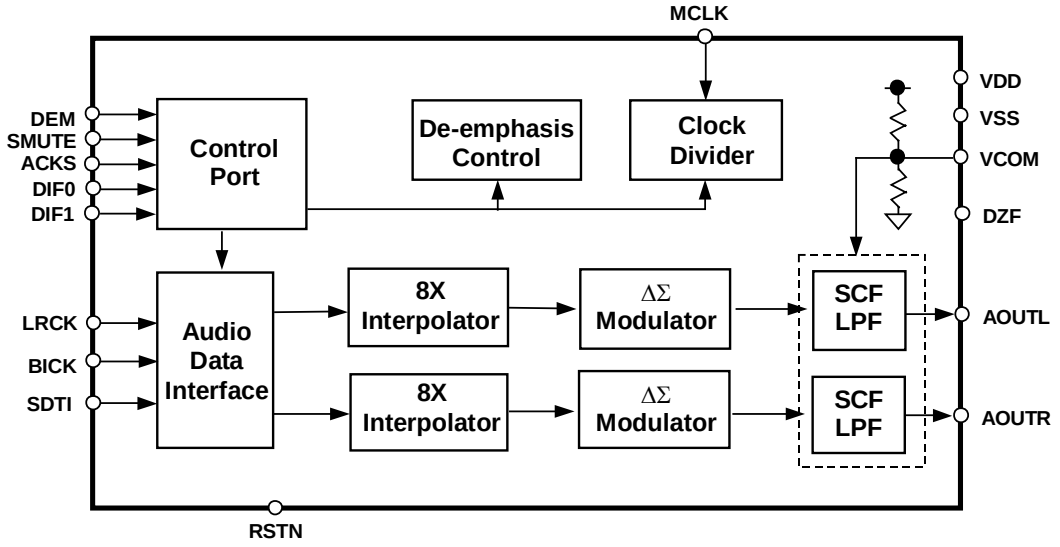
## 192kHz 24-Bit 2ch ΔΣ DAC

## GENERAL DESCRIPTION

The AK4388 offers the perfect mix for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator, the AK4388 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4388 integrates a combination of SCF and CTF filters increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of applications including DVD-Audio. The AK4388 is offered in a space saving 16pin TSSOP package.

## FEATURES

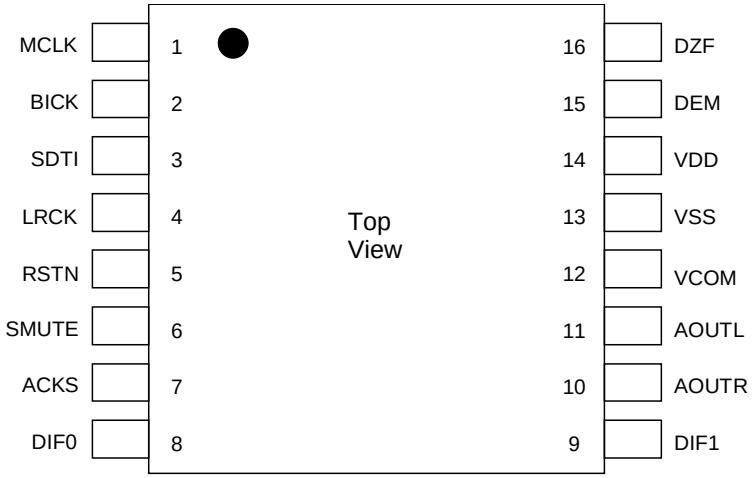
- **Sampling Rate Ranging from 8kHz to 192kHz**
- **128 times Oversampling (Normal Speed Mode)**
- **64 times Oversampling (Double Speed Mode)**
- **32 times Oversampling (Quad Speed Mode)**
- **24-Bit 8 times FIR Digital Filter**
- **SCF with High Tolerance to Clock Jitter**
- **Single Ended Output Buffer**
- **Digital de-emphasis**
- **Soft mute**
- **I/F format: 24-Bit MSB justified, 24/16-Bit LSB justified or $I^2S$**
- **Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)**
  **256fs or 384fs (Double Speed Mode)**
  **128fs, 192fs (Quad Speed Mode)**
- **THD+N: -90dB**
- **Dynamic Range: 106dB**
- **Power supply: 4.5 to 5.5V**
- **Very Small Package: 16pin TSSOP (6.4mm x 5.0mm)**
- **AK4384 Parallel Mode Compatible**



## ■ Ordering Guide

| | | |
|---|---|---|
| AK4388ET | -20 ~ +85°C | 16pin TSSOP (0.65mm pitch) |
| AK4388VT | -40 ~ +85°C | 16pin TSSOP (0.65mm pitch) |
| AKD4388 | Evaluation Board for AK4388 | |

## ■ Pin Layout




## ■ Compatibility with AK4384

### 1. Function

| Functions | AK4384 | AK4388 |
|---|---|---|
| THD+N | -94dB | -90dB |
| Output Voltage | 3.4Vpp | 3.2Vpp |
| Slow Roll-Off Filter | Available | Not Available |
| Mode Setting | Serial/Parallel | Parallel |
| DEM in Parallel control | Not Available | Available |
| Audio Format in Parallel control | 24-Bit $I^2S$<br>24-Bit MSB justified | 24/16-Bit $I^2S$<br>24-Bit MSB justified<br>24/16-Bit LSB justified |
| Zero Data Detect Pin | 2 pins | 1 pin |

### 2. Pin Configuration

| AK4388 | AK4384 | Pin# | Pin# | AK4384 | AK4388 |
|---|---|---|---|---|---|
| MCLK | MCLK | 1 | 16 | DZFL | DZF |
| BICK | BICK | 2 | 15 | DZFR | DEM (pd) |
| SDTI | SDTI | 3 | 14 | VDD | VDD |
| LRCK | LRCK | 4 | 13 | VSS | VSS |
| RSTN | PDN | 5 | 12 | VCOM | VCOM |
| SMUTE | SMUTE/CSN | 6 | 11 | AOUTL | AOUTL |
| ACKS | ACKS/CCLK | 7 | 10 | AOUTR | AOUTR |
| DIF0 | DIF0/CDTI | 8 | 9 | P/S (pu) | DIF1 (pu) |

Different points from AK4384

* pu: Pull-up, pd: Pull-down

## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | MCLK | I | Master Clock Input Pin<br>An external TTL clock should be input on this pin. |
| 2 | BICK | I | Audio Serial Data Clock Pin |
| 3 | SDTI | I | Audio Serial Data Input Pin |
| 4 | LRCK | I | L/R Clock Pin |
| 5 | RSTN | I | Reset Mode Pin<br>When at "L", the AK4388 is in the power-down mode and is held in reset.<br>The AK4388 must be reset once upon power-up. |
| 6 | SMUTE | I | Soft Mute Pin<br>"H": Enable, "L": Disable |
| 7 | ACKS | I | Auto Setting Mode Pin<br>"L": Manual Setting Mode, "H": Auto Setting Mode |
| 8 | DIF0 | I | Audio Data Interface Format Pin |
| 9 | DIF1 | I | Audio Data Interface Format Pin (Internal pull-up pin) |
| 10 | AOUTR | O | Rch Analog Output Pin |
| 11 | AOUTL | O | Lch Analog Output Pin |
| 12 | VCOM | O | Common Voltage Pin, VDD/2<br>Normally connected to VSS with a 10μF electrolytic cap. |
| 13 | VSS | - | Ground Pin |
| 14 | VDD | - | Power Supply Pin |
| 15 | DEM | I | De-emphasis Mode Pin (Internal pull-down pin)<br>When at "H", the de-emphasis filter is available. |
| 16 | DZF | O | Zero Input Detect Pin |

Note: All input pins except pull-up and pull-down pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supply | | VDD | -0.3 | 6.0 | V |
| Input Current (any pins except for supplies) | | IIN | - | ±10 | mA |
| Input Voltage | | VIND | -0.3 | VDD+0.3 | V |
| Ambient Operating Temperature | AK4388ET | Ta | -20 | 85 | °C |
| | AK4388VT | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supply | VDD | 4.5 | 5.0 | 5.5 | V |

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; VDD=5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data;
Measurement frequency=20Hz ~ 20kHz; $R_L \geq 5k\Omega$; unless otherwise specified)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Resolution | | | | | 24 | Bits |
| **Dynamic Characteristics** | | (Note 3) | | | | |
| THD+N | fs=44.1kHz | 0dBFS | | –90 | –80 | dB |
| | BW=20kHz | –60dBFS | | –42 | - | dB |
| | fs=96kHz | 0dBFS | | –90 | - | dB |
| | BW=40kHz | –60dBFS | | –39 | - | dB |
| | fs=192kHz | 0dBFS | | –85 | - | dB |
| | BW=40kHz | –60dBFS | | –39 | - | dB |
| Dynamic Range (-60dBFS with A-weighted) | | (Note 4) | 98 | 106 | | dB |
| S/N (A-weighted) | | (Note 5) | 98 | 106 | | dB |
| Interchannel Isolation (1kHz) | | | 90 | 100 | | dB |
| Interchannel Gain Mismatch | | | | 0.2 | 0.5 | dB |
| **DC Accuracy** | | | | | | |
| Gain Drift | | | | 100 | - | ppm/°C |
| Output Voltage | | (Note 6) | 2.95 | 3.20 | 3.45 | Vpp |
| Load Resistance | | (Note 7) | 5 | | | kΩ |
| Load Capacitance | | | | | 25 | pF |
| **Power Supplies** | | | | | | |
| Power Supply Current (VDD) | | | | | | |
| Normal Operation (RSTN pin = "H", fs ≤ 96kHz) | | | | 16 | - | mA |
| Normal Operation (RSTN pin = "H", fs = 192kHz) | | | | 18 | 27 | mA |
| Power-Down Mode (RSTN pin = "L") | | (Note 8) | | 60 | 160 | μA |

Notes: 3. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
4. 100dB at 16bit data.
5. S/N does not depend on input bit length.
6. Full-scale voltage (0dB). Output voltage scales with the voltage of VDD,
AOUT (typ.@0dB) = 3.20Vpp × VDD/5.
7. For AC-load.
8. DIF1 pin is tied to VDD and the other all digital inputs including clock pins (MCLK, BICK and LRCK) are tied to VSS.

## FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.5 ~ 5.5V; fs = 44.1kHz)

| Parameter | | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|---|
| **Digital filter** (DEM = OFF) | | | | | | | |
| Passband ±0.05dB (Note 9) | | | PB | 0 | | 20.0 | kHz |
| –6.0dB | | | | - | 22.05 | - | kHz |
| Stopband (Note 9) | | | SB | 24.1 | | | kHz |
| Passband Ripple | | | PR | | | ± 0.02 | dB |
| Stopband Attenuation | | | SA | 54 | | | dB |
| Group Delay (Note 10) | | | GD | - | 19.3 | - | 1/fs |
| De-emphasis Filter (DEM = ON) | | | | | | | |
| De-emphasis Error | fs = 32kHz | | | - | - | –1.5/0 | dB |
| (Relative to 0Hz) | fs = 44.1kHz | | | - | - | –0.2/+0.2 | dB |
| | fs = 48kHz | | | - | - | 0/+0.6 | dB |
| **Digital Filter + LPF** (DEM = OFF) | | | | | | | |
| Frequency Response | 20.0kHz | fs=44.1kHz | FR | - | ±0.2 | - | dB |
| | 40.0kHz | fs=96kHz | FR | - | ±0.3 | - | dB |
| | 80.0kHz | fs=192kHz | FR | - | +0.1/-0.6 | - | dB |

Notes: 9. The passband and stopband frequencies scale with fs(system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

## DC CHARACTERISTICS

(Ta=25°C; VDD=4.5 ~ 5.5V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 2.2 | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 0.8 | V |
| High-Level Output Voltage (Iout=-80μA) | VOH | VDD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=80μA) | VOL | - | | 0.4 | V |
| Input Leakage Current (Note 11) | Iin | - | - | ± 10 | μA |

Note: 11. Except DIF1 and DEM pins. DIF1 pin has internal pull-up device, DEM pin has internal pull-down device, nominally 100kΩ.

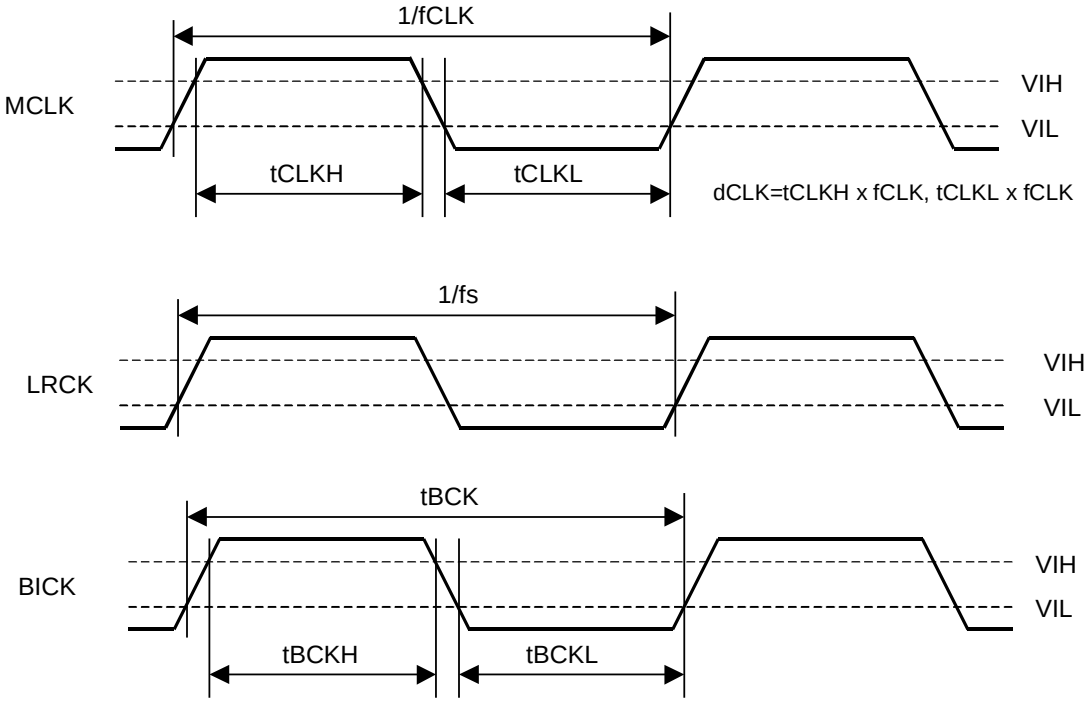
## SWITCHING CHARACTERISTICS

(Ta=25°C; VDD=4.5 ~ 5.5V; $C_L$=20pF)

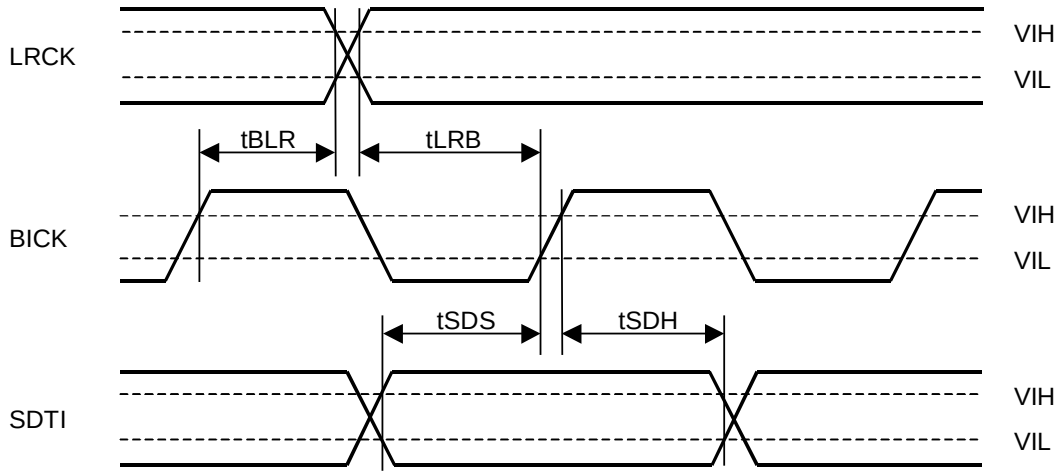
| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Master Clock Frequency** | fCLK | 2.048 | 11.2896 | 36.864 | MHz |
| Duty Cycle | dCLK | 40 | | 60 | % |
| **LRCK Frequency** | | | | | |
| Normal Speed Mode | fsn | 8 | | 48 | kHz |
| Double Speed Mode | fsd | 32 | | 96 | kHz |
| Quad Speed Mode | fsq | 120 | | 192 | kHz |
| Duty Cycle | Duty | 45 | | 55 | % |
| **Audio Interface Timing** | | | | | |
| BICK Period | | | | | |
| Normal Speed Mode | tBCK | 1/128fs | | | ns |
| Double/Quad Speed Mode | tBCK | 1/64fs | | | ns |
| BICK Pulse Width Low | tBCKL | 30 | | | ns |
| Pulse Width High | tBCKH | 30 | | | ns |
| BICK "↑" to LRCK Edge (Note 12) | tBLR | 20 | | | ns |
| LRCK Edge to BICK "↑" (Note 12) | tLRB | 20 | | | ns |
| SDTI Hold Time | tSDH | 20 | | | ns |
| SDTI Setup Time | tSDS | 20 | | | ns |
| **Reset Timing** | | | | | |
| RSTN Pulse Width (Note 13) | tRST | 150 | | | ns |

Notes: 12. BICK rising edge must not occur at the same time as LRCK edge.
13. The AK4388 can be reset by bringing RSTN pin = "L".

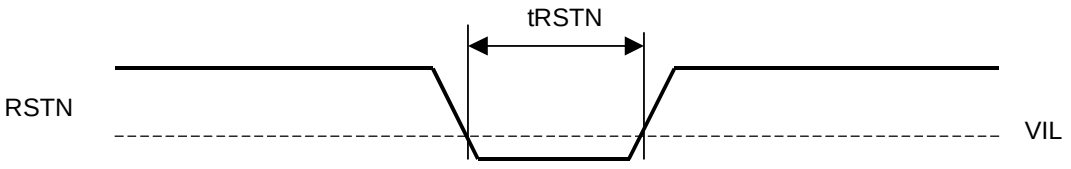
■ **Timing Diagram**




Clock Timing




Serial Interface Timing




Power-down Timing

## OPERATION OVERVIEW

### ■ System Clock

The external clocks, which are required to operate the AK4388, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS pin = "L", Normal Speed Mode), the frequency of MCLK is set automatically (Table 1). After exiting reset (RSTN pin= "↑"), the AK4388 is in Auto Setting Mode. In Auto Setting Mode (ACKS pin = "H"), as MCLK frequency is detected automatically (Table 2), and the internal master clock becomes the appropriate frequency (Table 3).

All external clocks (MCLK,BICK and LRCK) should always be present whenever the AK4388 is in the normal operation mode (RSTN pin = "H"). If these clocks are not provided, the AK4388 may draw excess current and may fall into unpredictable operation. This is because the device utilizes dynamic refreshed logic internally. The AK4388 should be reset by RSTN pin = "L" after these clocks are provided. If the external clocks are not present, the AK4388 should be in the power-down mode (RSTN pin = "L"). After exiting reset at power-up etc., the AK4388 is in the power-down mode until MCLK and LRCK are input.

| LRCK | MCLK | | | | | BICK |
|---|---|---|---|---|---|---|
| fs | 256fs | 384fs | 512fs | 768fs | 1152fs | 64fs |
| 32.0kHz | 8.1920MHz | 12.2880MHz | 16.3840MHz | 24.5760MHz | 36.8640MHz | 2.0480MHz |
| 44.1kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz | N/A | 2.8224MHz |
| 48.0kHz | 12.2880MHz | 18.4320MHz | 24.5760MHz | 36.8640MHz | N/A | 3.0720MHz |

Table 1. System Clock Example (Manual Setting Mode, ACKS pin = "L", Normal Speed Mode)

| MCLK | | Mode | Sampling Rate |
|---|---|---|---|
| 1152fs | | Normal | 8kHz~32kHz |
| 512fs | 768fs | Normal | 8kHz~48kHz |
| 256fs | 384fs | Double | 32kHz~96kHz |
| 128fs | 192fs | Quad | 120kHz~192kHz |

Table 2. Sampling Speed (Auto Setting Mode, ACKS pin = "H")

| LRCK | MCLK (MHz) | | | | | | |
|---|---|---|---|---|---|---|---|
| fs | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1152fs |
| 32.0kHz | - | - | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 36.8640 |
| 44.1kHz | - | - | 11.2896 | 16.9344 | 22.5792 | 33.8688 | - |
| 48.0kHz | - | - | 12.2880 | 18.4320 | 24.5760 | 36.8640 | - |
| 88.2kHz | - | - | 22.5792 | 33.8688 | - | - | - |
| 96.0kHz | - | - | 24.5760 | 36.8640 | - | - | - |
| 176.4kHz | 22.5792 | 33.8688 | - | - | - | - | - |
| 192.0kHz | 24.5760 | 36.8640 | - | - | - | - | - |

Table 3. System Clock Example (Auto Setting Mode, ACKS pin = "H")

When MCLK= 256fs/384fs, the Auto Setting Mode supports sampling rate of 32kHz~96kHz (Table 2). But, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

| ACKS pin | MCLK | DR,S/N |
|---|---|---|
| L | 256fs/384fs/512fs/768fs | 106dB |
| H | 256fs/384fs | 103dB |
| H | 512fs/768fs | 106dB |

Table 4. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

## ■ Audio Serial Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0-1 as shown in Table 5 can select four serial data modes. DIF1 pin is internal pull-up pin. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK.

| Mode | DIF1 | DIF0 | SDTI Format | BICK | Figure |
|---|---|---|---|---|---|
| 0 | L | L | 16bit MSB justified | ≥32fs | Figure 1 |
| 1 | L | H | 24bit MSB justified | ≥48fs | Figure 2 |
| 2 | H | L | 24bit LSB justified | ≥48fs | Figure 3 |
| 3 | H | H | 16/24bit $I^2S$ Compatible | ≥48fs or 32fs | Figure 4 |

Table 5. Audio Data Formats

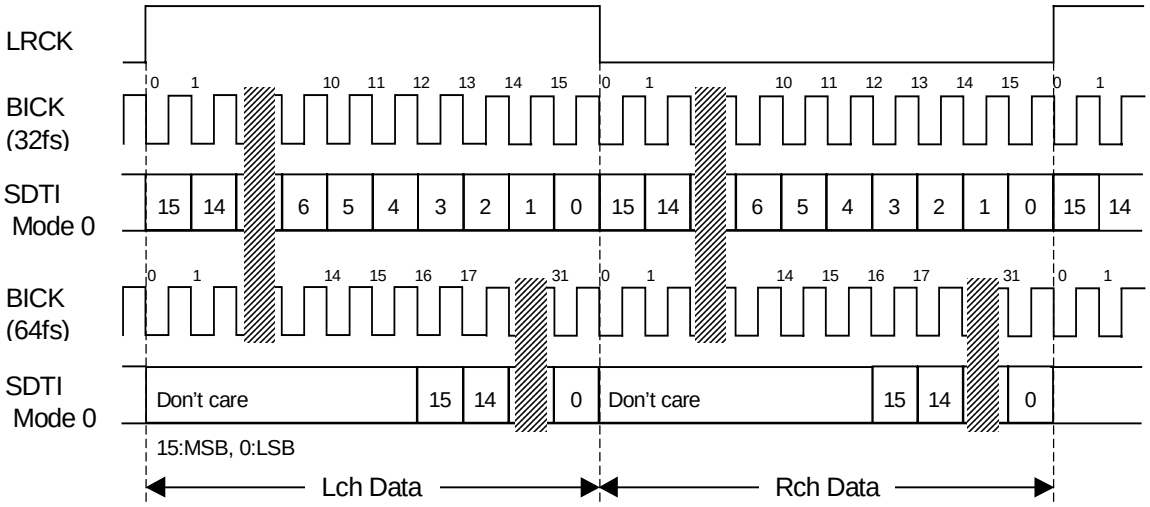



Figure 1. Mode 0 Timing

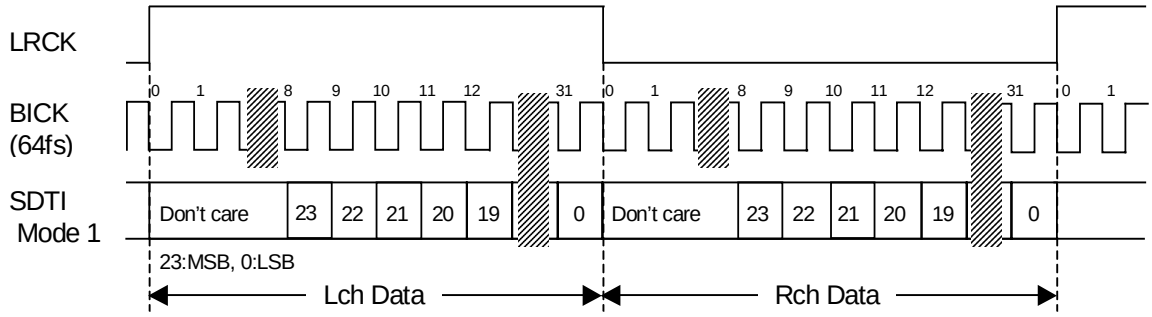



Figure 2. Mode 1 Timing

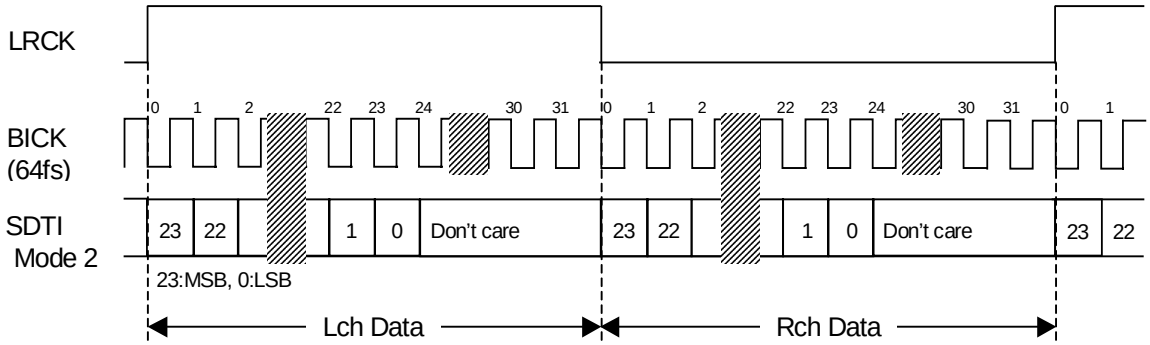



Figure 3. Mode 2 Timing

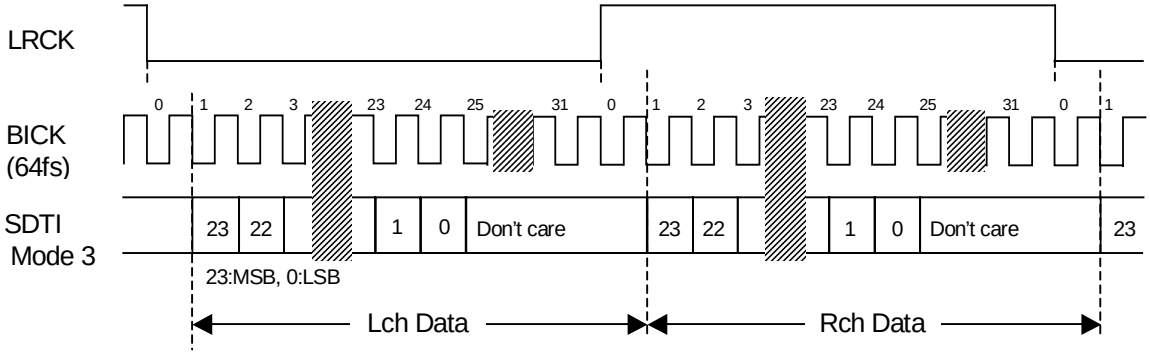



Figure 4. Mode 3 Timing

## ■ De-emphasis Filter

A digital de-emphasis filter is built-in (tc = 50/15μs). DEM pin is internal pull-down pin. The digital de-emphasis filter is enabled by setting DEM pin "H". Refer to the section of "FILTER CHARACTERISTICS" regarding the gain error when the de-emphasis filter is enabled.

| DEM pin | De-emphasis Filter | |
|---|---|---|
| 1 | ON | |
| 0 | OFF | Default |

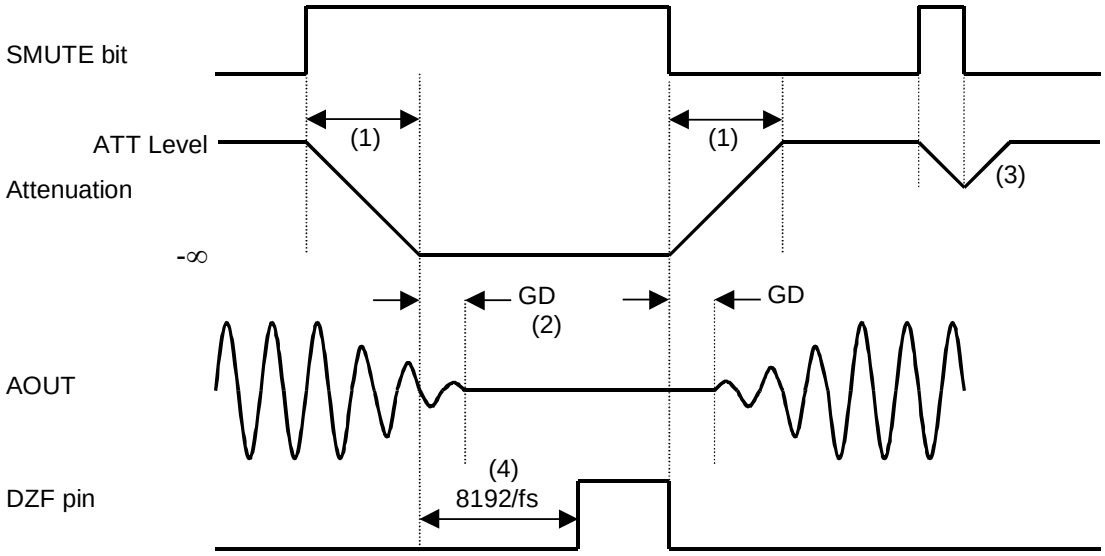
Table 6. De-emphasis Filter Control

## ■ Zero Detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF pin goes to "H". DZF pin immediately goes to "L" if input data of both channels are not zero after going DZF "H"(Figure 5).

## ■ Soft Mute Operation

Soft mute operation is performed at digital domain. When the SMUTE pin goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When the SMUTE pin is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within the 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.




Notes:

(1) 1020LRCK cycles (1020/fs) at input data is attenuated to -∞.
(2) The analog output corresponding to the digital input has a group delay, GD.
(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(4) When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF pin goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF "H".

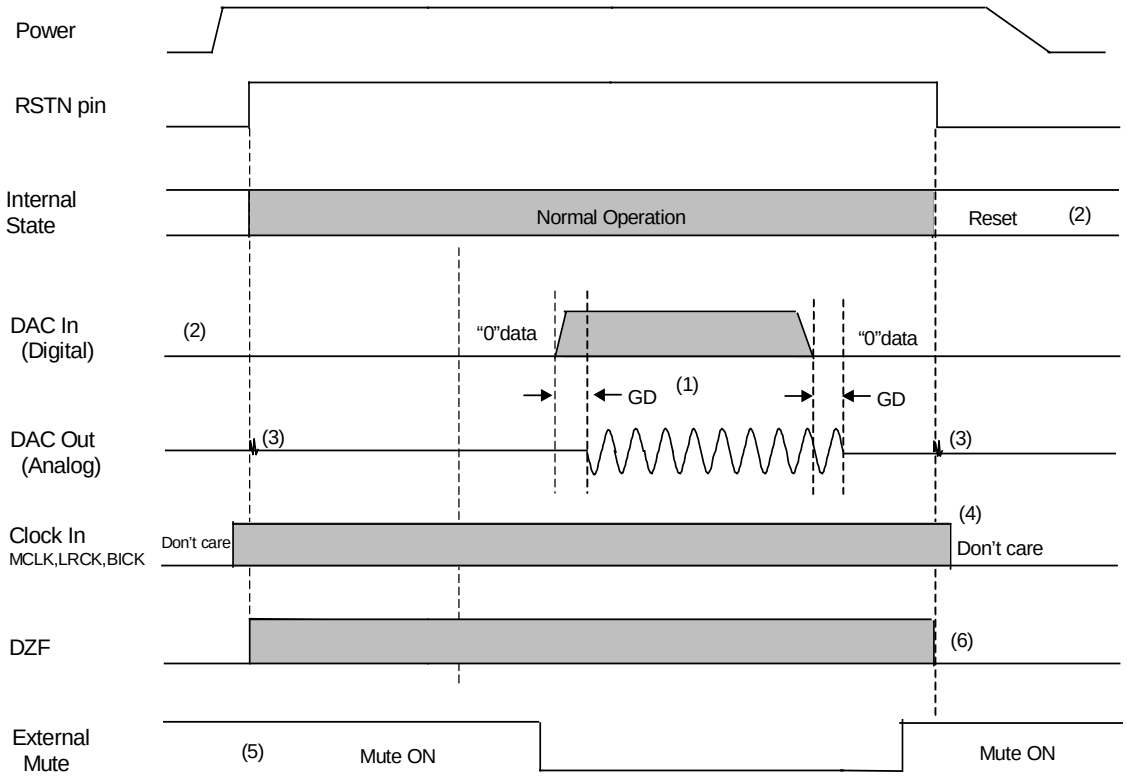
Figure 5. Soft Mute and Zero Detection

## ■ System Reset

The AK4388 must be reset once by bringing RSTN pin = "L" upon power-up. The AK4388 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4388 is in the power-down mode until LRCK are input.

## ■ Power ON/OFF timing

AK4388 is placed in the power-down mode by bringing RSTN pin "L" and the registers are initialized. The analog outputs go to VCOM (VDD/2). Since some click noise occurs at the edge of the RSTN signal, the analog output should be muted externally if the click noise influences system application.




Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are VCOM (VDD/2) in power-down mode.
(3) Click noise occurs at the edge of RSTN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (RSTN pin = "L").
(5) Mute the analog output externally if the click noise (3) influences the system application.
The timing example is shown in this figure.
(6) DZF pins are "L" in the power-down mode (RSTB pin = "L").

Figure 6. Power-down/up Sequence Example

## SYSTEM DESIGN

Figure 7 shows the system connection diagram. An evaluation board (AKD4388) is available in order to allow an easy study on the layout of a surrounding circuit.

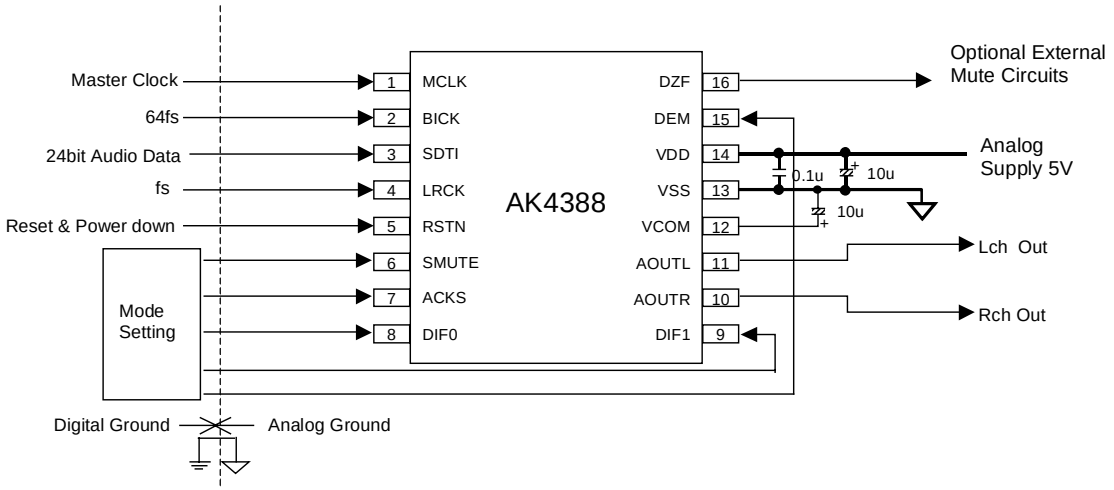



Figure 7. Typical Connection Diagram

Notes:

- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except DIF1 and DEM pins should not be left floating.

## 1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to VDD as possible. The differential Voltage between VDD and VSS pins set the analog output range.

## 2. Analog Outputs

The analog outputs are single-ended and centered around the VCOM voltage. The output signal range is typically 3.20Vpp (typ@VDD=5V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV. Figure 8 shows an example of the external LPF with 3.20Vpp (1.13Vrms) output. Figure 9 shows an example of the external LPF with 2Vrms output.

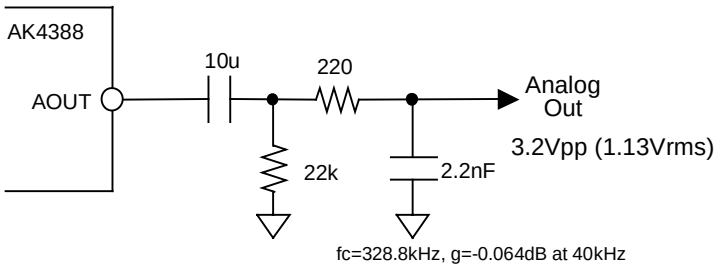



Figure 8. External 1st order LPF Circuit Example (simple)

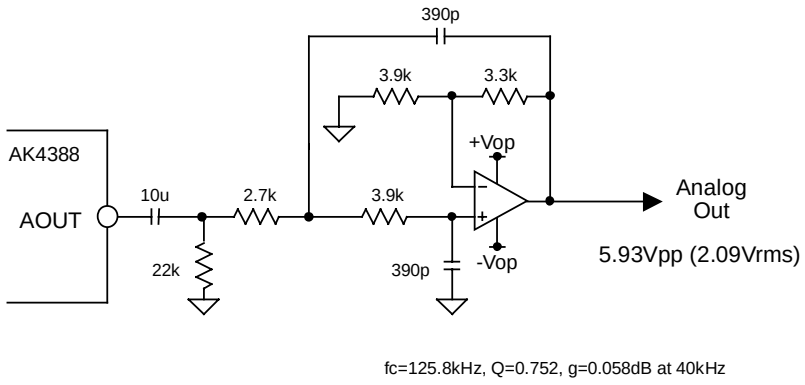
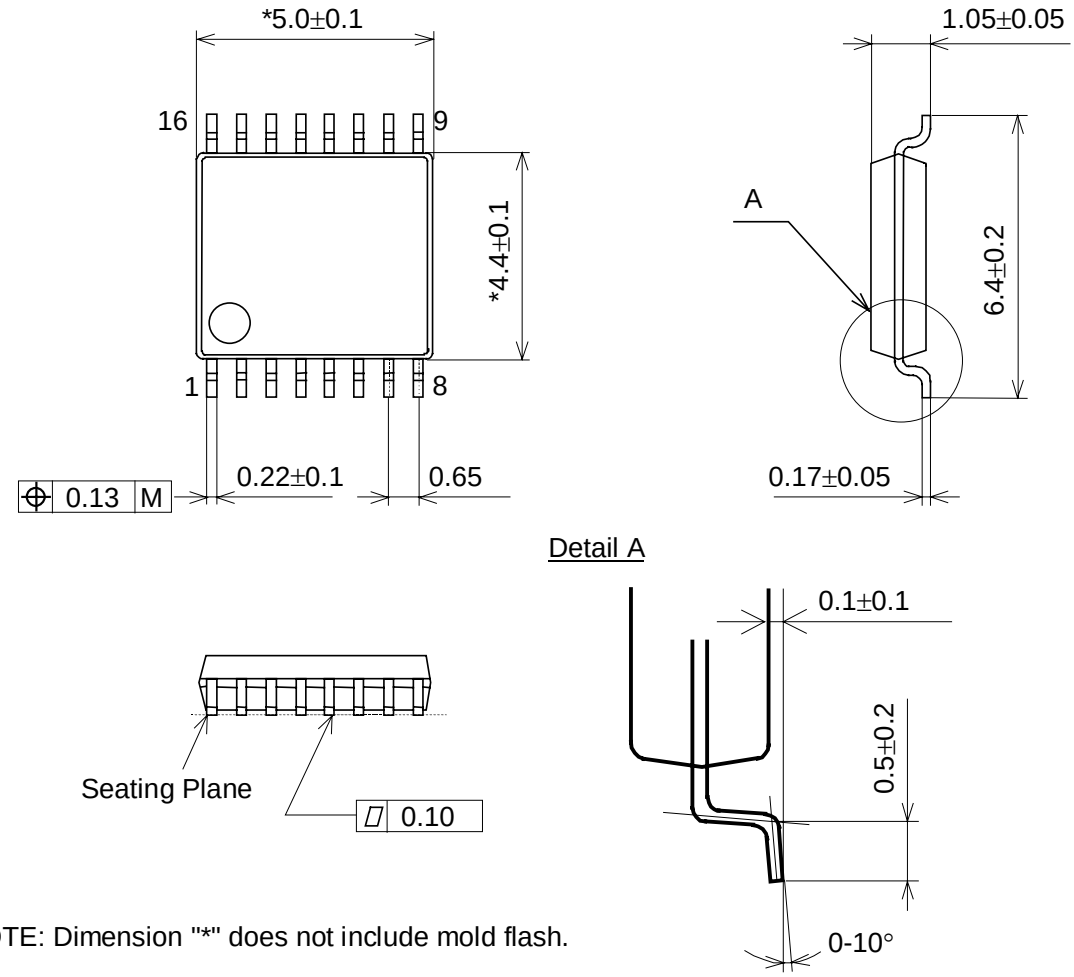



Figure 9. External 2nd order LPF Circuit Example (using op-amp with dual power supplies)

## PACKAGE

16pin TSSOP (Unit: mm)

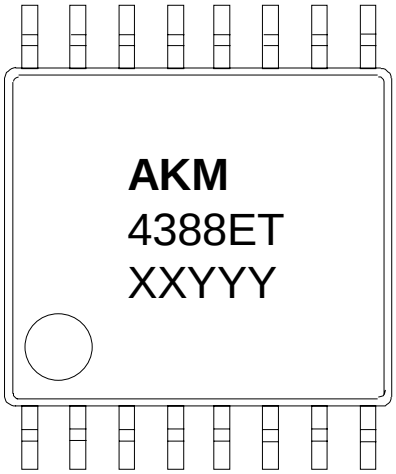



NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

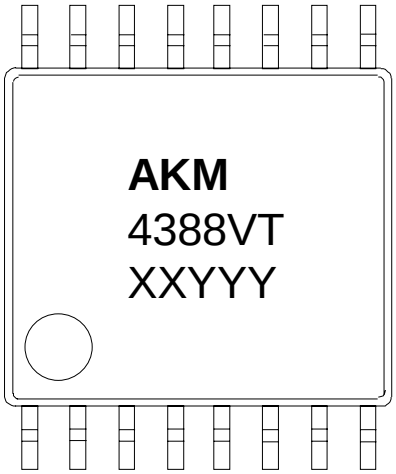
| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

## MARKING (AK4388ET)




1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4388ET
4) Asahi Kasei Logo

## MARKING (AK4388VT)




1) Pin #1 indication
2) Data Code : XXYYY(5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4388VT
4) Asahi Kasei Logo

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 06/04/24 | 00 | First edition | | |
| 06/07/28 | 00 | Error Correction | 12 | Figure 6<br>DZF1/DZF2 → DZF<br>"(6) DZF pins are "L" in the power-down mode (RSTB pin = "L")." was added. |
| | | | 14 | Figure 8<br>fc=154kHz, g=0.284dB at 40kHz →<br>fc=328.8kHz, g=-0.064dB at 40kHz |