

SED1530 Series

Dot Matrix LCD Controller Driver

- Ultra Low Power Consumption
- Built-in Power Supply Circuit for LCD
- 133 Driver Output

■ DESCRIPTION

The SED1530 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's) which is directly connectable to a microcomputer bus. It accepts 8-bit serial or parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of microprocessor clock.

The use of the on-chip display RAM of 65×132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

As a total of 133 circuits of common and segment outputs are incorporated, a single chip of SED1530 series can make 33×100 -dot (16×16 -dot kanji font: 6 columns $\times$ 2 lines) displays, and a single chip of SED1531 can make 65×132 -dot (kanji font: 8 columns $\times$ 4 lines) displays when the SED1531 is combined with the common driver SED1635.

The SED1532 can display the 65×200 -dot (or 12-column by 4-line Kanji font) area using two ICs in master and slave modes. As an independent static indicator display is provided for time-division driving, the low-power display is realized during system standby and others.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with a minimum current consumption and a smallest LSI configuration.

Two types of SED1530 series are available: one in which common outputs are arranged on a single side and the other in which common outputs are arranged on both sides.

■ FEATURES

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (At normal display)
- RAM capacity: $65 \times 132 = 8580$ bits
- High-speed 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800.
- Serial interface
- Many command functions: Read/Write Display Data, Display ON/OFF, Normal/Reverse Display, Page Address Set, Set Display Start Line, Set Column Address, Read Status, All Display ON/OFF, Set LCD Bias, Electronic contrast Controls, Read Modify Write, Select Segment Driver Direction, Power Save

SED1530 Series

LINE UP

Type 1 [VREG Temperature gradient 0.2% / °C]

• Specifications (for chip models)

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
SED1530D0*	1/33	1/5, 1/6	100	33	33 × 100	COM single-side assignment
SED1530DA*	1/33	1/5, 1/6	100	33	33 × 100	COM dual-side assignment
SED1531D0*	1/65	1/6, 1/8	132	0	65 × 132	SED1635 is used for COM.
SED1532D0*	1/65	1/6, 1/8	100	33	65 × 200	COM single-side right assignment
SED1532DB*	1/65	1/6, 1/8	100	33	65 × 200	COM single-side left assignment

Type 2 [VREG Temperature gradient 0.00% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
SED1530DF*	1/33	1/5, 1/6	100	33	33 × 100	COM both-side layout
SED1532DE*	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
SED1533DF*	1/17	1/5	116	17	17 × 116	COM both-side layout
SED1534DE*	1/9	1/5	124	9	9 × 124	COM single-side layout

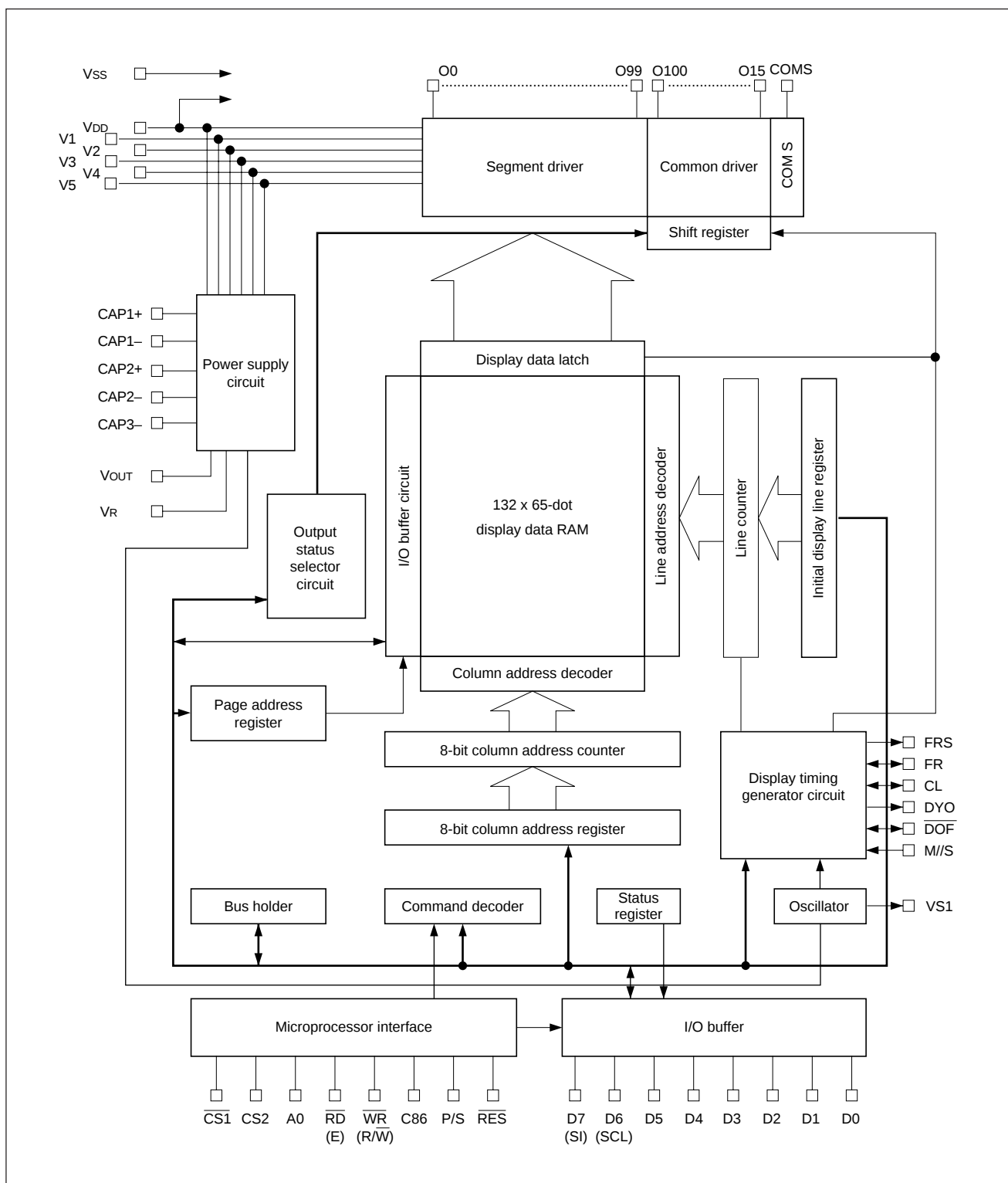
Note: The SED1530 series has the following subcodes depending on their shapes. (The SED1530 examples are given.)

SED1530T** : TCP (The TCP subcode differs from the inherent chip subcode.)

SED1530D** : Bear chips — SED1530D*A : Aluminum pad
 SED1530D*B : Gold bump

- On-chip LCD power circuit: Liquid crystal driving power supply booster circuit, voltage regulator circuit, voltage follower × 4.
- On-chip electronic contrast control functions
- Ultra low power consumption
- Power supply voltages: VDD - VSS -2.4 V to -6.0 V
 VDD - V5 -4.5 V to -16.0 V (In the case of external power supply)
- Wide operating temperature range:
 Ta = -40 to 85°C
- CMOS process
- Package: TCP and bare chip
- Non-radiation-resistant design

■ BLOCK DIAGRAM (SED1530D0B)



SED1530 Series

PIN LAYOUT



Chip Size: 6.65x4.57 mm
Pad Pitch: 118 μm (Min.)

SED153*D*A (Aluminum pad model)
Pad Center Size: 90x90 μm
Chip Thickness: 300 μm

SED153*D*B (Gold bump model)
Bump Size: 76x76 μm
Bump Height: 23 μm (Typ.)
Chip Thickness: 625 μm

■ PAD CENTER COORDINATES

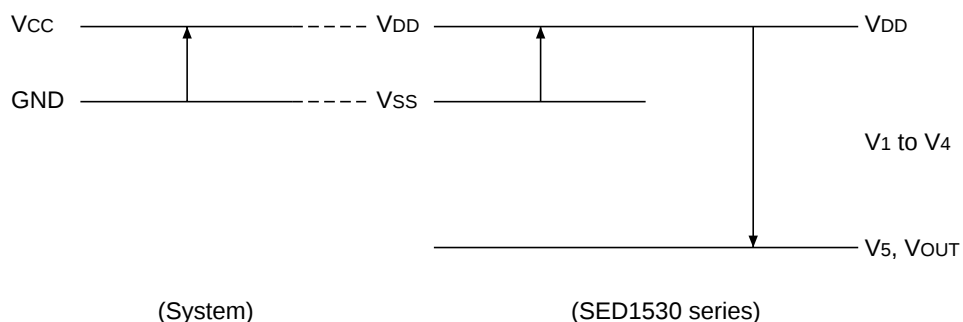
Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	0127	2986	2142	51	O5	-2986	2142	101	O55	-1298	-2142	151	O105	3178	-472
2	0128	2862		52	O6	-3178	2006	102	O56	-1180		152	O106		-354
3	0129	2738		53	O7		1888	103	O57	-1062		153	O107		-236
4	0130	2614		54	O8		1770	104	O58	-944		154	O108		-118
5	0131	2490		55	O9		1652	105	O59	-826		155	O109		0
6	COMS	2366		56	O10		1534	106	O60	-708		156	O110		118
7	FRS	2242		57	O11		1416	107	O61	-590		157	O111		236
8	FR	2124		58	O12		1298	108	O62	-472		158	O112		354
9	DYO	2006		59	O13		1180	109	O63	-354		159	O113		472
10	CL	1888		60	O14		1062	110	O64	-236		160	O114		590
11	$\overline{\text{DOF}}$	1770		61	O15		944	111	O65	-118		161	O115		708
12	VS1	1652		62	O16		826	112	O66	0		162	O116		826
13	M/S	1534		63	O17		708	113	O67	118		163	O117		944
14	$\overline{\text{RES}}$	1416		64	O18		590	114	O68	236		164	O118		1062
15	P/S	1298		65	O19		472	115	O69	354		165	O119		1180
16	CS1	1180		66	O20		354	116	O70	472		166	O120		1298
17	CS2	1062		67	O21		236	117	O71	590		167	O121		1416
18	C86	944		68	O22		118	118	O72	708		168	O122		1534
19	A0	826		69	O23		0	119	O73	826		169	O123		1652
20	$\overline{\text{WR}}(\overline{\text{WR}})$	708		70	O24		-118	120	O74	944		170	O124		1770
21	$\overline{\text{RD}}(\text{E})$	590		71	O25		-236	121	O75	1062		171	O125		1888
22	V _{DD}	354		72	O26		-354	122	O76	1180		172	O126		2006
23	D0	236		73	O27		-472	123	O77	1298					
24	D1	236		74	O28		-590	124	O78	1416					
25	D2	118		75	O29		-708	125	O79	1534					
26	D3	0		76	O30		-826	126	O80	1652					
27	D4	-118		77	O31		-944	127	O81	1770					
28	D5	-236		78	O32		-1062	128	O82	1888					
29	D6(SCL)	-354		79	O33		-1180	129	O83	2006					
30	D7(SI)	-472		80	O34		-1298	130	O84	2124					
31	V _{SS}	-590		81	O35		-1416	131	O85	2242					
32	V _{OUT}	-708		82	O36		-1534	132	O86	2366					
33	CAP3-	-826		83	O37		-1652	133	O87	2490					
34	CAP1+	-944		84	O38		-1770	134	O88	2614					
35	CAP1-	-1062		85	O39		-1888	135	O89	2738					
36	CAP2+	-1180		86	O40		-2006	136	O90	2862					
37	CAP2-	-1298		87	O41	-2986	-2142	137	O91	2986					
38	V ₅	-1416		88	O42	-2862		138	O92	3178	-2006				
39	V _R	-1534		89	O43	-2738		139	O93		-1888				
40	V _{DD}	-1652		90	O44	-2614		140	O94		-1770				
41	V ₁	-1770		91	O45	-2490		141	O95		-1652				
42	V ₂	-1888		92	O46	-2366		142	O96		-1534				
43	V ₃	-2006		93	O47	-2242		143	O97		-1416				
44	V ₄	-2124		94	O48	-2124		144	O98		-1298				
45	V ₅	-2242		95	O49	-2006		145	O99		-1180				
46	O0	-2366		96	O50	-1888		146	O100		-1062				
47	O1	-2490		97	O51	-1770		147	O101		-944				
48	O2	-2614		98	O52	-1652		148	O102		-826				
49	O3	-2738		99	O53	-1534		149	O103		-708				
50	O4	-2862		100	O54	-1416		150	O104		-590				

SED1530 Series

■ ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply voltage range		V_{DD}	-0.3 to +7.0	V
	Triple boosting		-0.3 to +6.0	
	Quadruple boosting		-0.3 to +4.5	
Supply voltage range (1) (V_{DD} Level)		V_5, V_{OUT}	-18.0 to +0.3	V
Supply voltage range (2) (V_{DD} Level)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage range		V_{IN}	-0.3 to $V_{DD}+0.3$	V
Output voltage range		V_O	-0.3 to $V_{DD}+0.3$	V
Operating temperature range		T_{OPR}	-40 to +85	°C
Storage temperature range	TCP	T_{STR}	-55 to +100	°C
	Bear chip		-55 to +125	



- Notes:
1. V_1 to V_5 and V_{OUT} voltages are based on $V_{DD}=0$ V.
 2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must always be satisfied.
 3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{SS} = 0 V, V_{DD} = 5 V ±10%, Ta = −40 to +85°C unless otherwise noted.)

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used	
Power voltage(1)		V _{DD}			4.5	5.0	5.5	V	V _{SS} *1	
					2.4	—	6.0			
Operating voltage (2)		V ₅	V _{DD} level (V _{DD} = 0 V)		−16.0	—	−4.5	V	V ₅ *2	
		V ₁ , V ₂	V _{DD} level (V _{DD} = 0 V)		0.4 × V ₅	—	V _{DD}	V	V ₁ , V ₂	
		V ₃ , V ₄	V _{DD} level (V _{DD} = 0 V)		V ₅	—	0.6 × V ₅	V	V ₃ , V ₄	
CMOS	High-level input voltage		V _{IHC}		0.7 × V _{DD}	—	V _{DD}	V	*3	
				V _{DD} = 2.7 V	0.8 × V _{DD}	—	V _{DD}		*3	
	Low-level input voltage		V _{ILC}		V _{SS}	—	0.3 × V _{DD}	V	*3	
				V _{DD} = 2.7 V	V _{SS}	—	0.2 × V _{DD}		*3	
	High-level output voltage		V _{OHC}	I _{OH} = −1 mA	0.8 × V _{DD}	—	V _{DD}	V	*5	
				V _{DD} = 2.7 V, I _{OH} = −0.5 mA	0.8 × V _{DD}	—	V _{DD}		*5	
	Low-level output voltage		V _{OLC}	I _{OL} = 1 mA	V _{SS}	—	0.2 × V _{DD}	V	*5	
				V _{DD} = 2.7 V, I _{OL} = 0.5 mA	V _{SS}	—	0.2 × V _{DD}		*5	
Schmitt	High-level input voltage		V _{IHS}		0.85 × V _{DD}	—	V _{DD}		*4	
				V _{DD} = 2.7 V	0.8 × V _{DD}	—	V _{DD}		*4	
	Low-level input voltage		V _{ILS}		V _{SS}	—	0.15 × V _{DD}		*4	
				V _{DD} = 2.7 V	V _{SS}	—	0.2 × V _{DD}		*4	
Input leakage current			I _{LI}	V _{IN} = V _{DD} or V _{SS}		−1.0	—	1.0	μA	*6
Output leakage current			I _{LO}			−3.0	—	3.0	μA	*7
LCD driver ON resistance			R _{ON}	Ta = 25°C	V ₅ = −14.0 V	—	2.0	3.0	KΩ	SEG n COM n *8
				V _{DD} level	V ₅ = −8.0 V	—	3.0	4.5		
Static current consumption			I _{SSQ}	V _{IN} = V _{DD} or V _{SS}		—	0.01	5.0	μA	V _{SS}
			I _{5Q}	V ₅ = −18.0 V (V _{DD} level)		—	0.01	15.0	μA	V ₅
Input pin capacity			C _{IN}	Ta = 25°C, f = 1 MHz		—	5.0	8.0	pF	*3 *4
Oscillation frequency			f _{OSC}	Ta = 25°C	V _{DD} = 5 V	18	22	26	kHz	*9
					V _{DD} = 2.7 V	18	22	26		
Built-in power circuit	Input voltage		V _{DD}	Triple boosting		2.4	—	6.0	V	*10
				Quadruple boosting		2.4	—	4.5		
	Booster output voltage		V _{OUT}	Triple voltage conversion (V _{DD} level)		−18.0	—	—	V	V _{OUT}
	Voltage regulator operation voltage		V _{OUT}	(V _{DD} level)		−18.0	—	−6.0	V	V _{OUT}
	Voltage follower operation voltage		V ₅	(V _{DD} level)		−18.0	—	−6.0	V	*11
						−16.0	—	−4.5		
Reference voltage		V _{REG}	Ta = 25°C (V _{DD} level)		−2.75	−2.55	−2.35	V		

SED1530 Series

● Dynamic current consumption (1) when the built-in power supply is OFF

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SED1530	I _{DD} (1)	V _{DD} = 5.0 V, V ₅ – V _{DD} = –8.0 V	—	24	40	μA	*12
		V _{DD} = 3.0 V, V ₅ – V _{DD} = –8.0 V	—	22	35		
SED1531		V _{DD} = 5.0 V, V ₅ – V _{DD} = –11.0 V	—	40	65		
		V _{DD} = 3.0 V, V ₅ – V _{DD} = –11.0 V	—	36	60		
SED1532		V _{DD} = 5.0 V, V ₅ – V _{DD} = –11.0 V	—	39	65		
		V _{DD} = 3.0 V, V ₅ – V _{DD} = –11.0 V	—	32	55		
SED1533		V _{DD} = 3.0 V, V ₅ – V _{DD} = –5.0 V	—	20	35		
SED1534		V _{DD} = 3.0 V, V ₅ – V _{DD} = –5.0 V	—	20	35		

● Dynamic current consumption (2) when the built-in power supply is ON

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SED1530	(1)	V _{DD} = 5.0 V, V ₅ – V _{DD} = –8.0 V, dual boosting	—	41	70	μA	*13
		V _{DD} = 3.0 V, V ₅ – V _{DD} = –8.0 V, triple boosting	—	48	80		
SED1531		V _{DD} = 5.0 V, V ₅ – V _{DD} = –11.0 V, triple boosting	—	96	160		
		V _{DD} = 3.0 V, V ₅ – V _{DD} = –11.0 V, quadruple boosting	—	118	190		
SED1532		V _{DD} = 5.0 V, V ₅ – V _{DD} = –11.0 V, triple boosting	—	95	160		
		V _{DD} = 3.0 V, V ₅ – V _{DD} = –11.0 V, quadruple boosting	—	114	190		
SED1533		V _{DD} = 3.0 V, V ₅ – V _{DD} = –5.0 V, dual boosting	—	30	50		
SED1534		V _{DD} = 3.0 V, V ₅ – V _{DD} = –5.0 V, dual boosting	—	32	55		

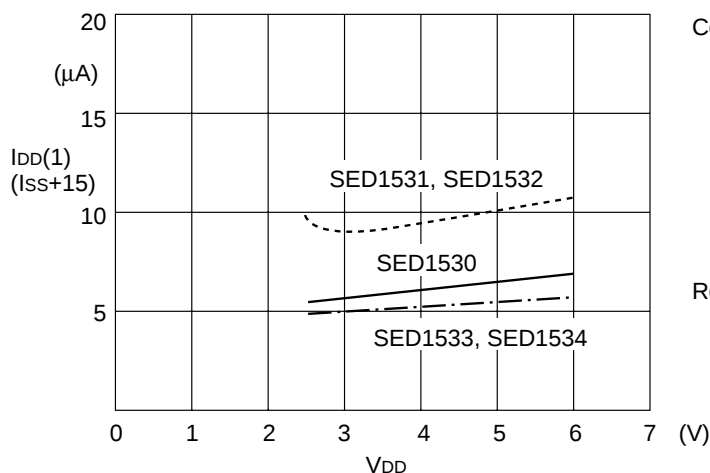
● Current consumption during Power Save mode

V_{SS}=0V, V_{DD}=2.7 to 5.5V Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
During sleep	I _{DD} S1	SED1530, SED1531, SED1532	—	0.01	1	μA	
During standby	I _{DD} S2	SED1530, SED1531, SED1532	—	10	20		

● Typical current consumption characteristics (reference data)

- Dynamic current consumption (1) when LCD external power mode lamp is ON



Conditions: The built-in power supply is OFF and an external power supply is used.

SED1530 V₅-V_{DD} = -8.0V

SED1531 V₅-V_{DD} = -11.0V

SED1532 V₅-V_{DD} = -11.0V

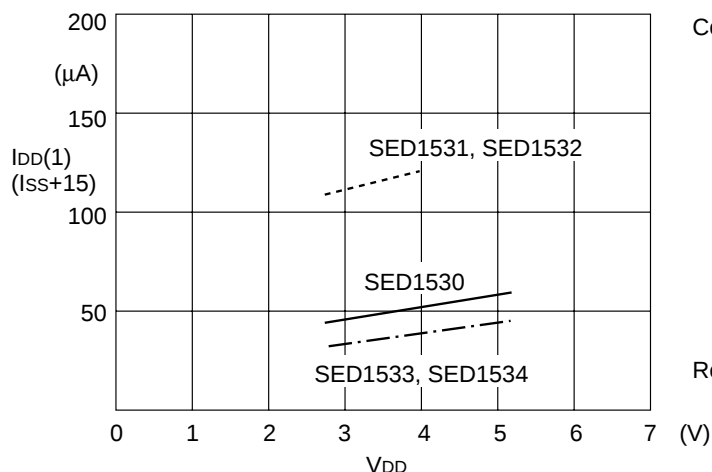
SED1533 V₅-V_{DD} = -6.0V

SED1534 V₅-V_{DD} = -6.0V

Ta = 25°C

Remarks: *12

- Dynamic current consumption (2) when the LCD built-in power circuit lamp is ON



Conditions: The built-in power supply is ON.
 SED1530 $V_5-V_{DD} = -8.0V$, triple boosting
 SED1531 $V_5-V_{DD} = -11.0V$, quadruple boosting
 SED1532 $V_5-V_{DD} = -11.0V$, quadruple boosting
 SED1533 $V_5-V_{DD} = -5.0V$, dual boosting
 SED1534 $V_5-V_{DD} = -5.0V$, dual boosting
 $T_a = 25^\circ C$

Remarks: *13

- *1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the microprocessor.
- *2 V_{DD} and V_5 operating voltage range. (Refer to Fig.)
The operating voltage range applies if an external power supply is used.
- *3 A0, D0 - D5, D6, D7 (SI), RD (E), WR (R/W), CS1, CS2, FR, M/S, C86, P/S and $\overline{DOF}$ pins
- *4 CL, SCL (D6) and RES pins
- *5 D0 - D5, D6, D7 (SI), FR, FRS, DYO, $\overline{DOF}$ and CL pins
- *6 A0, RD (E), WR (R/W), CS1, CS2, M/S, RES, C86 and P/S pins
- *7 Applies when the D0 - D7, FR, CL, DYO and $\overline{DOF}$ pins are in high impedance,
- *8 Resistance value when 0.1 V is applied between the output pin SEGn or COMn and each power supply pin (V_1 , V_2 , V_3 , V_4).
This is specified in the operating voltage (2) range.
 $R_{ON} = 0.1 V / \Delta I$ (ΔI : Current flowing when 0.1 V is applied in the ON status.)
- *9 For the relationship between oscillation frequency and frame frequency. (Refer to Fig.)
- *10 For triple or quadruple boosting using the on-chip power using the primary-side power supply V_{DD} must be used within the input voltage range.
- *11 The voltage regulator adjusts V_5 within the voltage follower operating voltage range.
- *12, *13 Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc.
This is current consumption under the conditions of display data = checker, display ON, SED1530 = 1/33 duty, and SED1531 and SED1532 = 1/65 duty.
- *12 Applies to the case where the on-chip oscillator circuit is used and no access is made from the microprocessor.
- *13 Applies to the case where the on-chip oscillator circuit and the on-chip power circuit are used and no access is made from the microprocessor.
The current flowing through voltage regulation resistors (R_1 , R_2 and R_3) is not included.
The current consumption, when the on-chip voltage booster is used, is for the power supply V_{DD} .

- Relationship between oscillation frequency and frame frequency
The relationship between oscillation frequency f_{osc} and LCD frame frequency f_F can be obtained by the following expression.

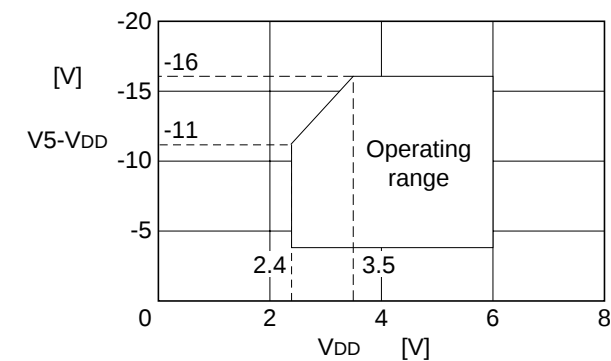
	Duty	f_{CL}	f_F
SED1530	1/33	$f_{osc}/8$	$f_{osc}/(8*33)$
SED1531 SED1532	1/65	$f_{osc}/4$	$f_{osc}/(4*65)$
SED1533	1/17	$f_{osc}/8$	$f_{osc}/(8*17)$
SED1534	1/9	$f_{osc}/8$	$f_{osc}/(8*9)$

(f_F does not indicate the FR signal cycle but the AC cycle.)

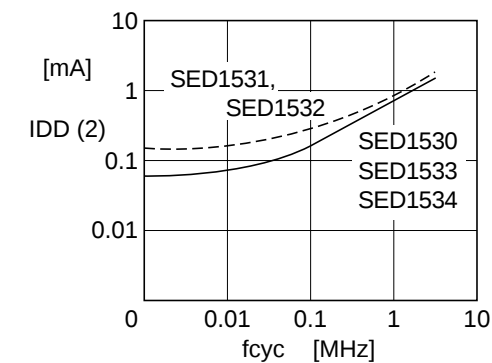
Relationship between clock (f_{CL}) and frame frequency f_F

SED1530 Series

- Vss and V5 operating voltage range



- Current consumption at access IDD (2) - Microprocessor access cycle



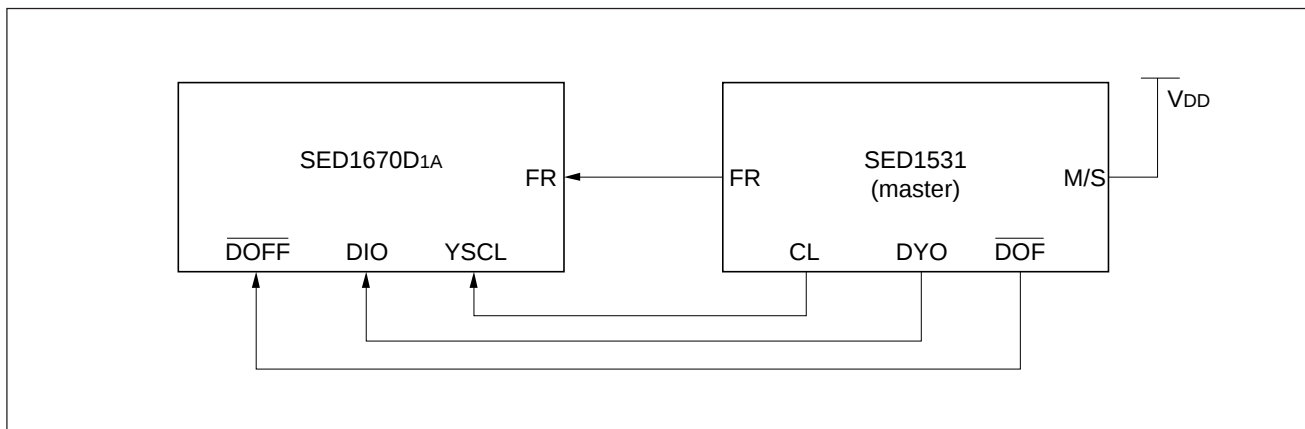
This indicates current consumption when data is always written on the checker pattern at fcyc. When no access is made, only IDD (1) occurs.

Condition: SED1530 V5-VDD=−8.0V, triple boosting
 SED1531 V5-VDD=−11.0V, quadruple boosting
 SED1532 V5-VDD=−11.0V, quadruple boosting
 SED1533 V5-VDD=−6.0V, dual boosting
 SED1534 V5-VDD=−6.0V, dual boosting
 Ta = 25°C

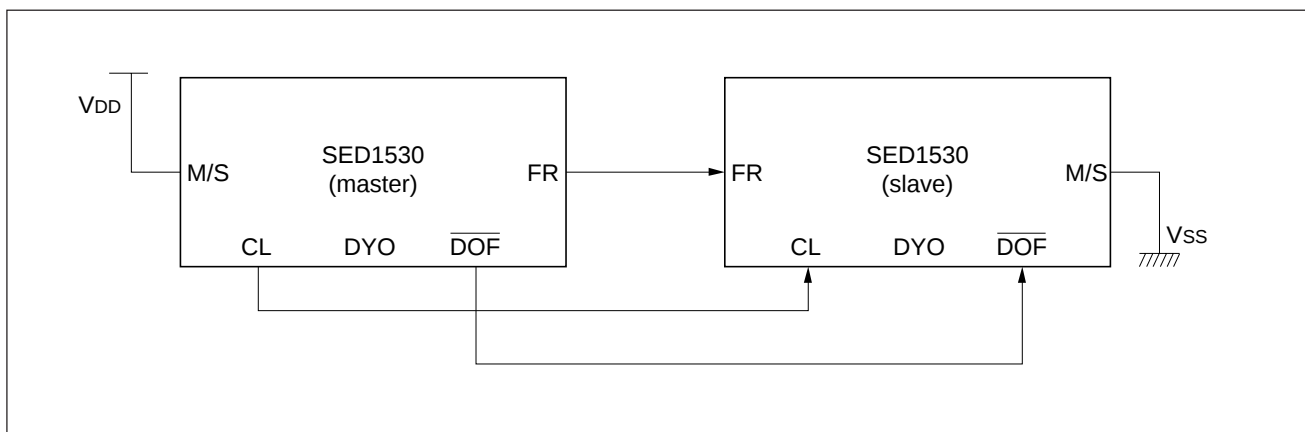
■ CONNECTION BETWEEN LCD Drivers

The LCD panel display area can easily be expanded by use of multiple SED1530 series chips. The SED1530 series can also be connected to the common driver (SED1670).

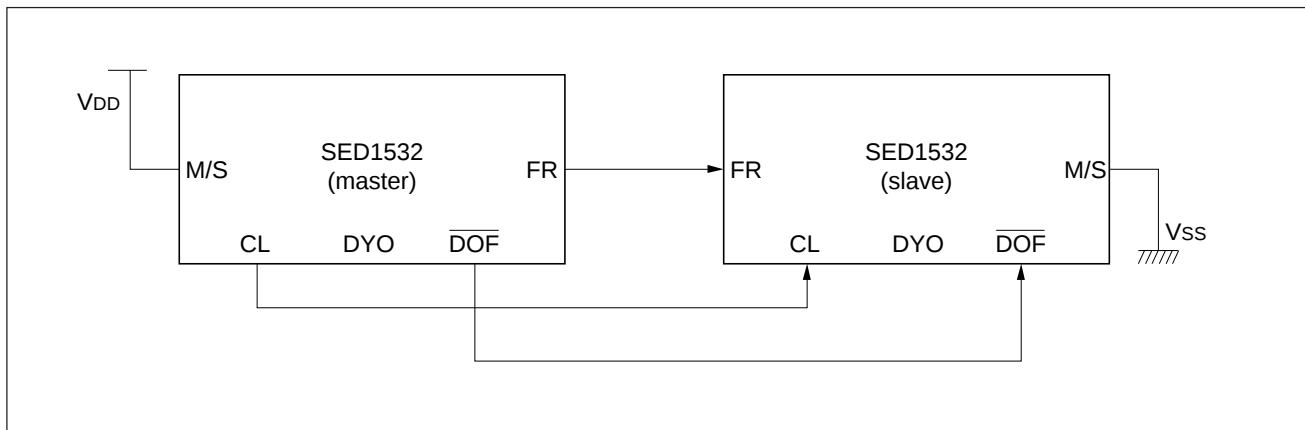
● SED1531 to SED1670



● SED1530 to SED1531

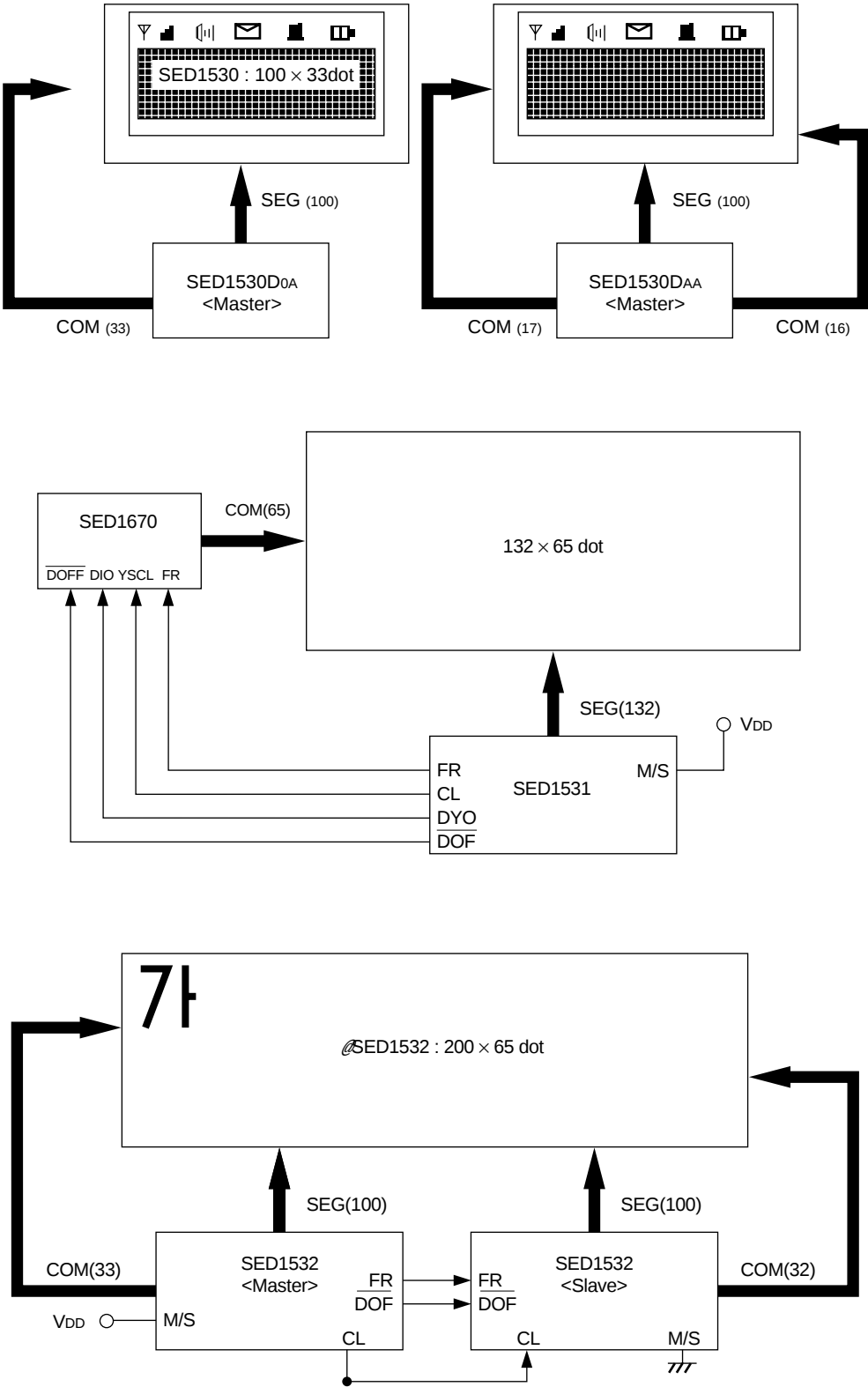


● SED1532 to SED1532



SED1530 Series

■ LCD PANEL CONNECTION EXAMPLES



SED1530 Series

NOTICE:

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