Multi-Phase PWM Controller for CPU Core Power Supply

General Description

RT9245 is a multi-phase buck DC/DC controller integrated with all control functions for Intel® GHz CPU which is VRD10.X-compliant. The RT9245 could be operated with 2, 3 or 4 buck switching stages operating in interleaved phase set automatically. The multiphase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9245 implements both voltage and current loops to achieve good regulation, response and power stage thermal balance.

RT9245 applies the DCR sensing technology newly. The RT9245 extracts the ESR of output inductor as sense component to deliver a precise load line regulation and good thermal balance for next generation processor application.

Current sense setting, droop tuning, V_{CORE} initial offset and over current protection are independent on compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning. The DAC output of RT9245 supports VRD10.x with 6-bit V_{ID} input, precise offset value & smooth V_{CORE} transient at V_{ID} jump. The IC monitors the V_{CORE} voltage for PGOOD and over-voltage protection. Soft-start, over-current protection and programmable under-voltage lockout are also provided to assure the safety of microprocessor and power system. The RT9245 comes to a small footprint package TSSOP-28.

Ordering Information

RT9245 □ □

- Package Type
  C : TSSOP-28
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Features

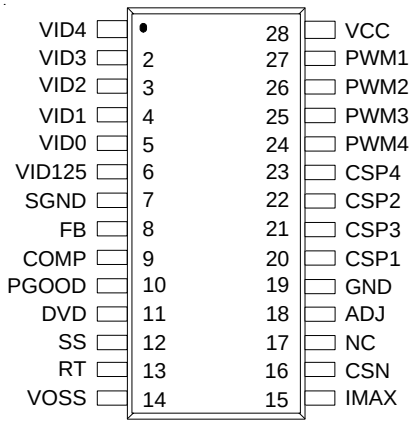
- **Multi-Phase Power Conversion with Automatic Phase Selection**
- **6-bits VRD10.x DAC Output with Active Droop Compensation for Fast Load Transient**
- **Smooth V_{CORE} Transition at VID Jump**
- **Power Stage Thermal Balance by DCR Current Sense**
- **Hiccup Mode Over-Current Protection**
- **Programmable Switching Frequency (50kHz to 400kHz per Phase), Under-Voltage Lockout and Soft-Start**
- **High Ripple Frequency Times Channel Number**
- **28-TSSOP Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Intel® Processors Voltage Regulator : VRD10.x
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

Pin Configurations

(TOP VIEW)



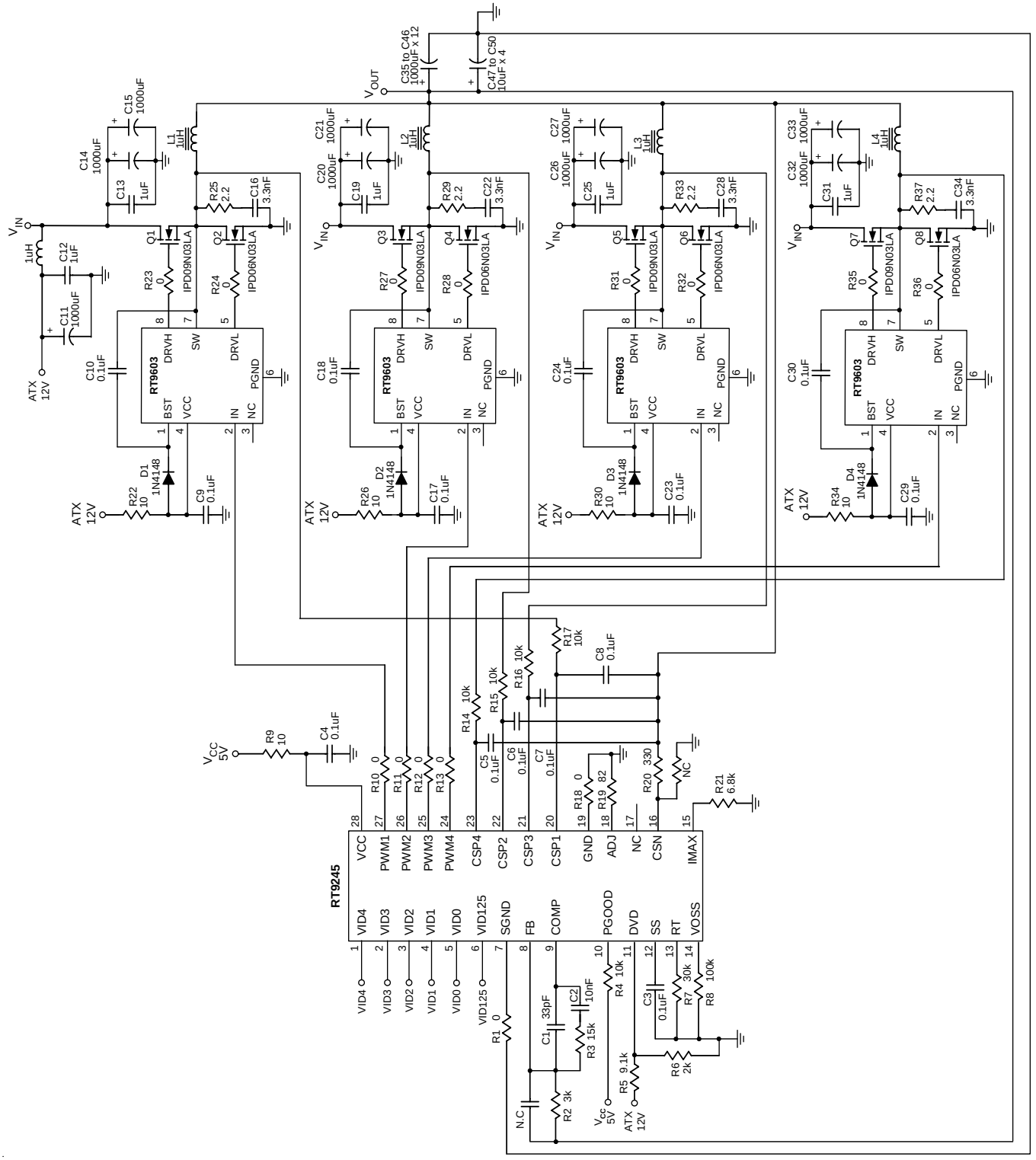
TSSOP-28

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Typical Application Circuit



Functional Pin Description

VID4 (Pin 1), VID3 (Pin 2), VID2 (Pin 3), VID1 (Pin 4), VID0 (Pin 5) & VID125 (Pin 6)

DAC voltage identification inputs for VRD10.x. These pins are internally pulled to 1.2V if left open.

SGND (Pin 7)

V_{CORE} differential sense negative input.

FB (Pin 8)

Inverting input of the internal error amplifier.

COMP (Pin 9)

Output of the error amplifier and input of the PWM comparator.

PGOOD (Pin 10)

Power good open-drain output.

DVD (Pin 11)

Programmable power UVLO detection input. Trip threshold = 1.2V at V_{DVD} rising.

SS (Pin 12)

Connect this SS pin to GND with a capacitor to set the soft-start time interval. Pulling this pin below 1V (ramp valley of sawtooth wave in pulse width modulator) would make all PWMs low, turn on low side MOSFETs, and turn off high side MOSFETs.

RT (Pin 13)

Switching frequency setting. Connect this pin to GND with a resistor to set the frequency.

VOSS (Pin 14)

V_{CORE} initial value offset. Connect this pin to GND with a resistor to set the negative offset value. Connect this pin to VCC to set positive offset value.

IMAX (Pin 15)

Programmable over currert setting.

CSN (Pin 16)

Current sense negative input of all channels.

NC (Pin 17)

No Connection.

ADJ (Pin 18)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the load droop.

GND (Pin 19)

Ground for the IC.

CSP1 (Pin 20), CSP2 (Pin 22), CSP3 (Pin 21) & CSP4 (Pin 23)

Current sense positive inputs for individual converter channel current sense.

PWM1 (Pin 27), PWM2 (Pin 26), PWM3 (Pin 25) & PWM4 (Pin 24)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver. For systems which use 3 channels, connect PWM4 high. Two channel systems connect PWM3 high.

VCC (Pin 28)

IC power supply. Connect this pin to a 5V supply.

Function Block Diagram

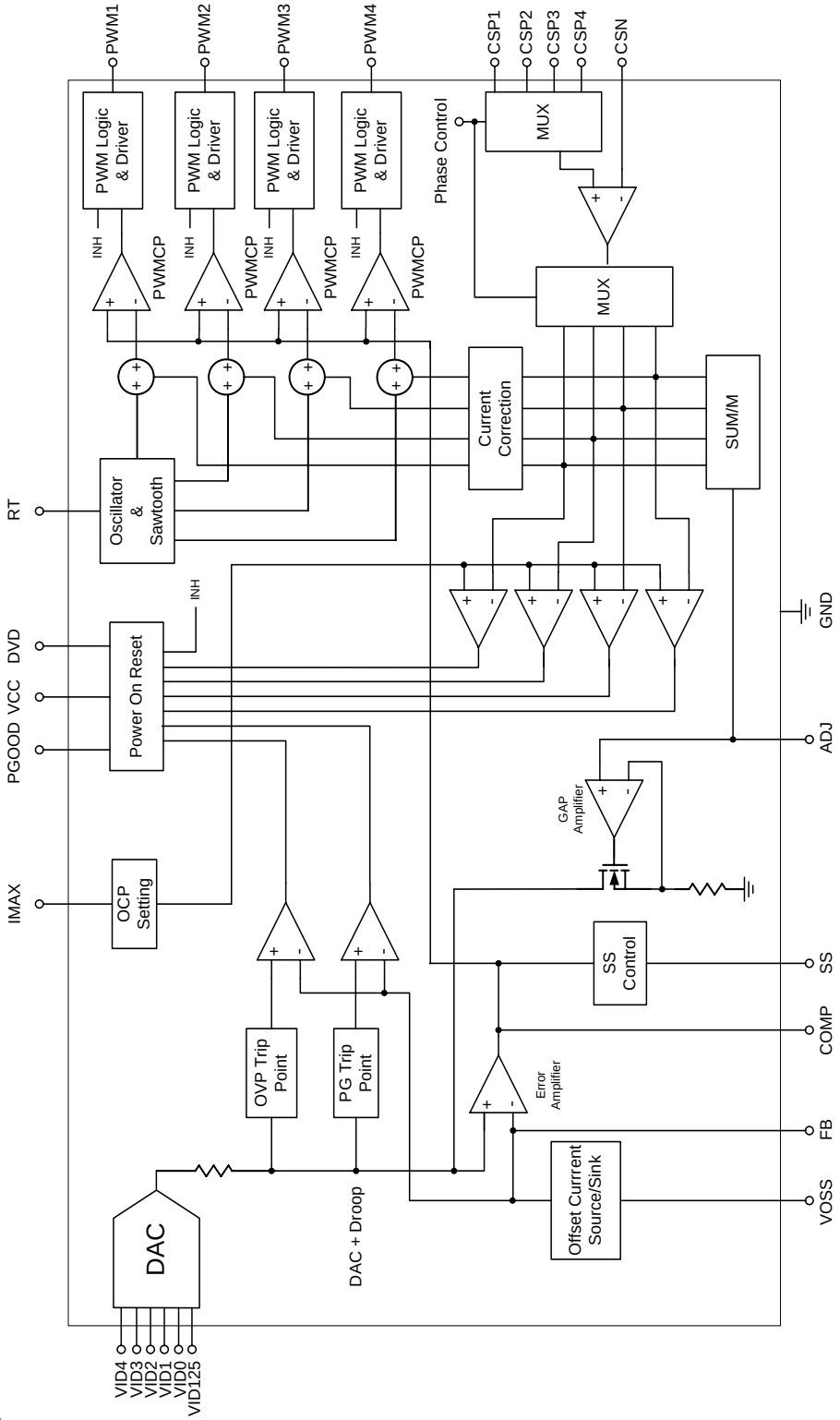


Table 1. Output Voltage Program

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	1	1	1	X	No CPU
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.850V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.875V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.900V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.925V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.950V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.025V
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.050V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.075V
0	0	0	0	0	0	1.0875V
1	1	1	1	0	1	1.100V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.125V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.150V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.175V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.200V
1	1	0	1	0	0	1.2125V

To be continued

Table 1. Output Voltage Program

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	0	0	1	1	1.225V
1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.250V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.275V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.300V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.325V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.350V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.375V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.400V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.425V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.450V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.475V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.500V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.525V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.550V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.575V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Note: (1) 0 : Connected to GND
(2) 1 : Open
(3) X : Don't Care

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 7V
- Input, Output or I/O Voltage ---------- GND – 0.3V to V_{CC} + 0.3V
- Package Thermal Resistance
  TSSOP-28, θ_{JA} ---------- 100°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 5V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current							
Nominal Supply Current		I_{CC}	PWM 1,2,3,4 Open	--	12	16	mA
Power-On Reset							
POR Threshold		V_{CCRTH}	V_{CC} Rising	4.0	4.2	4.5	V
Hysteresis		V_{CCHYS}		0.2	0.5	--	V
V_{DVD} Threshold	Trip (Low to High)	V_{DVDTP}	Enable	1.1	1.2	1.3	V
	Hysteresis	V_{DVDHYS}		--	50	--	mV
Oscillator							
Free Running Frequency		f_{OSC}	R_{RT} = 32kΩ	170	200	230	kHz
Frequency Adjustable Range		f_{OSC_ADJ}		50	--	400	kHz
Ramp Amplitude		ΔV_{OSC}	R_{RT} = 32kΩ	--	1.9	--	V
Ramp Valley		V_{RV}		0.7	1.0	--	V
Maximum On-Time of Each Channel				62	66	75	%
RT Pin Voltage		V_{RT}	R_{RT} = 32kΩ	1.4	1.60	1.8	V
Reference and DAC							
DACOUT Voltage Accuracy		ΔV_{DAC}	$V_{DAC} \geq 1V$	–1	--	+1	%
			$V_{DAC} < 1V$	–10	--	+10	mV
DAC (VID0-VID125) Input Low		V_{ILDAC}		--	--	0.4	V
DAC (VID0-VID125) Input High		V_{IHDAC}		0.8	--	--	V
DAC (VID0-VID125) Bias Current		I_{BIAS_DAC}		25	50	75	μA
VOSS Pin Voltage		V_{VOSS}	R_{VOSS} = 100kΩ	1.5	1.65	1.8	V

To be continued

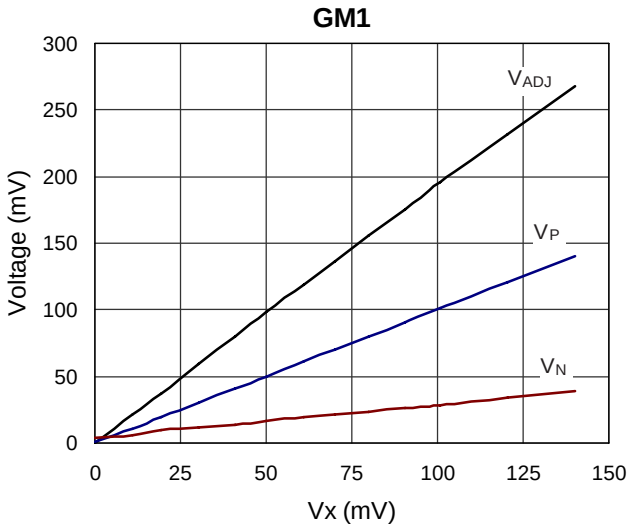
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Error Amplifier						
DC Gain			--	85	--	dB
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR	COMP = 10pF	--	3	--	V/μs
Current Sense GM Amplifier						
CSN Full Scale Source Current	I_{ISPFSS}		100	--	--	μA
CSN Current for OCP			150	--	--	μA
Protection						
SS Current	I_{SS}	V_{SS} = 1V	8	13	18	μA
Over-Voltage Trip (VSEN/DACOUT)	Δ_{OVT}		130	140	150	%
IMAX Voltage	V_{IMAX}	R_{IMAX} = 32k	1.4	1.60	1.8	V
Power Good						
Output Low Voltage	V_{PGOODL}	I_{PG} = 4mA	--	--	0.2	V

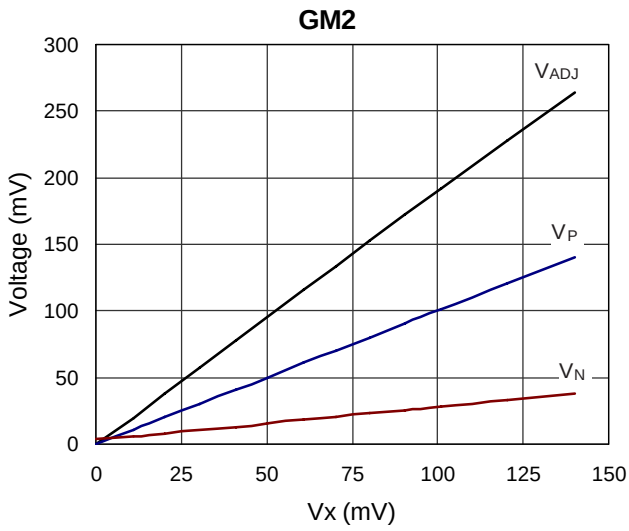
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

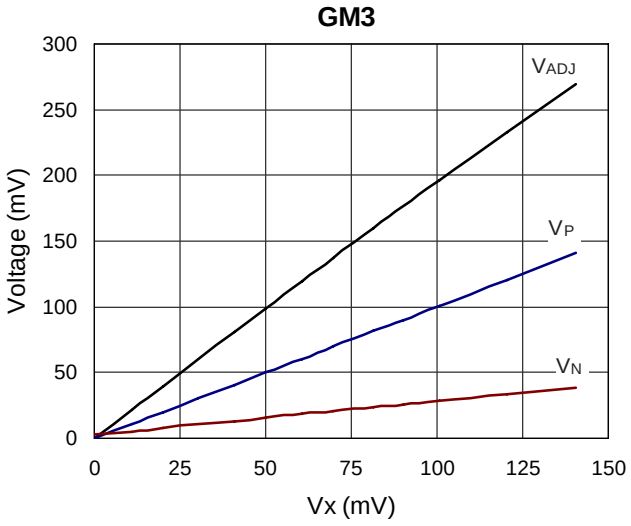
Note 2. Devices are ESD sensitive. Handling precaution recommended.

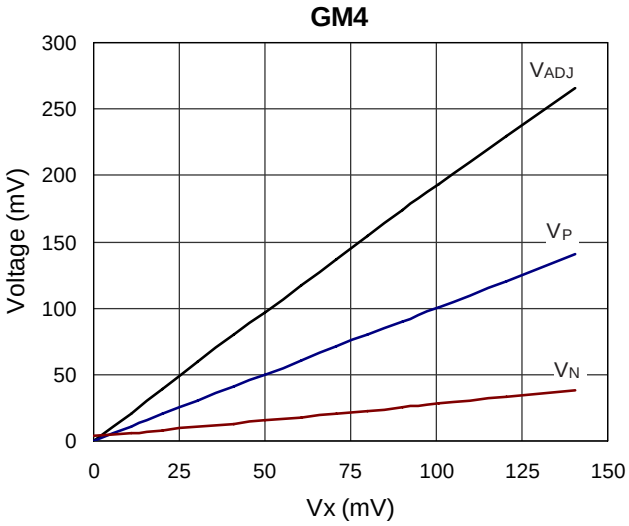
Note 3. The device is not guaranteed to function outside its operating conditions.

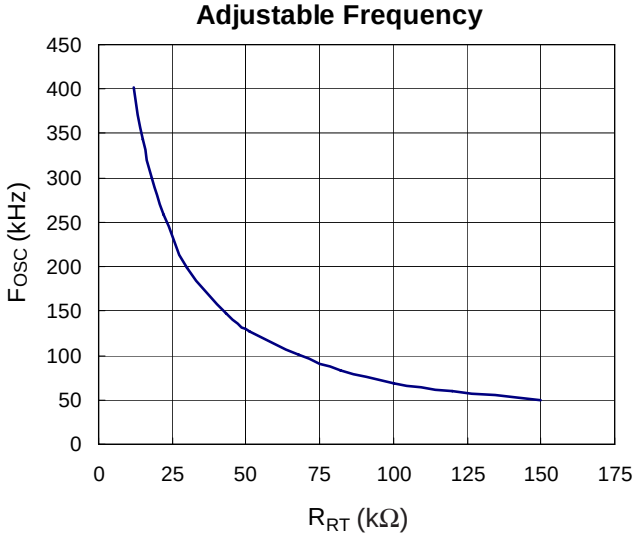
Typical Operating Characteristics

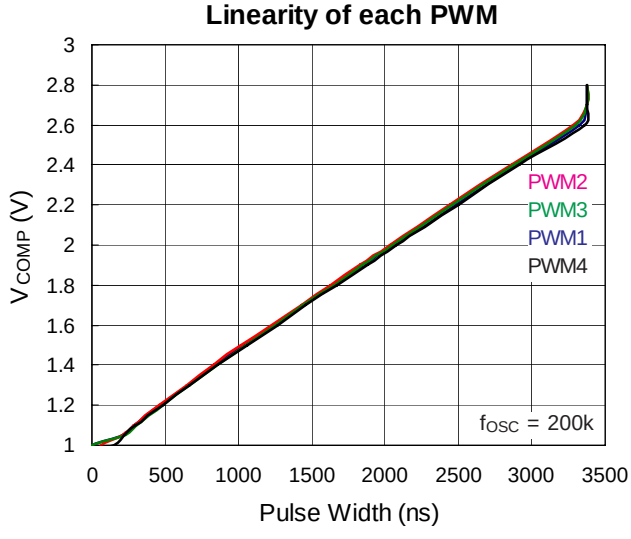




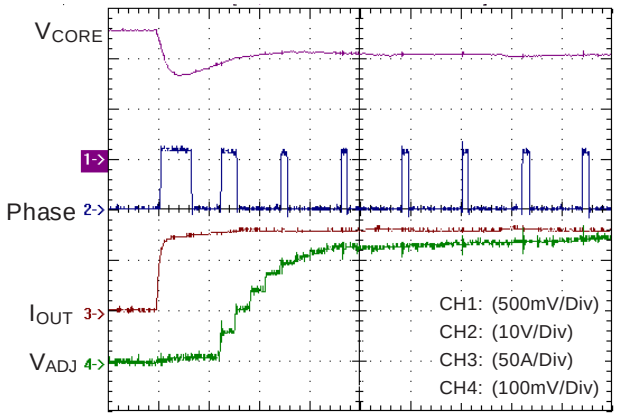






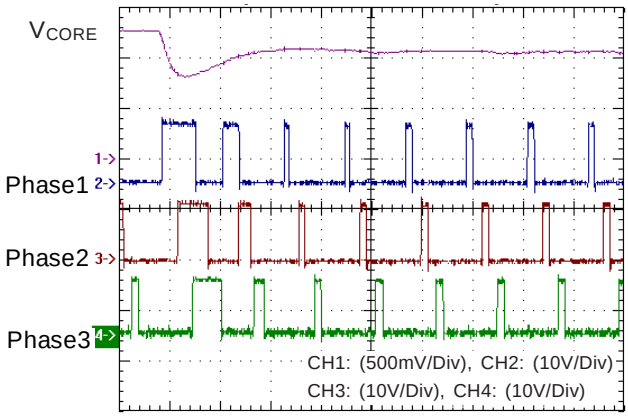


Load Transient Response



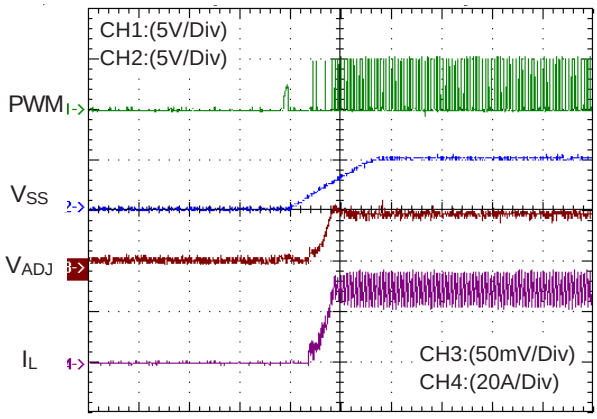
Time (5µs/Div)

Load Transient Response



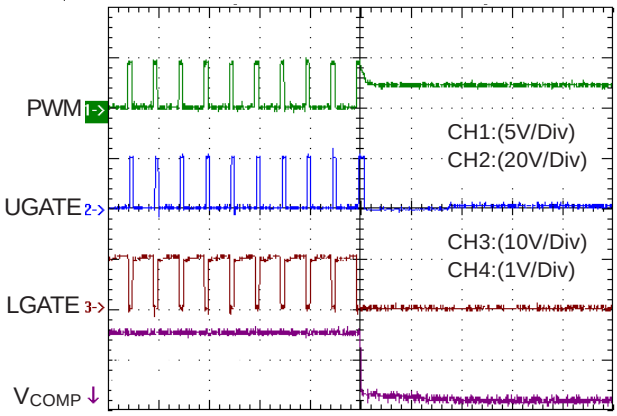
Time (5µs/Div)

Relationship Between Inductor Current and V_{ADJ}



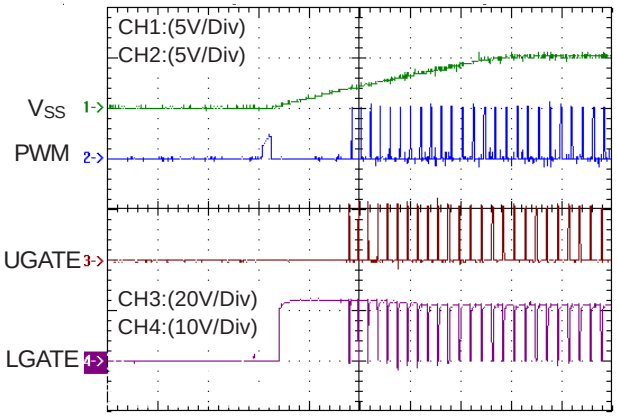
Time (25ms/Div)

Power-Off @ I_{OUT} = 60A



Time (10µs/Div)

Power-On @ I_{OUT} = 60A



Time (10ms/Div)

Application Information

RT9245 is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consisting of RT9245 and its companion MOSFET driver RT9603/ RT9603A provides high quality CPUpower and all protection functions to meet the requirement of modern VRM.

Voltage Control

RT9245 senses the CPU VCORE by SGND pin to sense the return of CPU to minimize the voltage drop on PCB trace at heavy load. OVP is sensed at FB pin. The internal high accuracy VID DAC provides the reference voltage for VRD10.X compliance. Control loop consists of error amplifier, multi-phase pulse width modulator, driver and power components. As conventional voltage mode PWM controller, the output voltage is locked at the VREF of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase sawtooth wave. Power stage transforms VIN to output by PWM signal on-time ratio.

Current Balance

RT9245 senses the inductor current via inductor's DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal balance circuit.

The current balance circuit sums and averages the current signals and then produces the balancing signals injected to pulse width modulator. If the current of some power channel is larger than average, the balancing signal reduces that channels pulse width to keep current balance. The use of single GM amplifier via time sharing technique to sense all inductor currents can reduce the offset errors and linearity variation between GMs. Thus it can greatly improve signal processing especially when dealing with such small signal as voltage drop across DCR.

Load Droop

The sensed power channel current signals regulate the reference of DAC to form an output voltage droop proportional to the load current. The droop or so call “active voltage positioning” can reduce the output voltage ripple at load transient and the LC filter size.

Fault Detection

The chip detects FB for over voltage and power good detection. The “hiccup mode” operation of over current protection is adopted to reduce the short circuit current. The in-rush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

Phase Setting and Converter Start Up

RT9245 interfaces with companion MOSFET drivers (like RT9603, RT9602 series) for correct converter initialization. The tri-state PWM output (high, low and high impedance) senses its interface voltage when IC POR acts (both VCC and DVD trip). The channel is enabled if the pin voltage is 1.2V less than VCC. Tie the PWM to VCC and the corresponding current sense pins to GND or left float if the channel is unused. For example, for 3-Channel application, connect PWM4 high.

Current Sensing Setting

RT9245 senses the current flowing through inductor via its DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal circuit (see Figure 1).

$$\frac{L}{DCR} = R \times C \quad V_C = DCR \times I_L \quad I_X = \frac{V_C}{R_{CSN}}$$

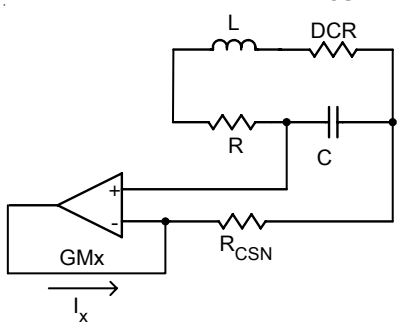


Figure 1. Current Sense Circuit

Figure 2 is the test circuit for GM. We apply test signal at GM inputs and observe its signal process output at ADJ pin. Figure 3 shows the variation of signal processing of all channels. We observe zero offsets and good linearity between phases.

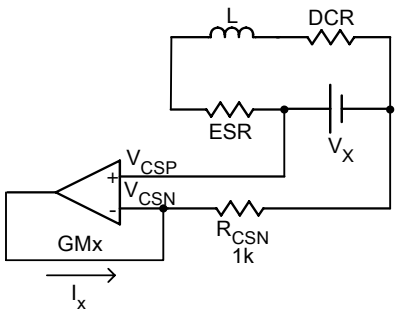


Figure 2. The Test Circuit of GM

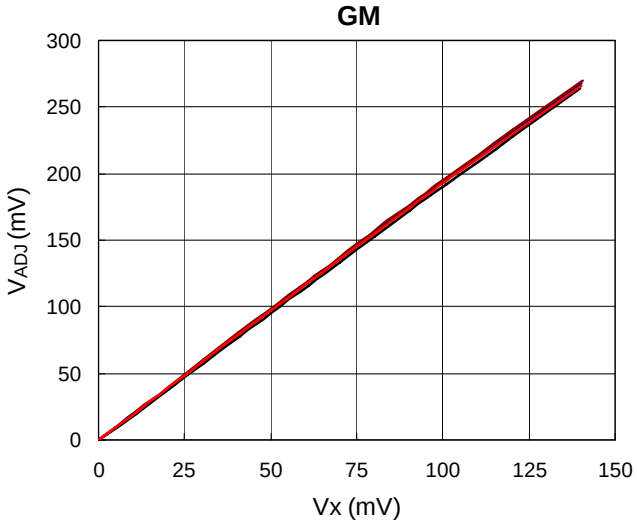


Figure 3. The Linearity of GMx

Figure 4 shows the time sharing technique of GM amplifier. We apply test signal at phase 4 and observe the waveforms at both pins of GM amplifier. The waveforms show time sharing mechanism and the perfomance of GM to hold both input pins equal when the shared time is on.

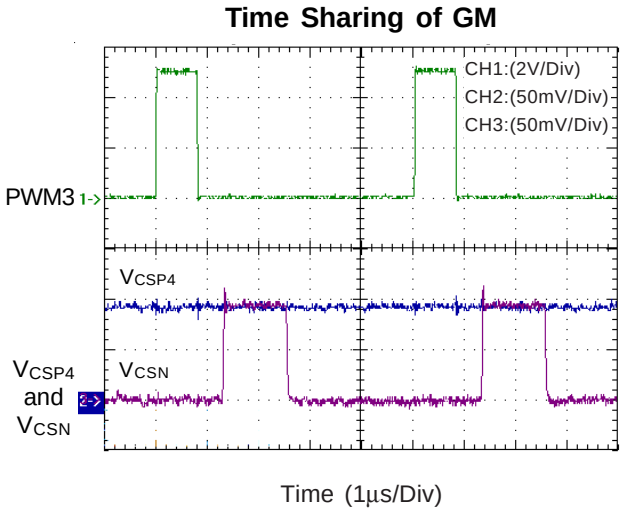


Figure 4

Over Current Protection

RT9245 uses an external resistor R_{IMAX} to set a programmable over current trip point. OCP comparator compares each inductor current with this reference current. RT9245 uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground.

$$\frac{1}{2}\times\frac{V_{IMAX}}{R_{IMAX}} \Leftrightarrow \frac{1}{3}\times\frac{I_L\times DCR}{R_{COMMON}}$$

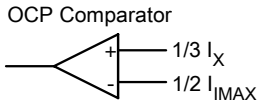


Figure 5. Over Current Comparator

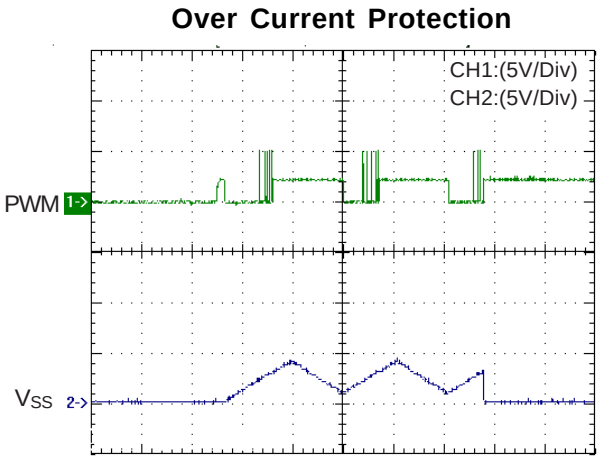


Figure 6. The Over Current Protection in the soft start interval

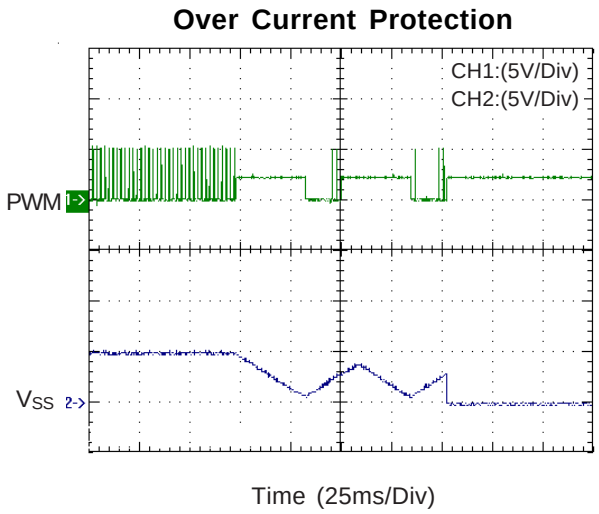


Figure 7. Over Current Protection at steady state

Current Ratio Setting

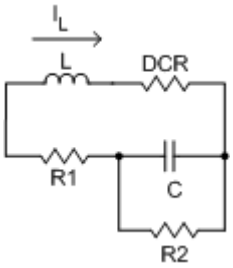


Figure 8. Application circuit for current ratio setting

For some case with preferable current ratio instead of current balance, the corresponding technique is provided. Due to different physical environment of each channel, it is necessary to slightly adjust current loading between channels. Figure 8 shows the application circuit of GM for current ratio requirement. Applying KVL along L+DCR branch and R1+C//R2 branch :

$$L\frac{dI_L}{dt}+DCR\times I_L = R_1(\frac{V_C}{R_2}+C\frac{dV_C}{dt})+V_C$$

$$= R_1C\frac{dV_C}{dt}+\frac{R_1+R_2}{R_2}V_C$$

$$\text{For}\quad V_C=\frac{R2}{R_1+R_2}DCR\times I_L$$

Look for its corresponding conditions :

$$L\frac{dI_L}{dt}+DCR\times I_L = (R1//R2)\times C\times DCR\times\frac{dI_L}{dt}+DCR\times I_L$$

$$\text{Let}\quad \frac{L}{DCR}=(R1//R2)\times C$$

$$\text{Thus if}\quad \frac{L}{DCR}=(R1//R2)\times C$$

$$\text{Then}\quad V_C=\frac{R2}{R1+R2}\times DCR\times I_L$$

With internal current balance function, this phase would share $(R_1+R_2)/R_2$ times current than other phases. Figure 9 &10 show different settings for the power stages. Figure 11 shows the performance of current ratio compared with conventional current balance function in Figure 12.

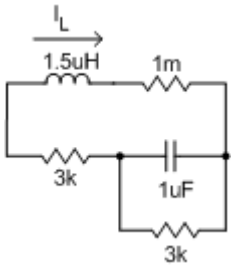


Figure 9. GM4 Setting for current ratio function

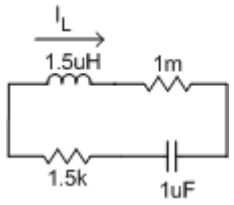


Figure 10. GM1~3 Setting for current ratio function

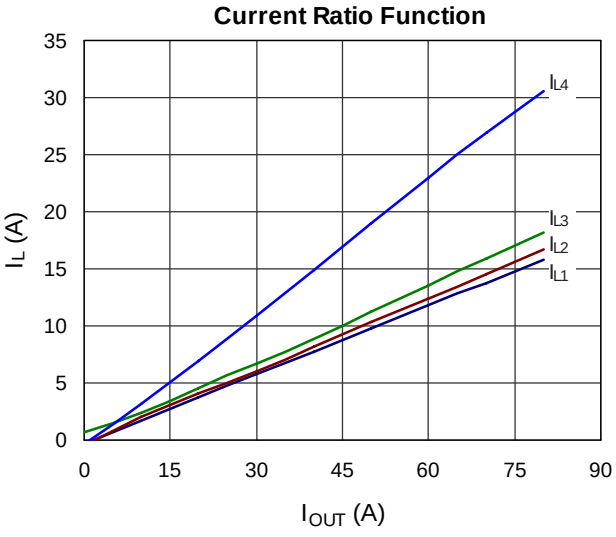


Figure 11

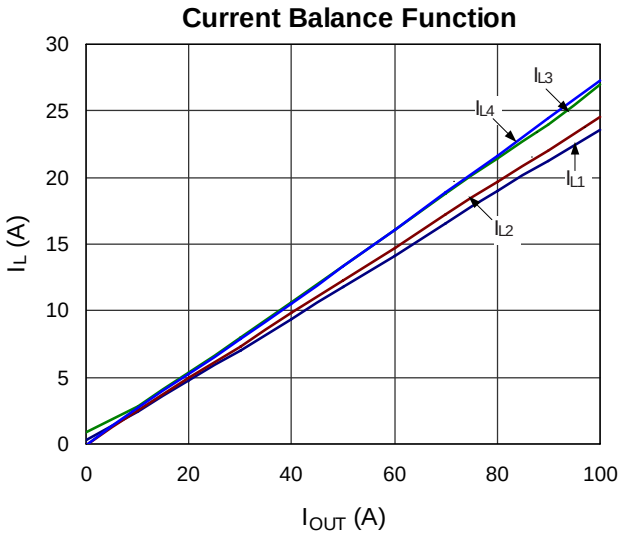


Figure 12

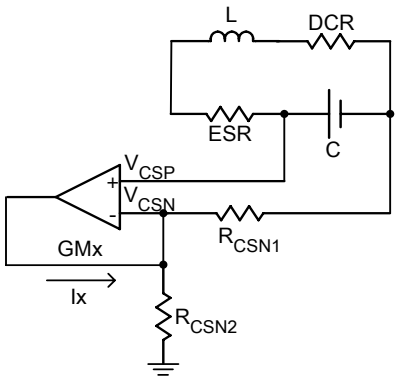


Figure13. Application circuit of GM

For load line design, with application circuit in Figure 13, it can eliminate the dead zone of load line at light loads.

$V_{CSP} = V_{OUT} + I_L \times DCR$

if GM holds input voltages equal, then

$$V_{CSP} = V_{CSN}$$

$$I_X = \frac{V_{CSN}}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN1}}$$

$$= \frac{V_{OUT} + I_L \times DCR}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN1}}$$

$$= \frac{V_{OUT}}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN1}}$$

For the lack of sinking capability of GM, R_{CSN2} should be small enough to compensate the negative inductor valley current especially at light loads.

$$\frac{V_{CSN}}{R_{CSN2}} \geq \left| \frac{I_L \times DCR}{R_{CSN1}} \right|$$

Assume the negative inductor valley current is –5A at no load, then for

$R_{CSN1} = 330\Omega$, $R_{ADJ} = 160\Omega$, $V_{OUT} = 1.300$

$$\frac{1.3V}{R_{CSN2}} \geq \left| \frac{-5A \times 1m\Omega}{330\Omega} \right|$$

$R_{CSN2} \leq 85.8k\Omega$

Choose $R_{CSN2} = 82k\Omega$

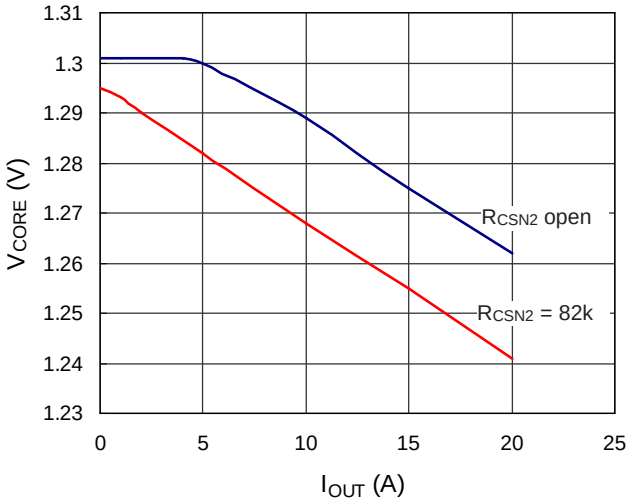


Figure 14

VID on the Fly

With external pull up resistors tied to VID pins, RT9245 converters different VID codes from CPU into output voltage. Figure 12 and Figure 13 show the waveforms of VID on the fly function.

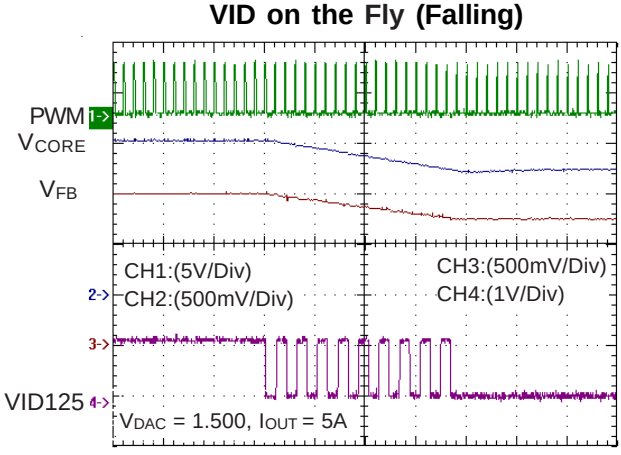


Figure 15

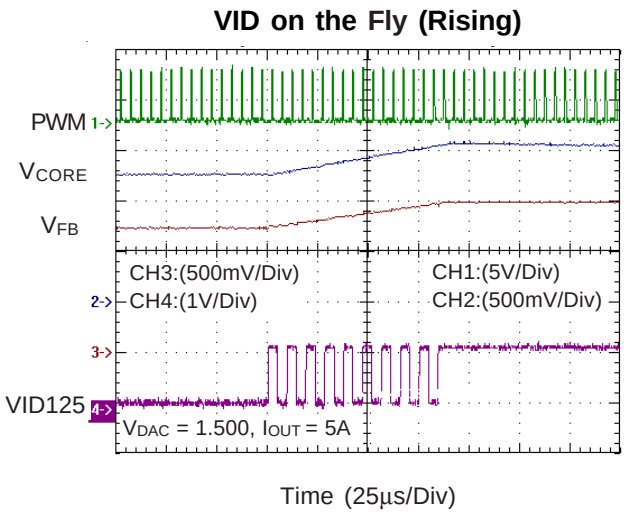


Figure 16

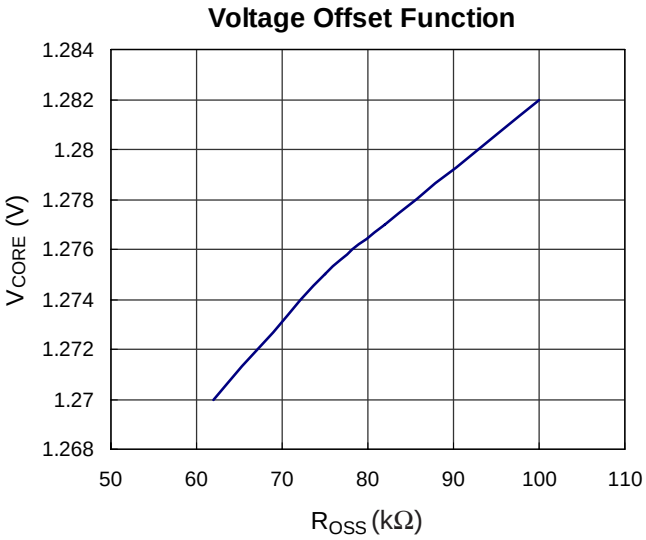


Figure 18

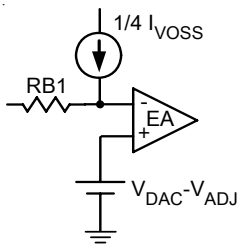


Figure 17

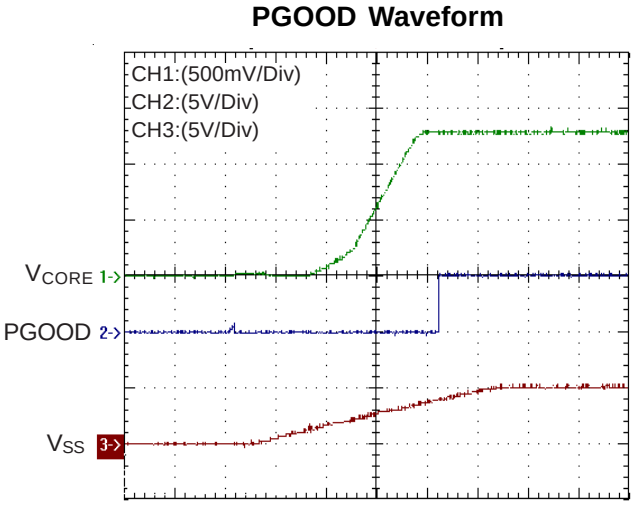


Figure 19

Output Voltage Offset Function

To meet Intel's requirement of initial offset of load line, RT9245 provides programmable initial offset function. With an external resistor R_{VOSS} and voltage source at V_{OSS} pin to set offset current I_{VOSS}. One quart of I_{VOSS} flows through RB1. Error amplifier would hold the inverting pin equal to V_{DAC}-V_{ADJ}. Thus output voltage is subtracted from $V_{DAL} – V_{ADJ}$ for a constant offset voltage.

PGOOD Function

To indicate the condition of multiphase converter, RT9245 provides PGOOD signal through an open drain connection. The waveforms of PGOOD function are shown in Figure 15.

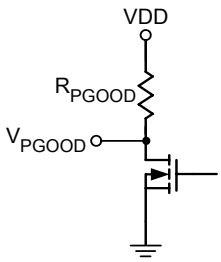


Figure 20. PGOOD Test Circuit

Error Amplifier Characteristic

For fast response of converter to meet stringent output current transient response, RT9245 provides large slew rate capability and high gain-bandwidth performance.

EA Falling Slew Rate

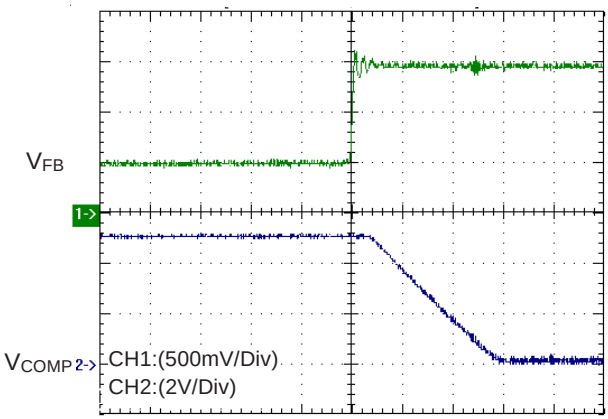


Figure 21. EA Rising Transient with 10pF Loading; Slew Rate=10V/us

EA Rising Slew Rate

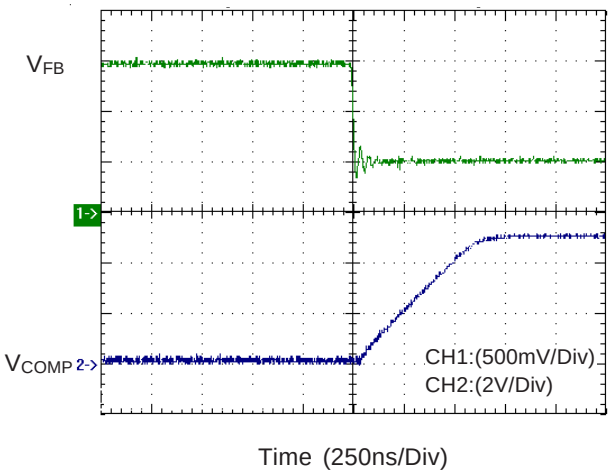


Figure 22. EA Falling Transient with 10pF Loading; Slew Rate=8V/us

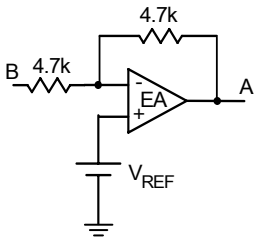


Figure 23. Gain-Bandwidth Measurement by signal A divided by signal B

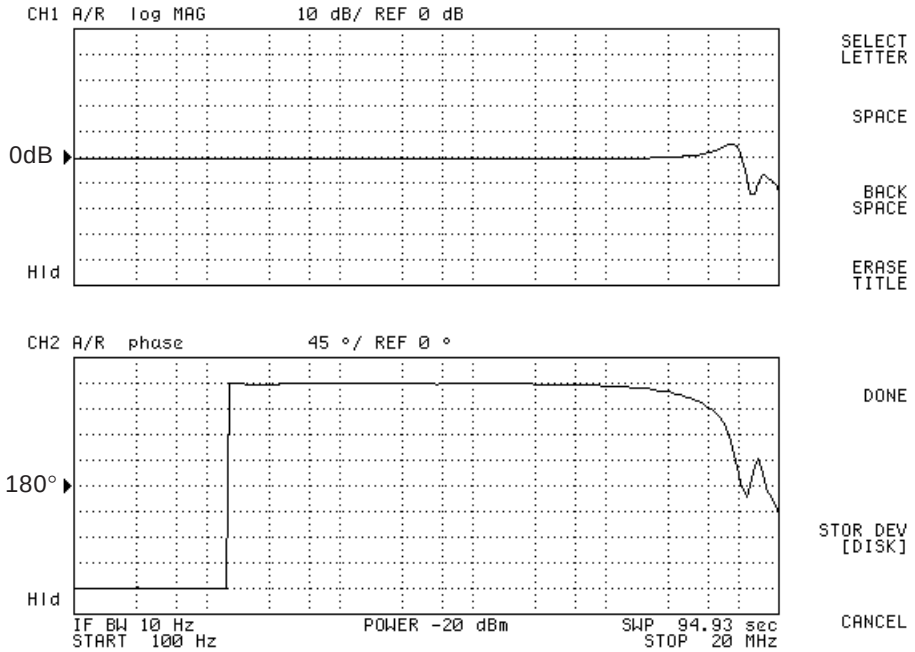


Figure 24. EA Frequency Response with closed loop gain set at 0db to observe gain-bandwidth product; -3dB at 10.86MHz

Design Procedure Suggestion

a. Output filter pole and zero (Inductor, output capacitor value & ESR).

b. Error amplifier compensation & sawtooth wave amplitude (compensation network).

c. Kelvin sense for VCORE.

Current Loop Setting

a. GM amplifier S/H current (current sense component DCR, CSN pin external resistor value).

b. Over-current protection trip point (R_{IMAX} resistor).

VRM Load Line Setting

a. Droop amplitude (ADJ pin resistor).

b. No load offset (R_{CSN2})

c. DAC offset voltage setting (VOSS pin & compen- sation network resistor RB1).

Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

a. Kelvin sense for current sense GM amplifier input.

b. Refer to layout guide for other items.

Voltage Loop Setting

Design Example

Given:

Apply for four phase converter

V_{IN} = 12V

V_{CORE} = 1.5V

$I_{LOAD\ (MAX)}$ = 100A

V_{DROOP} = 100mV at full load (1mΩ Load Line)

OCP trip point set at 40A for each channel (S/H)

DCR = 1mΩ of inductor at 25°C

L = 1.5µH

C_{OUT} = 8000µF with 5mΩ equivalent ESR.

1. Compensation Setting

a. Modulator Gain, Pole and Zero:

From the following formula:

Modulator Gain = V_{IN}/V_{RAMP} = 12/2.4=5 (i.e 14dB)

where V_{RAMP} : ramp amplitude of saw-tooth wave

LC Filter Pole = = 1.45kHz and

ESR Zero =3.98kHz

b. EA Compensation Network:

Select R1 = 4.7k, R2 = 15k, C1 = 12nF, C2 = 68pF and use the Type 2 compensation scheme shown in Figure 25. By calculation, the FZ = 0.88kHz, FP = 322kHz and Middle Band Gain is 3.19 (i.e 10.07dB).

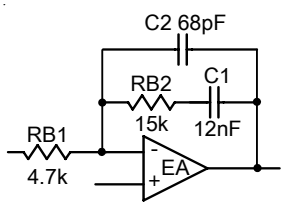


Figure 25. Type 2 compensation network of EA

The bode plot of EA compensation is shown as Figure 26.

The bode plot of power stage is shown as Figure 27. The total loop gain is in Figure 28.

3. Over-Current Protection Setting

Consider the temperature coefficient of copper 3900ppm/°C,

$$\frac{1}{2}\times\frac{V_{IMAX}}{R_{IMAX}} \Leftrightarrow \frac{1}{3}\times\frac{I_L\times DCR}{R_{COMMON}}$$

$$\frac{1}{2}\times\frac{1.690V}{R_{IMAX}} \Leftrightarrow \frac{1}{3}\times\frac{40A\times 1.39m\Omega}{330\Omega}$$

Let R_{IMAX} = 14kΩ

4. Soft-Start Capacitor Selection

For most application cases, 0.1µF is a good engineering value.

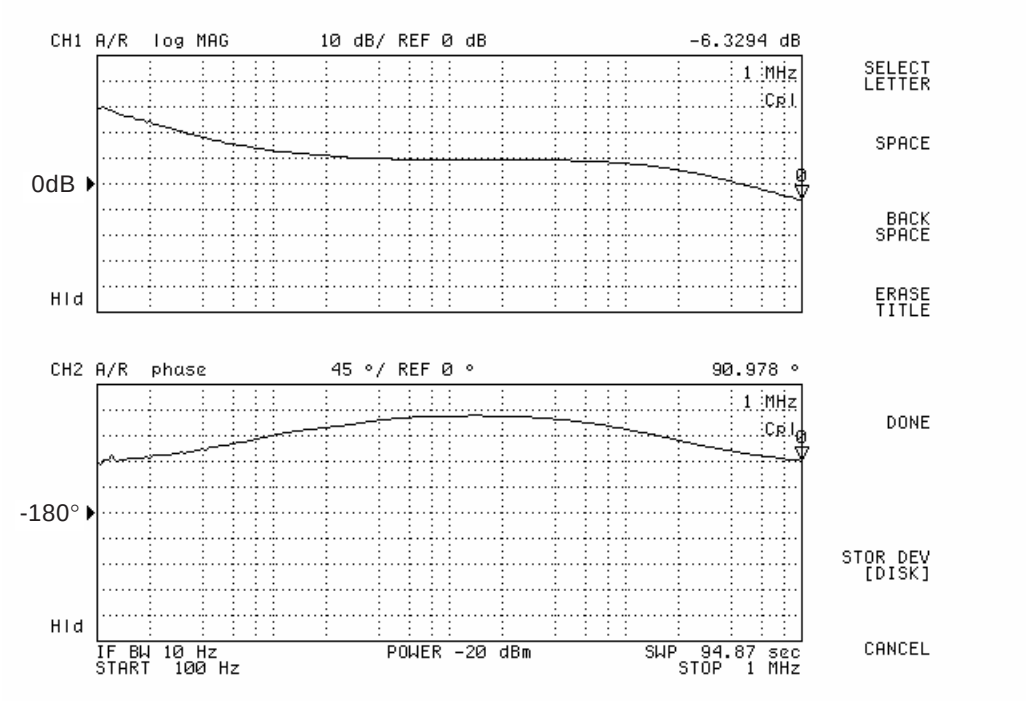


Figure 26. The Frequency Response of the Compensator Network

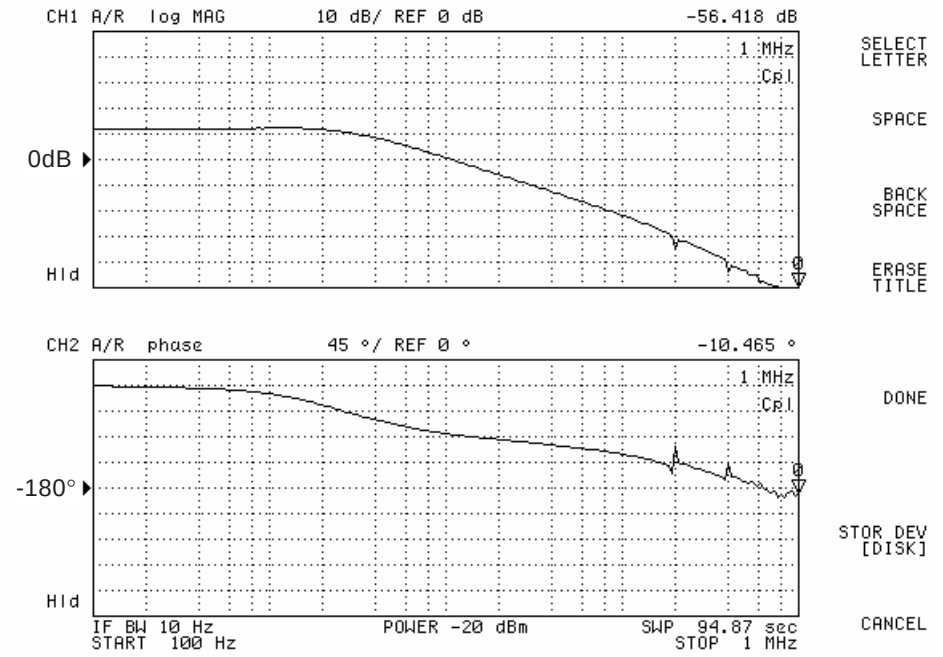


Figure 27. The Frequency Response of Power Stage

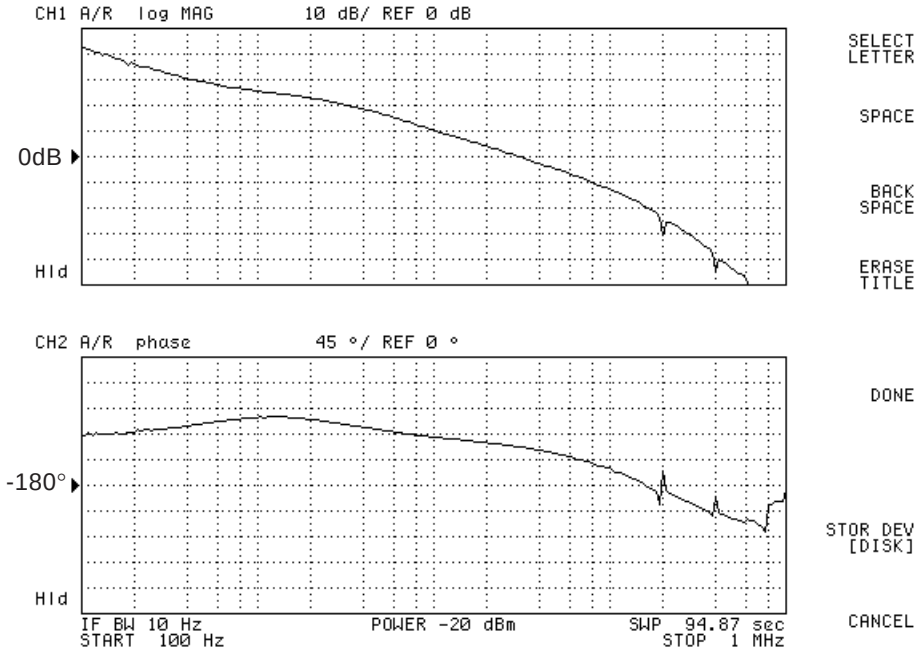


Figure 28. The Loop Gain of Converter

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. **Most critical path: the current sense circuit is the most sensitive part of the converter. The current sense resistors tied to CSP1,2,3,4 and CSN should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. Kelvin connection of the sense component (additional sense resistor or Inductor DCR) ensures the accurate stable current sensing.**

   Keep well Kelvin sense to ensure the stable operation!

2. Switching ripple current path:
   a. Input capacitor to high side MOSFET.
   b. Low side MOSFET to output capacitor.
   c. The return path of input and output capacitor.
   d. Separate the power and signal GND.
   e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.
   f. Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.

3. MOSFET driver should be closed to MOSFET.

4. The compensation, bypass and other function setting components should be near the IC and away from the noisy power path.

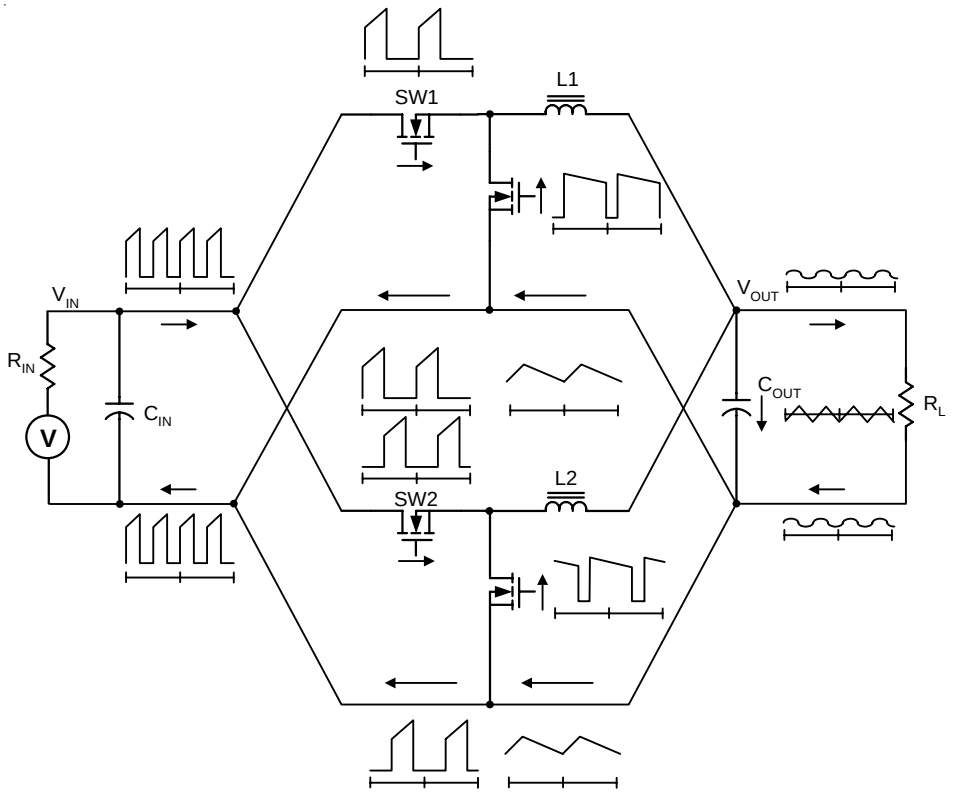


Figure 29. Power Stage Ripple Current Path

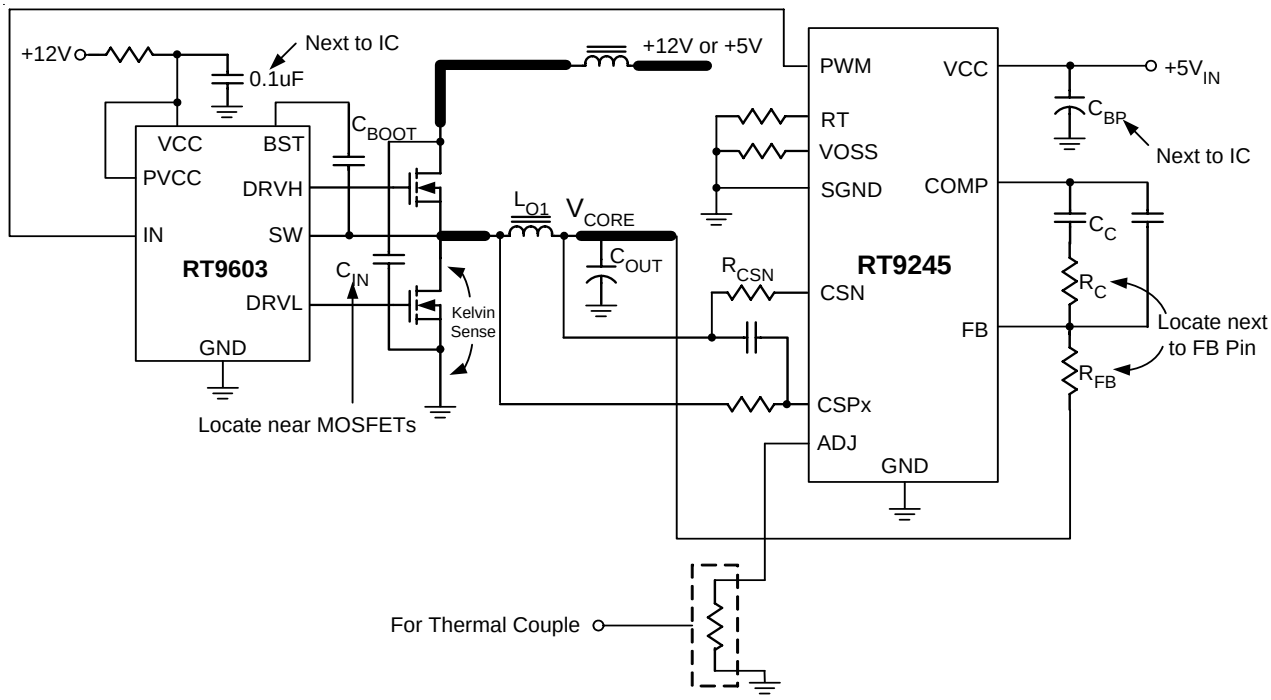


Figure 30. Layout Consideration

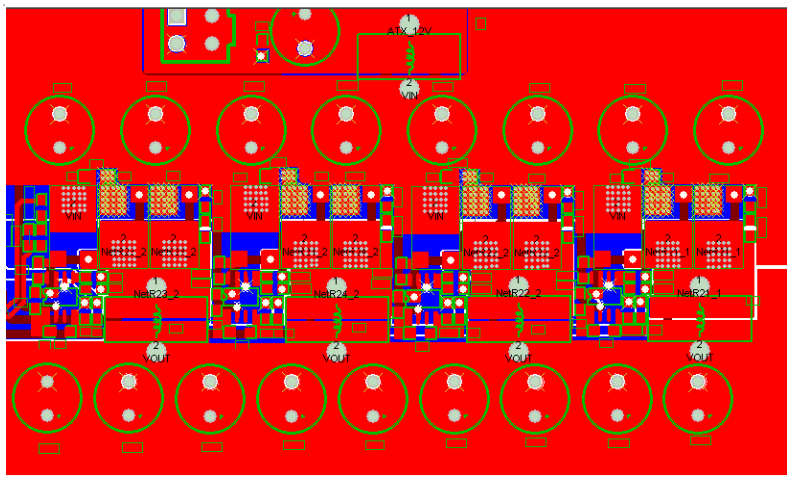


Figure 31. Layout of power stage

Test Conditions :

V_{IN} : 12V

V_{OUT} : 1.300V

F_{SW} : 200kHz

I_{OUT} : 80A

Phase Number : 4 Phases

U-MOSFET : IR3707 x 1 (9.5mΩ x 9.6nC)

L-MOSFET : IR8113 x 2 (6.0mΩ x 22nC)

L : 1.5uH

DCR : 1m

C_{IN} : 1000uF x 8

C_{OUT} : 1000uF x 8

Snubber : 2R2+3.3nF

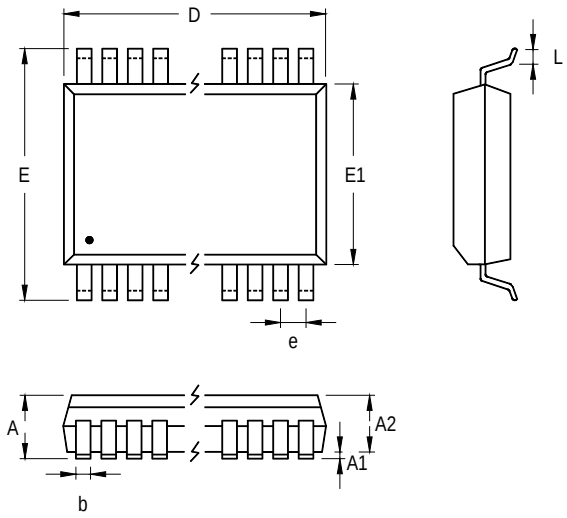
Air Speed : Using MAGIC MGA8012HS FAN with 5VDC drive.

P1	P1	P1	P1	P2	P2	P2	P2
Driver	M1	M2	M3	Driver	M4	M5	M6
55°C	58°C	58°C	56°C	56°C	60°C	60°C	60°C

P3	P3	P3	P3	P4	P4	P4	P4
Driver	M7	M8	M9	Driver	M10	M11	M12
55°C	64°C	64°C	65°C	59°C	69°C	66°C	61°C

Note: V_{IN}= 10.835V; I_{IN} = 10.6A; V_{OUT} = 1.2127V; I_{OUT} = 80A; η =84.47%

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.850	1.200	0.033	0.047
A1	0.050	0.152	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.178	0.305	0.007	0.012
D	9.601	9.804	0.378	0.386
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.293	4.496	0.169	0.177
L	0.450	0.762	0.018	0.030

28-Lead TSSOP Plastic Package

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