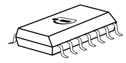
Low-Drop Fixed Voltage Regulator **TLE 4299**

Data Sheet

Features

- Output voltage 3.3V ± 2%
- 150 mA Output current
- Extreme low current consumption in ON state
- Inhibit function: Below 1 µA current consumption in off mode
- Early warning
- Reset output low down to V_Q = 1 V
- Overtemperature protection
- Reverse polarity proof
- Wide temperature range

P-DSO-8-3



P-DSO-14-3, -8, -9, -11

Type	Ordering Code	Package
TLE 4299 GV33	Q67065-A7033	P-DSO-8-3
TLE 4299 GMV33	Q67065-A7032	P-DSO-14-8

Functional Description

The TLE 4299 is a monolithic voltage regulator with fixed 5-V (see data sheet TLE4299G/GM) or 3.3 V output, supplying loads up to 150 mA. It is especially designed for applications that may not be powered down while the motor is off. In addition the TLE 4299GMV includes an inhibit function. When the inhibit signal is removed, the device is switched off and the quiescent current is less than 1 µA. To achieve proper operation of the µ-controller, the device supplies a reset signal. The reset delay time is selected application-specific by an external delay capacitor. The reset threshold is adjustable. An early warning signal supervises the voltage at pin SI. The TLE 4299 is pin-compatible to the TLE 4269 and functional similar with the additional inhibit function. The TLE 4299 is designed to supply microcontroller systems even under automotive environment conditions. Therefore it is protected against overload, short circuit and over temperature.

Circuit Description

The TLE 4299 is a PNP based very low drop linear voltage regulator. It regulates the output voltage to V_Q = 3.3 V for an input voltage range of 4.4 V ≤ V_I ≤ 45 V. The control circuit protects the device against potential damages caused by overcurrent and overtemperature.

The internal control circuit achieves a 3.3 V output voltage with a tolerance of ± 2%.

The device includes a power on reset and an under voltage reset function with adjustable reset delay time and adjustable reset switching threshold as well as a sense control/early warning function. The device includes an inhibit function to disable it when the ECU is not used for example while the motor is off.

The reset logic compares the output voltage V_Q to an internal threshold. If the output voltage drops below this level, the external reset delay capacitor C_D is discharged. When V_D is lower than V_{ST}, the reset output RO is switched Low. If the output voltage drop is very short, the V_{ST} level is not reached and no reset-signal is asserted. This feature avoids resets at short negative spikes at the output voltage e.g. caused by load changes.

As soon as the output voltage is more positive than the reset threshold, the delay capacitor is charged with constant current. When the voltage reaches V_{DT} the reset output RO is set High again.

The reset delay time and the reset reaction time are defined by the external capacitor C_D. The reset function is active down to V_I = 1 V.

In addition to the normal reset function, the device gives an early warning. When the SI voltage drops below $V_{SI,low}$, the devices asserts the SI output Low to indicate the logic and the µ-processor that this voltage has dropped. The sense function uses a hysteresis: When the SI-voltage reaches the $V_{SI,high}$ level, SO is set high again. This feature can be used as early warning function to notice the µ-controller about a battery voltage drop and a possible reset in a short time. Of course also any other voltage can be observed by this feature.

The user defines the threshold by the resistor-values R_{SI1} and R_{SI2}.

For the exact timing and calculation of the reset and sense timing and thresholds, please refer to the application section.

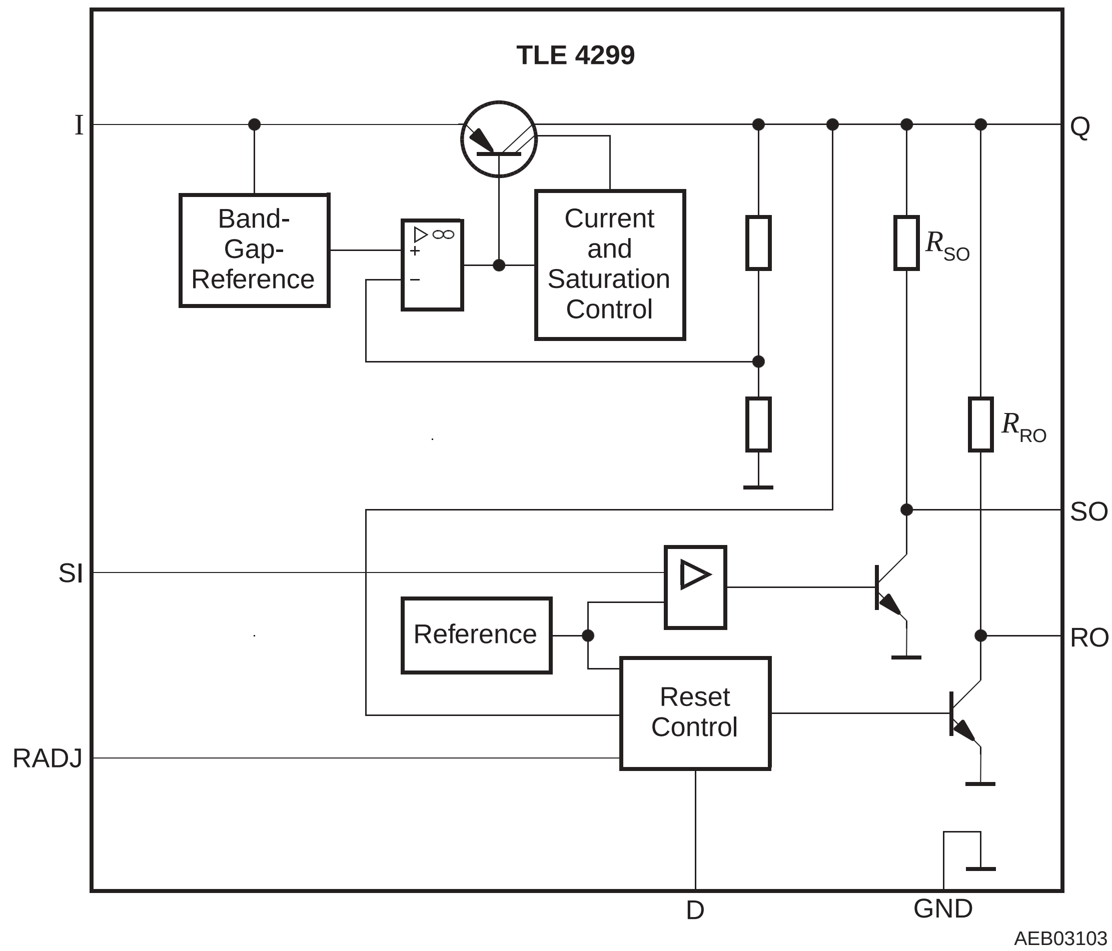


Figure 1 Block Diagram TLE 4299 GV33

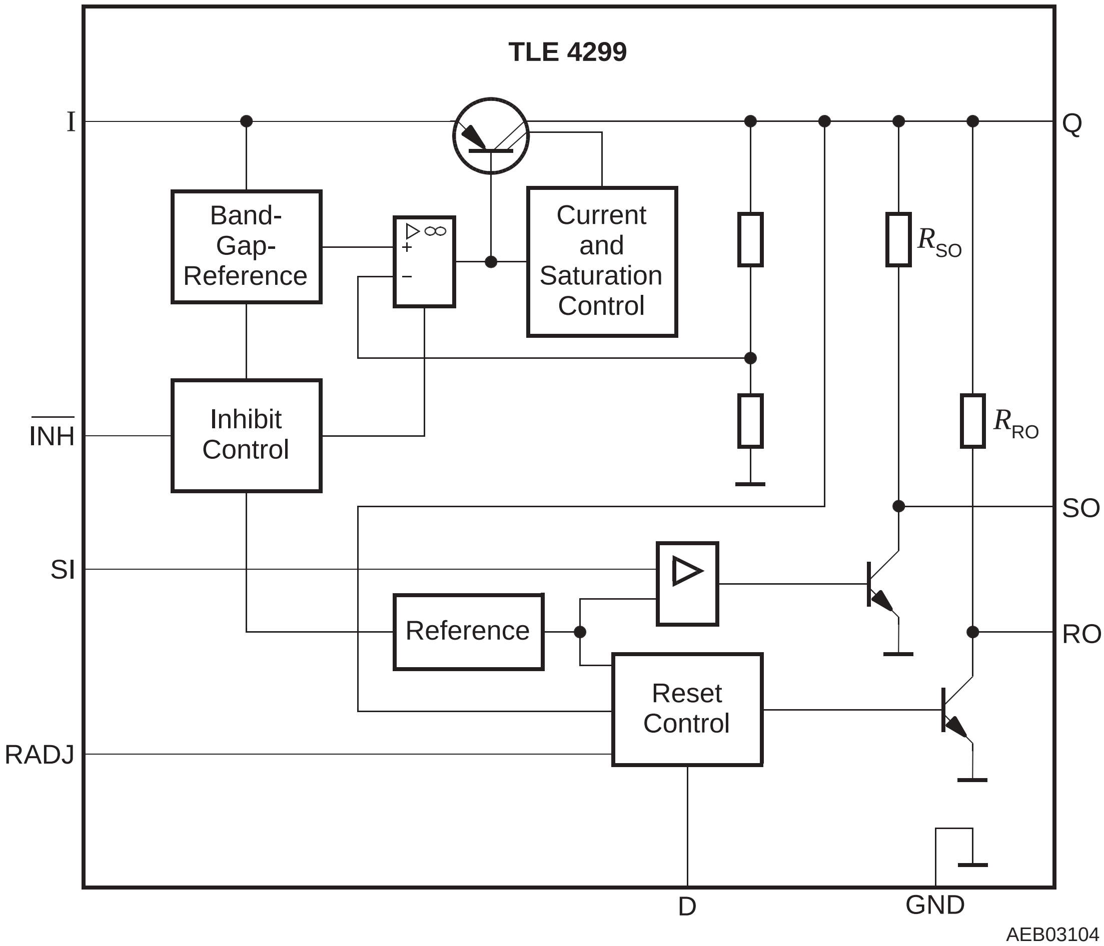


Figure 2 Block Diagram TLE 4299 GMV33

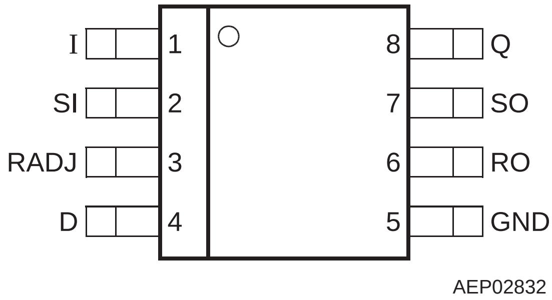


Figure 3 **Pin Configuration** (top view)

Pin Definitions and Functions (TLE 4299 GV33)

Pin No.	Symbol	Function
1	I	**Input;** block directly to GND on the IC with a ceramic capacitor.
2	SI	**Sense Input;** if not needed connect to Q.
3	RADJ	**Reset Threshold Adjust**; if not needed connect to GND.
4	D	**Reset Delay;** to select delay time, connect to GND via external capacitor.
5	GND	**Ground**
6	RO	**Reset Output;** the open-collector output is linked internally to Q via a 20kΩ pull-up resistor. Keep open, if the pin is not needed.
7	SO	**Sense Output;** open-collector output. Keep open, if the pin is not needed.
8	Q	**Output;** connect to GND with a 22 µF capacitor, 0.4 Ω < ESR < 3.7 Ω.[1]

[1] see characteristic curves

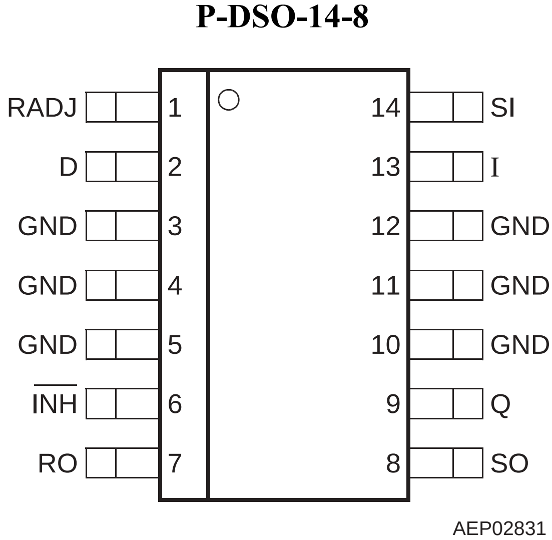


Figure 4 **Pin Configuration** (top view)

Pin Definitions and Functions (TLE 4299 GMV33)

Pin No.	Symbol	Function
1	RADJ	**Reset Threshold Adjust**; if not needed connect to GND.
2	D	**Reset Delay;** connect to GND via external delay capacitor for setting delay time.
3, 4, 5	GND	**Ground**
6	$\overline{INH}$	**Inhibit:** If not needed connect to Input pin I; A high signal switches the regulator ON.
7	RO	**Reset Output;** the open-collector output is linked internally to Q via a 20kΩ pull-up resistor. Keep open, if the pin is not needed.
8	SO	**Sense Output;** open-collector output. Keep open, if the pin is not needed.
9	Q	**Output;** connect to GND with a 22 µF capacitor, 0.4 Ω < ESR < 3.7 Ω.[1)]
10, 11, 12	GND	**Ground**
13	I	**Input;** block to GND directly at the IC by a ceramic capacitor.
14	SI	**Sense Input;** if not needed connect to Q.

1) see characteristic curves

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input I					
Input voltage	V_I	– 40	45	V	–
Inhibit Input $\overline{\text{INH}}$					
Input voltage	$V_{\overline{INH}}$	– 40	45	V	–
Sense Input SI					
Input voltage	V_{SI}	– 0.3	45	V	–
Input current	I_{SI}	-1	1	mA	–
Reset Threshold Adjust RADJ					
Input voltage	V_{RADJ}	– 0.3	7	V	–
Input current	I_{RADJ}	-10	10	mA	–
Reset Delay D					
Voltage	V_D	– 0.3	7	V	–
Reset Output RO					
Voltage	V_R	– 0.3	7	V	–
Sense Output SO					
Voltage	V_{SO}	– 0.3	7	V	–
Output Q					
Output voltage	V_Q	– 0.3	7	V	–
Output current	I_Q	– 5	–	mA	–

Absolute Maximum Ratings (cont'd)

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{Stg}	– 50	150	°C	–
Operating Range					
Input voltage	V_I	4.4	45	V	–
Junction temperature	T_j	– 40	150	°C	–
Thermal Data					
Junction-ambient for foot print only[1]	R_{thja}	–	200 130	K/W K/W	P-DSO-8-3 P-DSO-14-8
Junction-ambient for 300mm² cooling area[2]	R_{thja}	–	164 70	K/W K/W	P-DSO-8-3 P-DSO-14-8
Junction-pin	R_{thjp}	–	60 30	K/W K/W	P-DSO-8-3[3] P-DSO-14-8[4]

1) FR4, 80x80x1,5mm; 35µ Cu, 5µ Sn; Footprint only

2) FR4, 80x80x1,5mm; 35µ Cu, 5µ Sn; 300mm²

3) Measured to pin 5

4) Measured to pin 4

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. In the operating range, the functions given in the circuit description are fulfilled.

Characteristics

$V_I = 13.5$ V; $T_j = -40$ °C < T_j < 150 °C

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		
Output voltage	V_Q	3.23	3.30	3.37	V	1 mA ≤ I_Q ≤ 100 mA; 5.5 V ≤ V_I ≤ 16 V
Output voltage	V_Q	3.20	3.30	3.40	V	I_Q ≤ 150 mA; 5.5 V ≤ V_I ≤ 16 V
Current limit	I_Q	250	400	500	mA	–
Current consumption; $I_q = I_I - I_Q$	I_q	–	65	105	µA	Inhibit ON; I_Q ≤ 1 mA, T_j < 85 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	170	500	µA	Inhibit ON; I_Q = 10 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	0.7	2	mA	Inhibit ON; I_Q = 50 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	1	µA	$V_{\overline{INH}}$ = 0 V; T_j = 25 °C
Load regulation	ΔV_Q	–	5	30	mV	I_Q = 1 mA to 100 mA
Line regulation	ΔV_Q	–	10	25	mV	V_I = 6 V to 28 V; I_Q = 1 mA
Power Supply Ripple rejection	*PSRR*	–	66	–	dB	f_r = 100 Hz; V_r = 1 V_{SS}; I_Q = 100 mA

Inhibit (TLE 4299 GMV33 only)

Parameter	Symbol	min.	typ.	max.	Unit	Measuring Condition
Inhibit OFF voltage range	$V_{\overline{INH}\ OFF}$	–	–	0.8	V	V_Q off
Inhibit ON voltage range	$V_{\overline{INH}\ ON}$	3.5		-	V	V_Q on
High input current	$I_{\overline{INH}\ ON}$	–	3	5	µA	$V_{\overline{INH}}$ = 5V
Low input current	$I_{\overline{INH}\ OFF}$	–	0.5	2	µA	$V_{\overline{INH}}$ = 0.8 V

Characteristics (cont'd)

V_I = 13.5 V; T_j = – 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		
Reset Generator						
Switching threshold	V_{rt}	3.00	3.10	3.20	V	–
Reset threshold headroom	V_{RTHEAD}	50	200	300	mV	–
Reset pull up	R_{RO}	10	20	40	kΩ	–
Reset low voltage	V_R	–	0.17	0.40	V	V_Q < 3.0 V; internal R_{RO}; I_R = 1 mA
External reset pull up	$V_{R\ ext}$	5.6	–	–	kΩ	Pull up resistor Q
Delay switching threshold	V_{DT}	1.6	1.85	2.35	V	–
Switching threshold	V_{ST}	0.35	0.50	0.60	V	–
Reset delay low voltage	V_D	–	–	0.1	V	$V_Q < V_{RT}$
Charge current	I_{ch}	2.0	3.5	6.0	µA	V_D = 1 V
Power-up Reset delay time	t_d	36	51	60	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	1.2	3.0	µs	C_D = 100 nF
Reset Adjust Switching Threshold	VRADJ TH	1.26	1.36	1.44	V	V_Q < 3.5V
Input Voltage Sense						
Sense threshold high	$V_{SI\ high}$	1.34	1.45	1.54	V	–
Sense threshold low	$V_{SI\ low}$	1.26	1.36	1.44	V	–
Sense input switching hysteresis	$V_{SI\ HYST}$	50	90	130	mV	$V_{SI\ HYST} = V_{SI\ high} - V_{SI\ low}$
Sense output low voltage	$V_{SO\ low}$	–	0.1	0.4	V	V_{SI} < 1.20 V; V_i > 4.2 V; I_{SO} = 1mA
External SO pull up resistor	$R_{SO\ ext}$	5.6	–	–	kΩ	–
Sense input current	I_{SI}	– 1	0.1	1	µA	Si > 1.0V
Sense high reaction time	$t_{pd\ SO\ LH}$	–	2.4	4.0	µs	$R_{SO\ ext}$ = 5.6kΩ
Sense low reaction time	$t_{pd\ SO\ HL}$	–	2.5	6.0	µs	$R_{SO\ ext}$ = 5.6kΩ

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

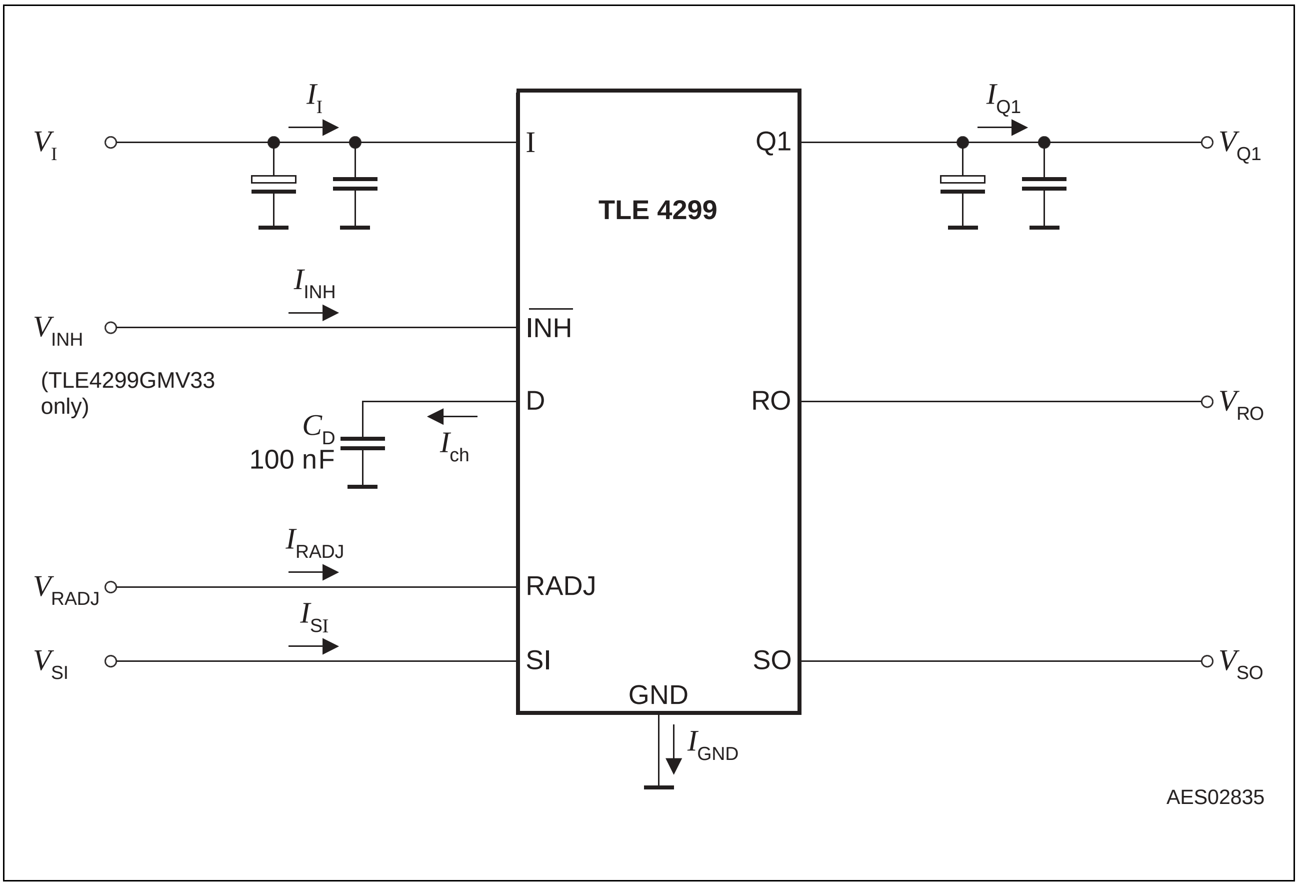


Figure 5 Measurement Circuit

Application Information

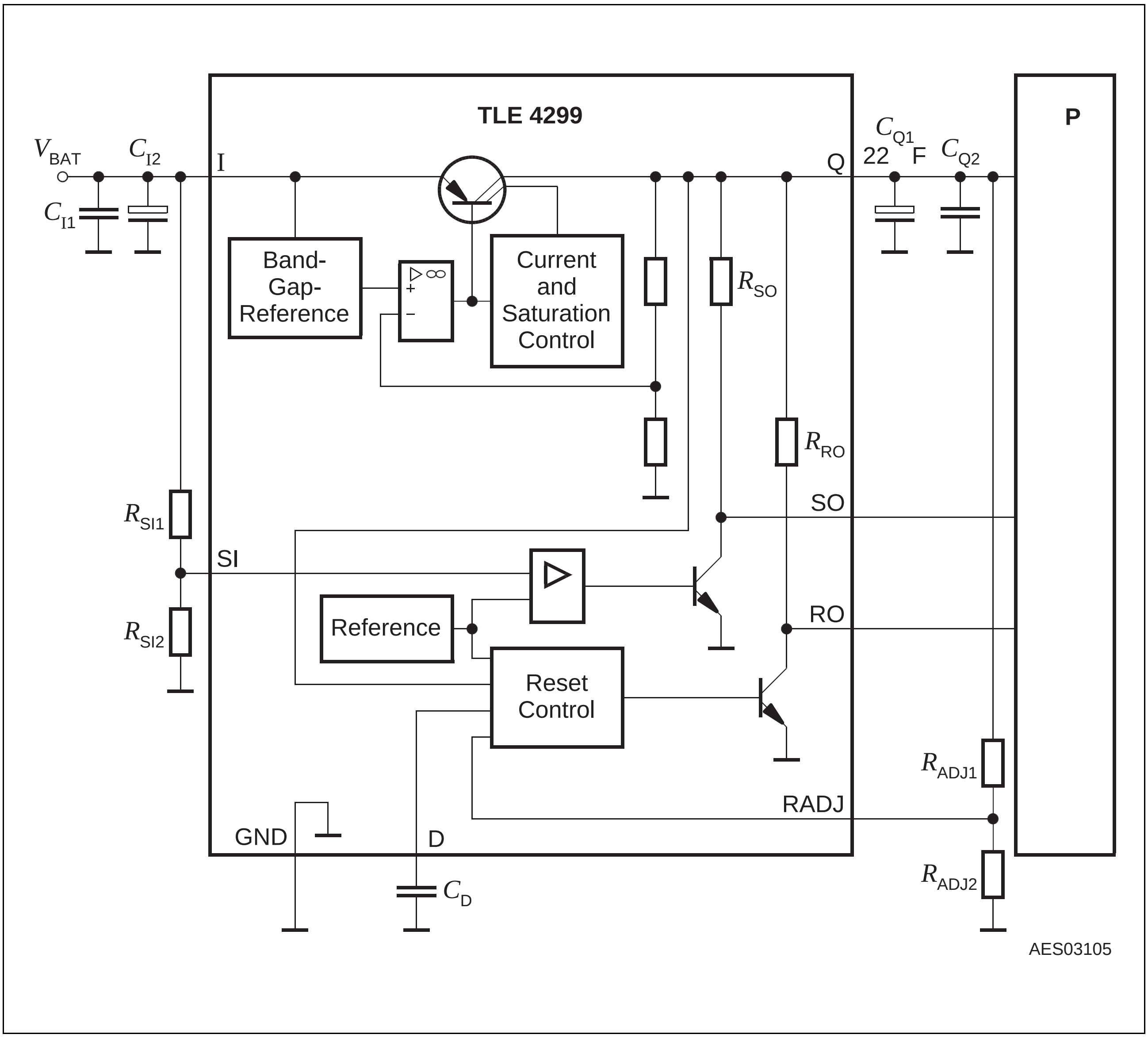


Figure 6 Application Diagram TLE 4299 GV33

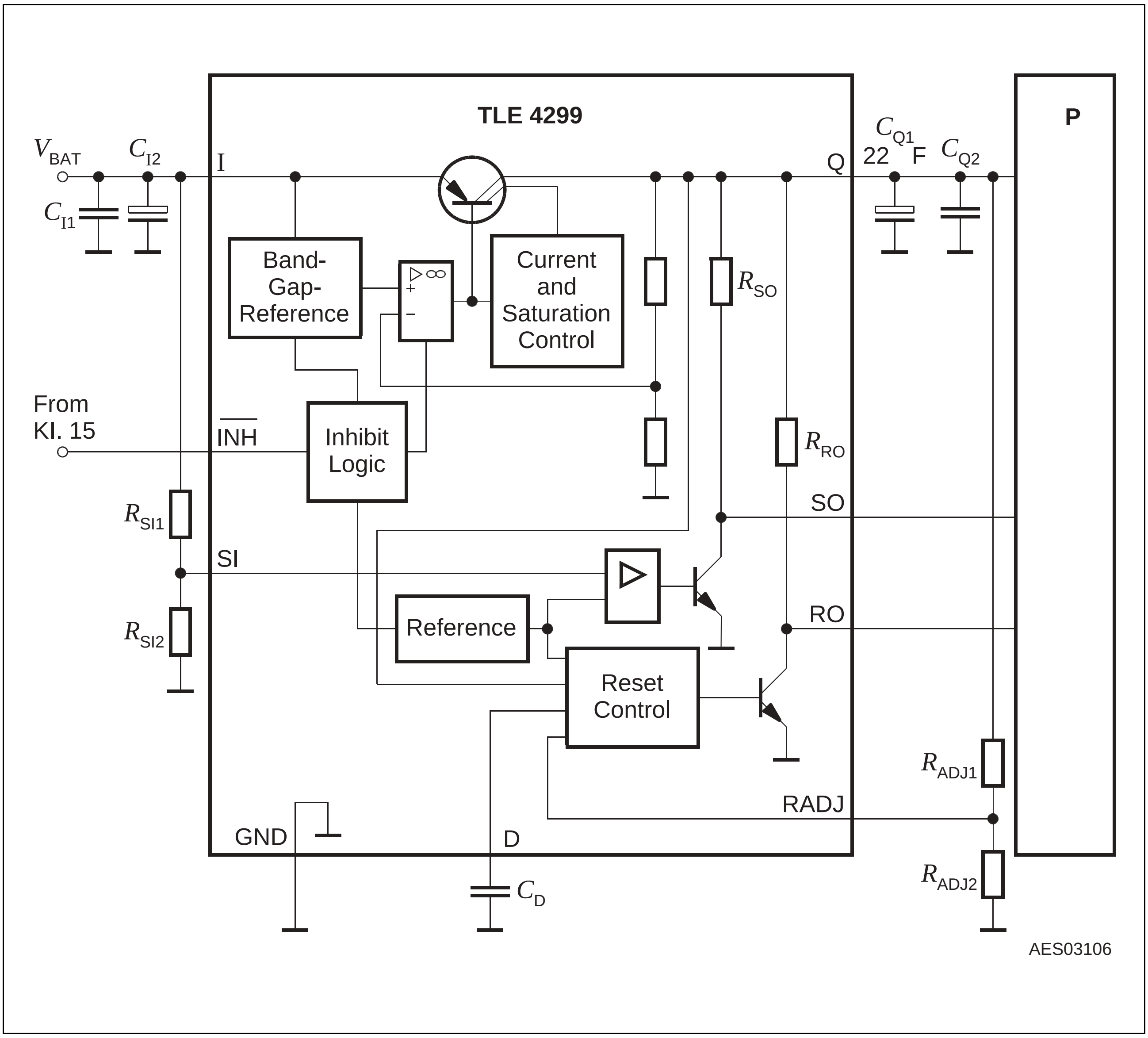


Figure 7 Application Diagram with Inhibit Function TLE4299 GMV33

The TLE 4299 supplies a regulated 3.3 V output voltage with an accuracy of 2% for an input voltage between 4.4 V and 45 V in the temperature range of T_j = – 40 to 150 °C, in an output current range of 1 mA to 100 mA.

The device is capable to supply 150 mA with an accuracy of 3%. For protection at high input voltage above 25 V, the output current is reduced (SOA protection).

An input capacitor is necessary for compensating line influences and to limit steep input edges. A resistor of approx. 1 Ω in series with C_I, can damp the LC of the input inductivity and the input capacitor.

The voltage regulator requires for stability an output capacitor C_Q of at least 22 µF with an 0.4Ω < ESR < 3.7Ω for the whole load- and temperature range. For more detailed information, refer to the characteristical curves.

Reset

The power on reset feature is necessary for a defined start of the microprocessor when switching on the application. For the reset delay time after the output voltage of the regulator is above the reset threshold, the reset signal is set High again. The reset delay time is defined by the reset delay capacitor C_D at pin D.

The under-voltage reset circuitry supervises the output voltage. In case V_Q decreases below the reset threshold the reset output is set LOW after the reset reaction time. The reset LOW signal is generated down to an output voltage V_Q to 1 V. Both the reset reaction time and the reset delay time is defined by the capacitor value.

The power on reset delay time is defined by the charging time of an external delay capacitor C_D.

$$C_D = (t_d \times I_D) / \Delta V \quad [1]$$

$$t_d = C_D \times \Delta V / I_D \quad [2]$$

With C_D reset delay capacitor
t_d reset delay time
ΔV $= V_{DT}$, typical 1.8 V for power up reset
I_{ch} charge current typical 3.5 µA

For a delay capacitor C_D =100 nF the typical power on reset delay time is 51 ms.

The reset reaction time t_{RR} is the time it takes the voltage regulator to set reset output LOW after the output voltage has dropped below the reset threshold. It is typically 1.2 µs for delay capacitor of 100 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{RR} \sim 10 \text{ ns / nF} \times C_D \quad [3]$$

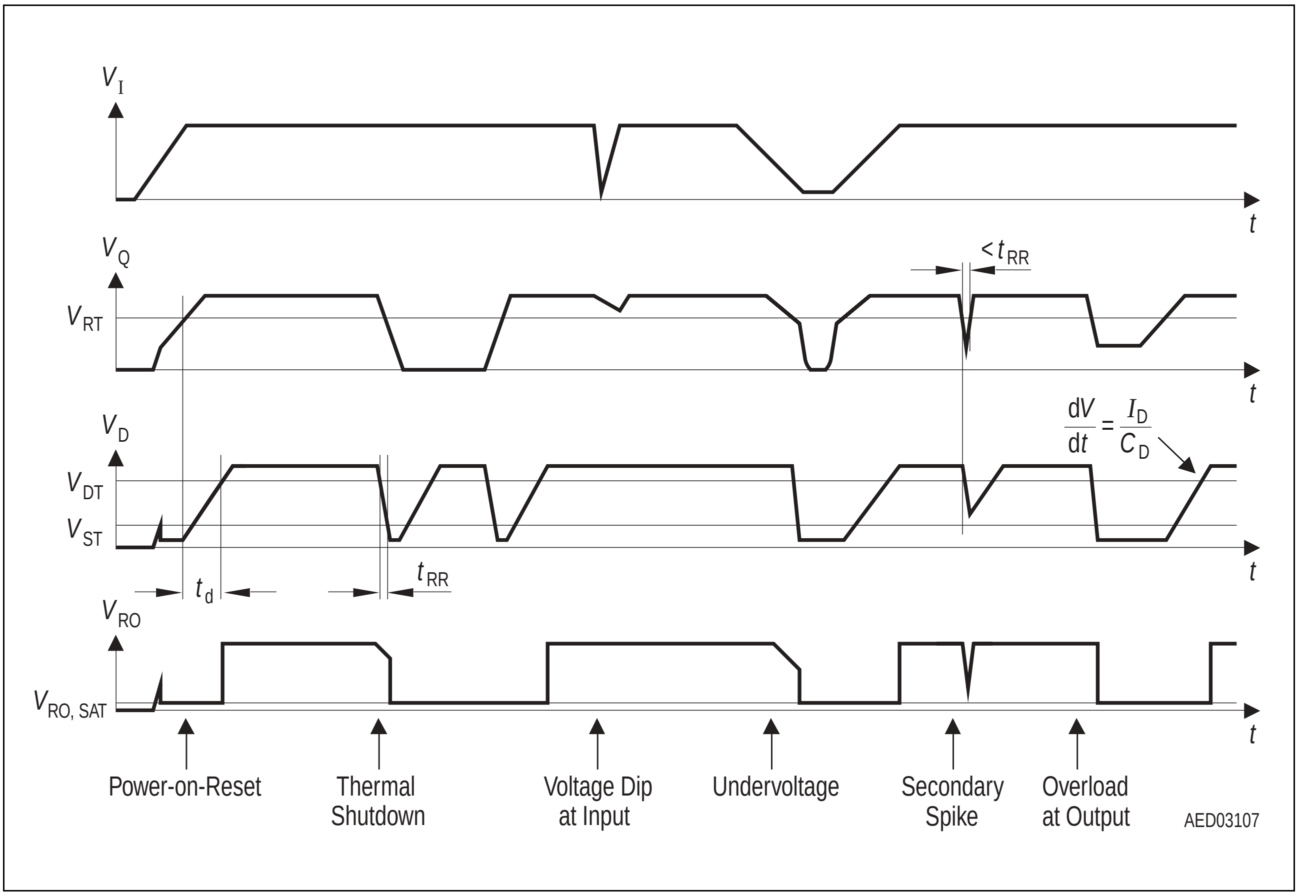


Figure 8 Reset Timing Diagram

The reset output is an open collector output. An external pull-up can be added with a resistor value of at least 5.6 kΩ.

In addition the reset switching threshold can be adjusted by an external voltage divider. The feature is useful for microprocessors which guarantee safe operation down to voltages below the internally set reset threshold of 3.10V typical. If the internal used reset threshold of typical 3.10V is used, the pin RADJ has to beconnected to GND. If a lower reset threshold is required by the system, a voltage divider defines the reset threshold VRth between 2.5V and 3.10V as long as the Input Voltage V_I>4.4V

$V_{Rth} = V_{RADJ\ TH}$ * $(R_{ADJ1} + R_{ADJ2}) / R_{ADJ2}$ (3)

$V_{RADJ\ TH}$ is typical 1.36 V.

Early Warning

The early warning function compares a voltage defined by the user to an internal reference voltage. Therefore the supervised voltage has to be scaled down by an external voltage divider in order to compare it to the internal sense threshold of typical 1.36 V. The sense output pin is set low, when the voltage at SI falls below this threshold.

A typical example where the circuit can be used is to supervise the input voltage V_{I} to give the microcontroller a prewarning of low battery condition.

Calculation to the voltage divider can be easily done since the sense input current can be neglected.

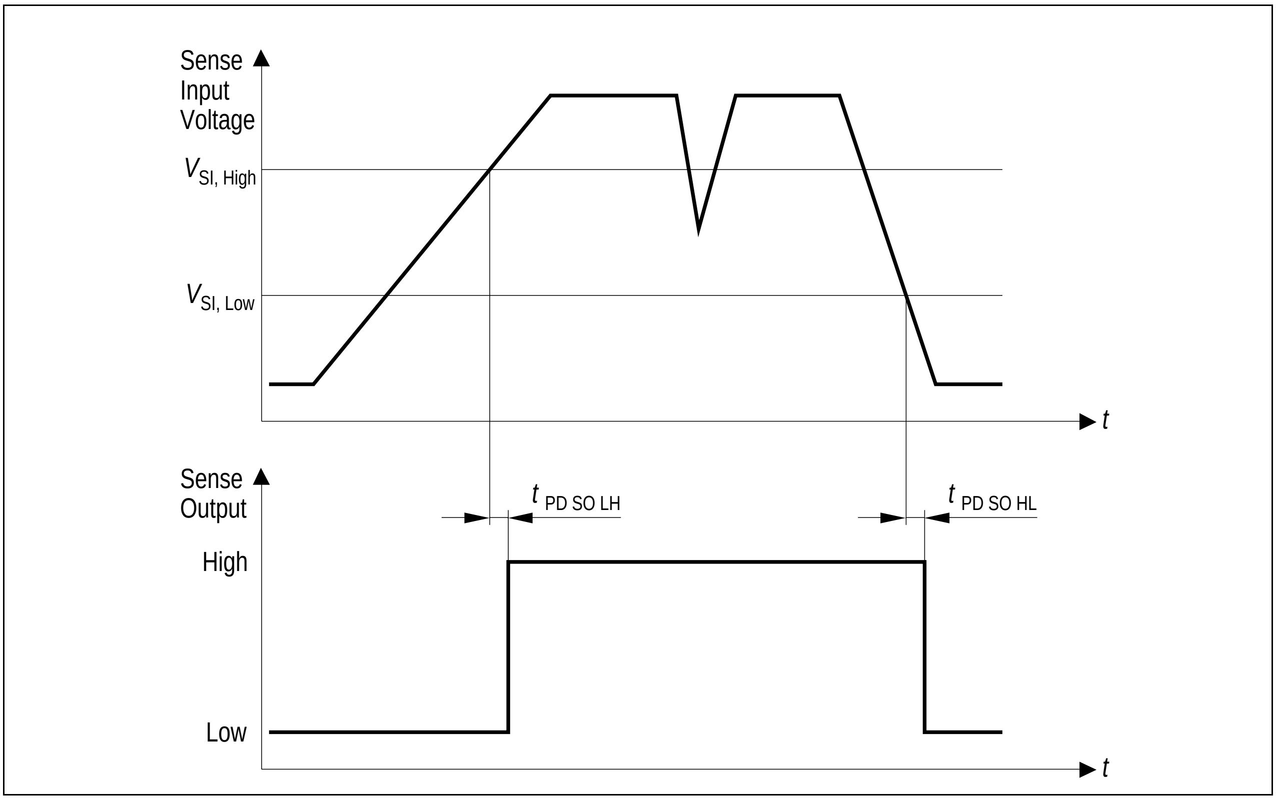


Figure 9 Sense Timing Diagram

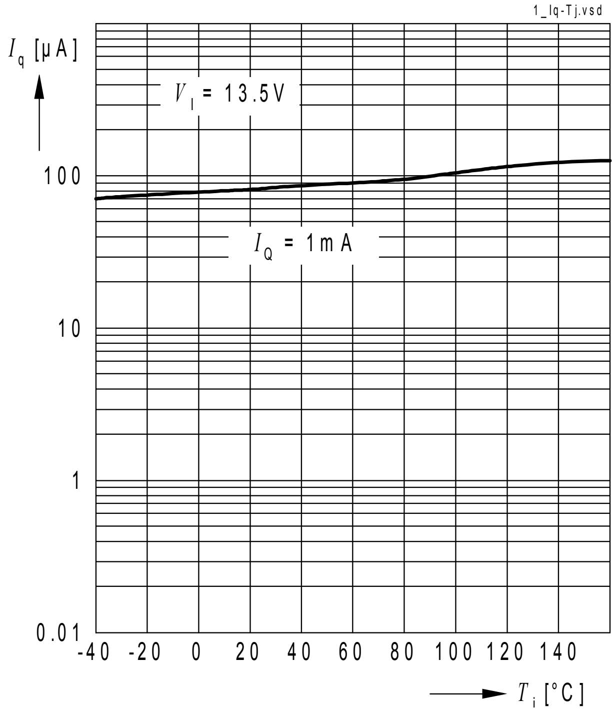
$$V_{\mathrm{thHL}} = (R_{\mathrm{SI1}} + R_{\mathrm{SI2}})/R_{\mathrm{SI2}} \times V_{\mathrm{SI\ low}} \qquad [4]$$

$$V_{\mathrm{thLH}} = (R_{\mathrm{SI1}} + R_{\mathrm{SI2}})/R_{\mathrm{SI2}} \times V_{\mathrm{SI\ high}} \qquad [5]$$

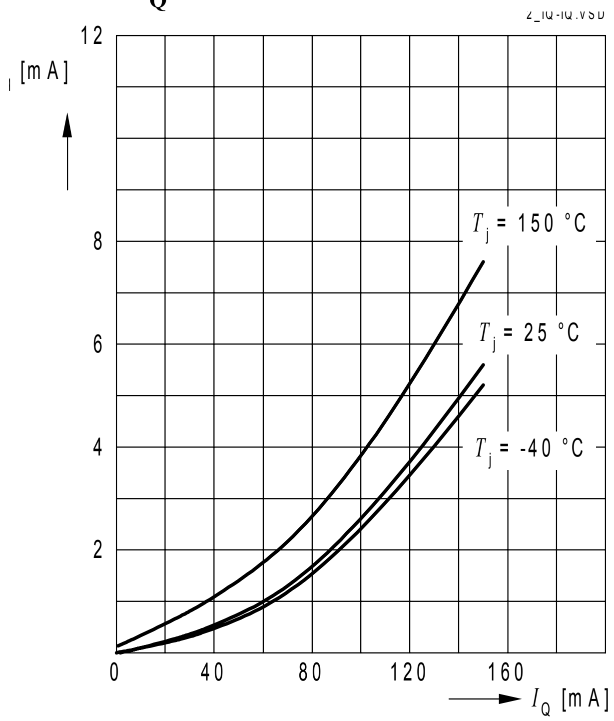
The sense in comparator uses a hysteresis of typical 90 mV. This hysteresis of the supervised threshold is multiplied by the resistor dividers amplification $(R_{\mathrm{SI1}} + R_{\mathrm{SI2}})/R_{\mathrm{SI1}}$.

The sense in comparator can also be used for receiving data with a threshold of typical 1.36 V and a hysteresis of 90 mV. Of course also the data signal can be scaled down with a resistive divider as shown above. With a typical delay time of 2.5 µs for positive transitions and 2.4 µs for negative transitions receiving data of up to 100 kBaud are possible. The sense output is an open collector output.

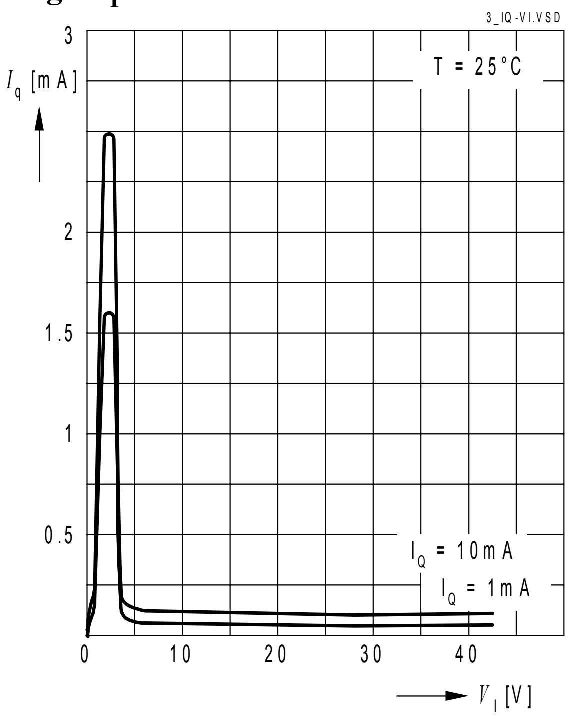
Current Consumption I_q versus Junction Temperature T_j



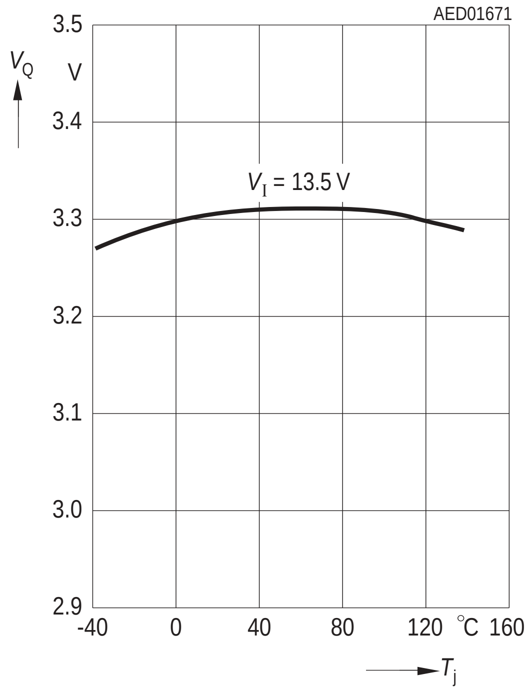
Current Consumption I_q versus Output Current I_Q



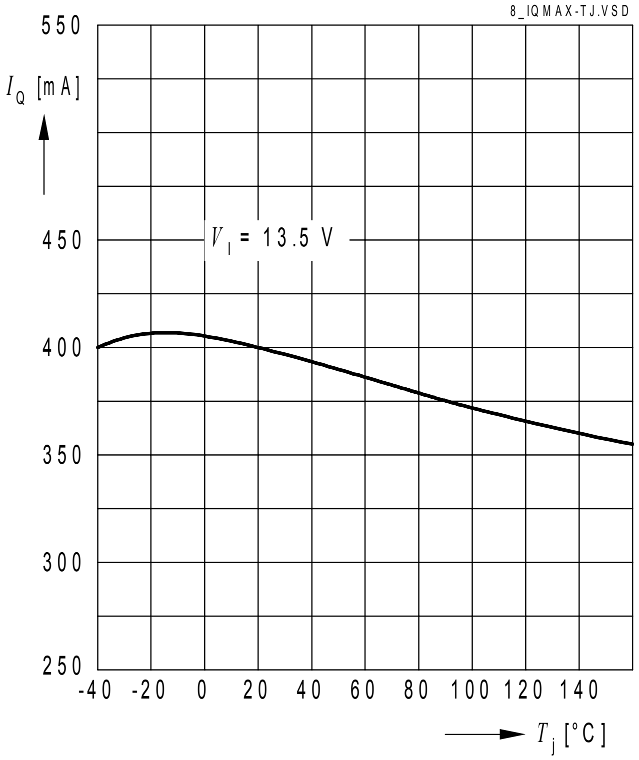
Current Consumption I_q versus Input Voltage V_I



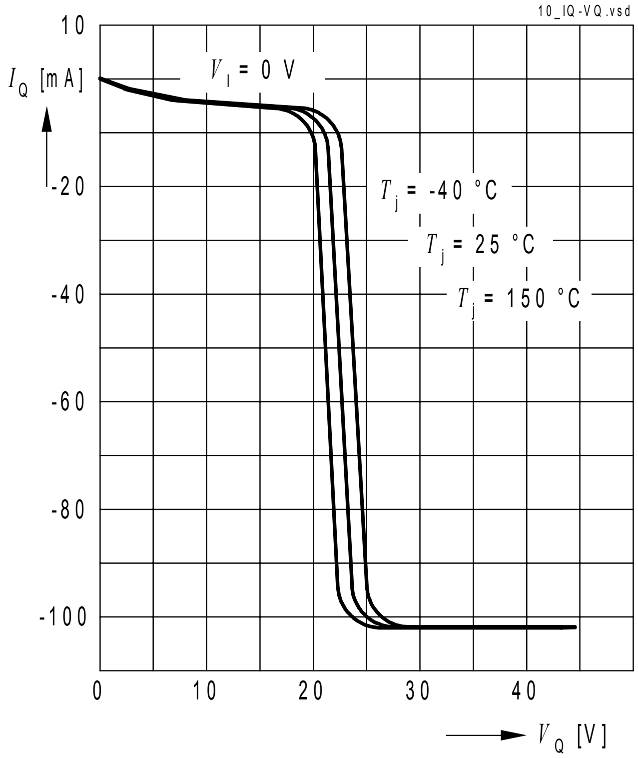
Output Voltage V_Q versus Junction Temperature T_j



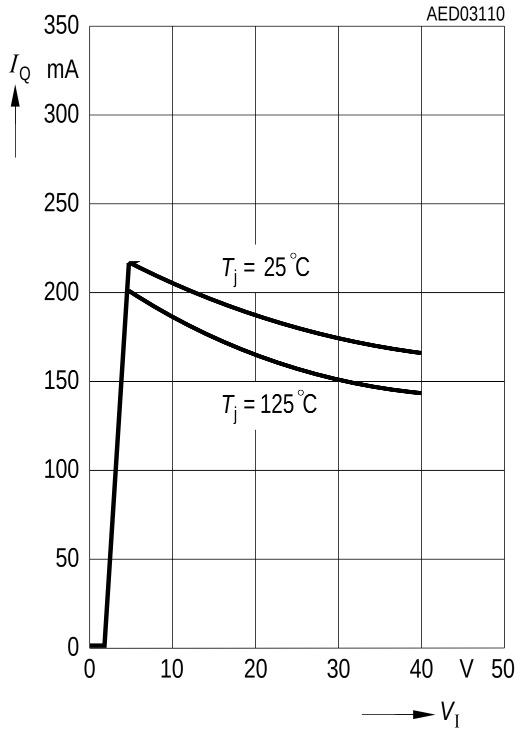
Maximum Output Current I_Q versus Junction Temperature T_j



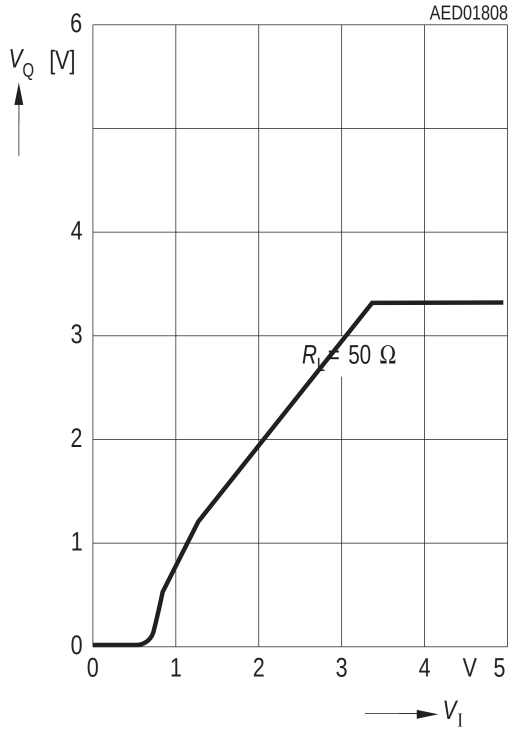
Reverse Output Current I_Q versus Output Voltage V_Q



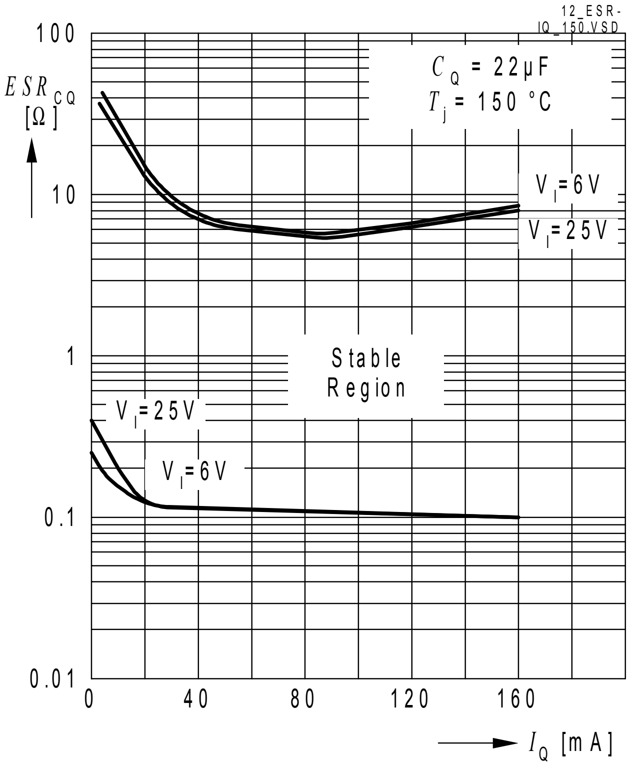
Maximum Output Current I_Q versus Input Voltage V_I



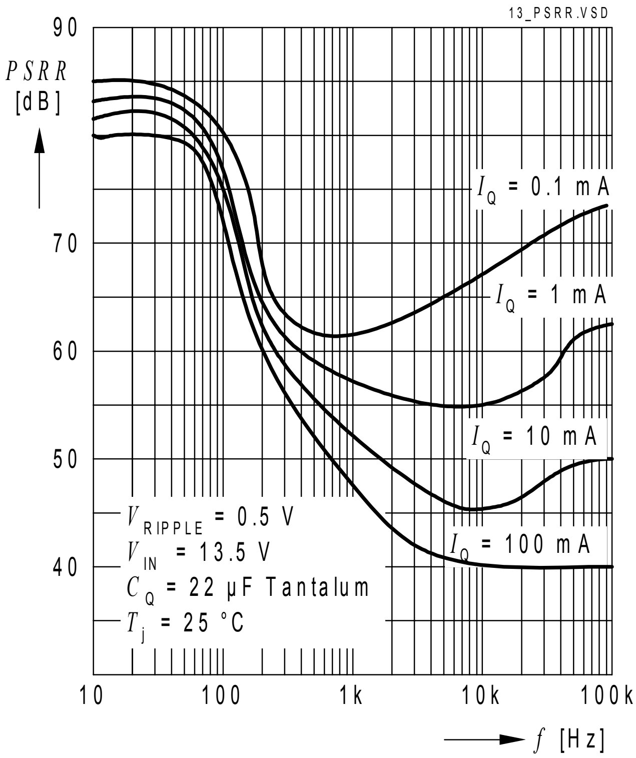
Output Voltage V_Q at Input Voltage Extremes



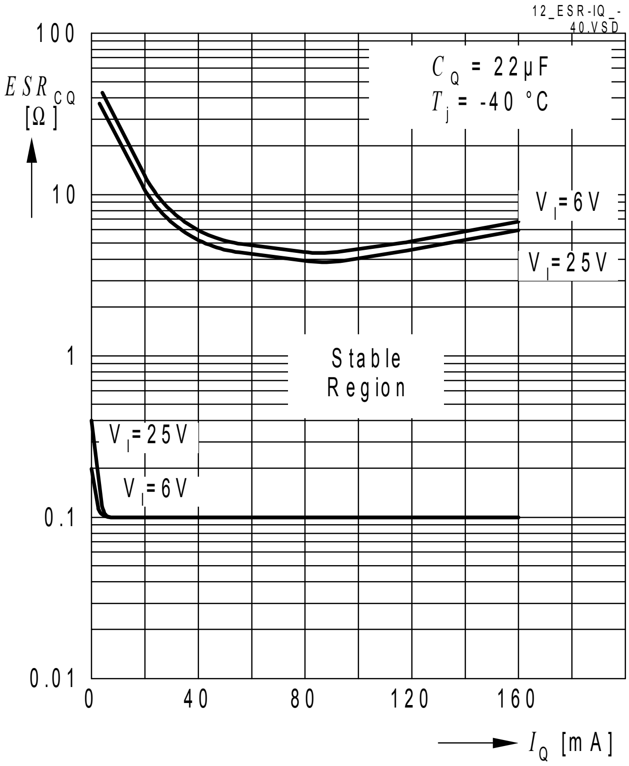
Region of Stability



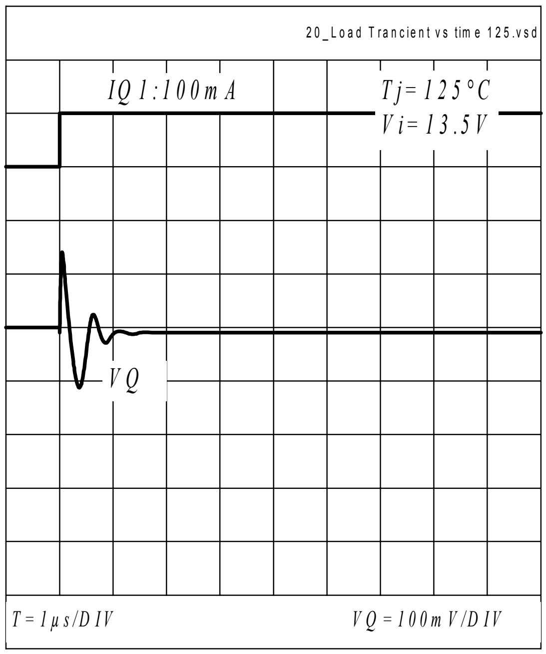
Power Supply Ripple Rejection PSRR versus Frequency f



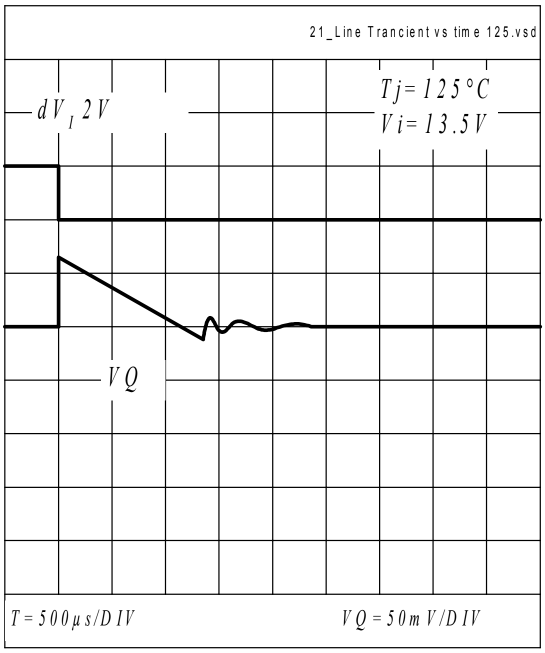
Region of Stability



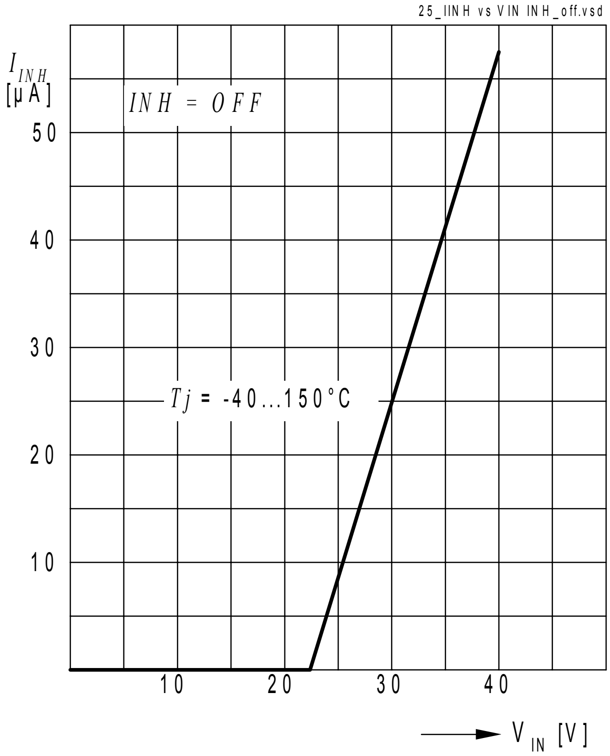
Load Transient Response Peak Voltage D_{VQ}



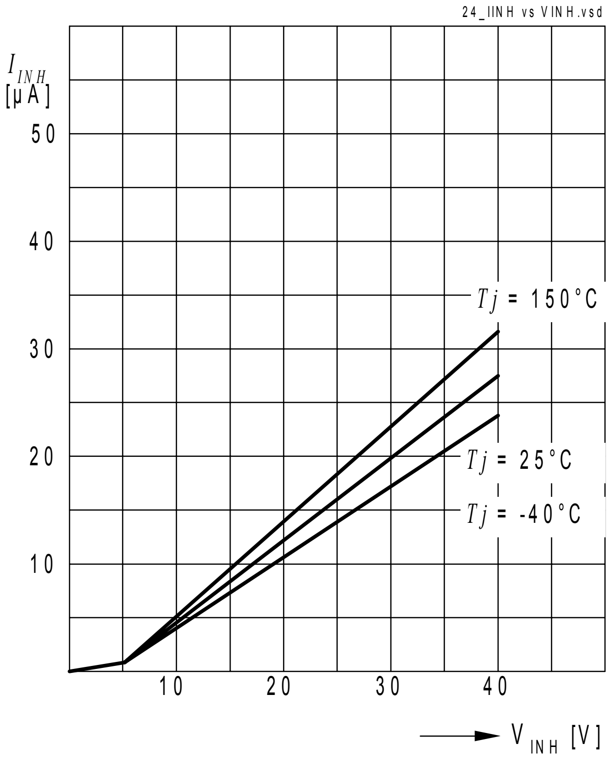
Line Transient Response Peak Voltage D_{VQ}



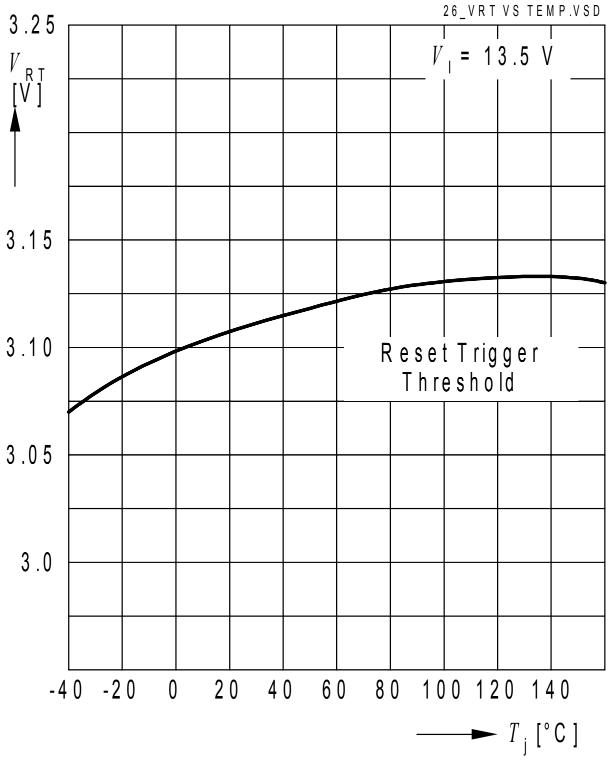
Inhibit Input Current at Input Voltage Extremes (INH=OFF)



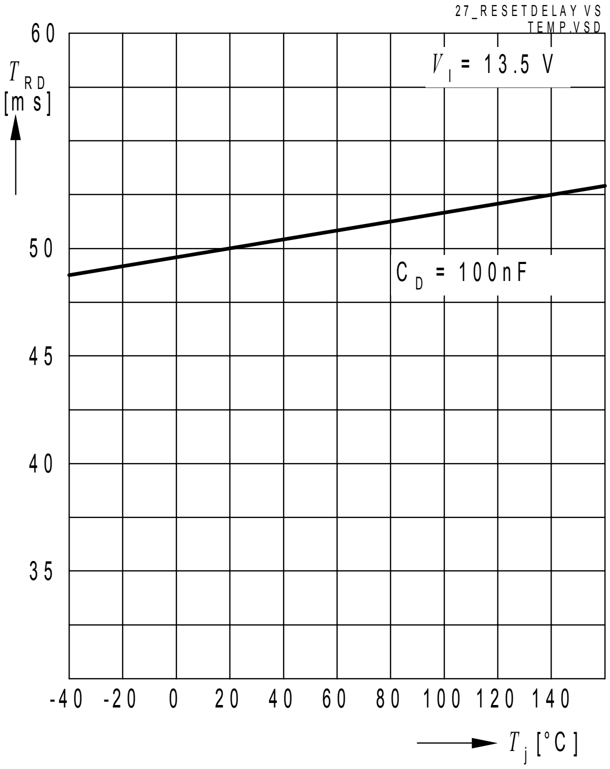
Inhibut Input Current I_{INH} at Inhibit Input Voltage Extremes



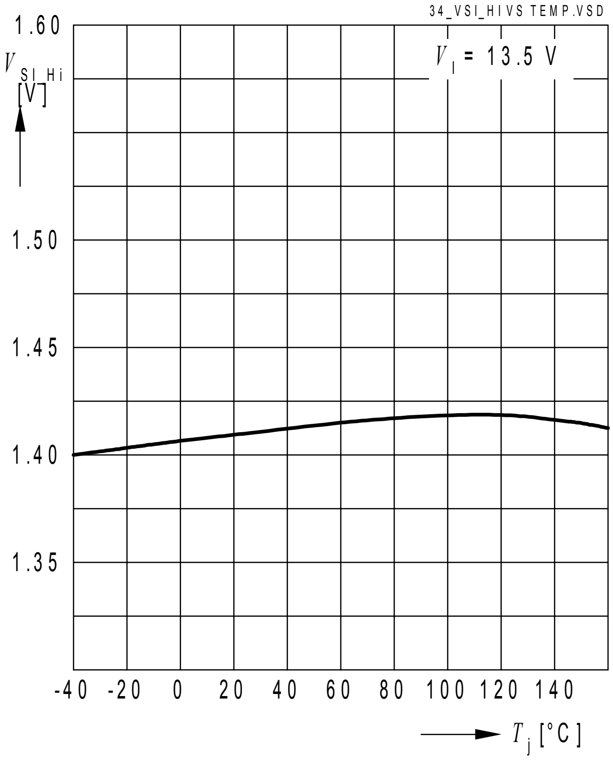
Reset Trigger Threshold V_{RT} versus Junction Temperature Tj



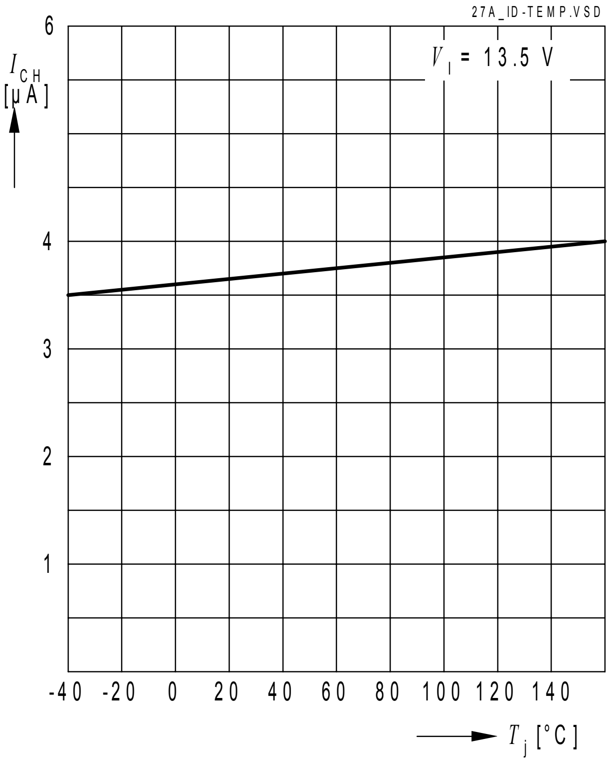
Reset Delay Time T_{RD} versus Junction Temperature Tj



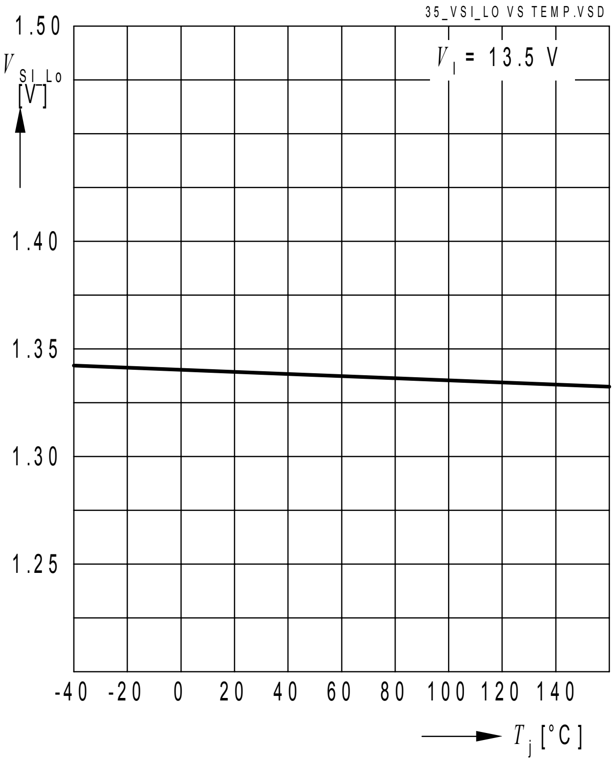
Sense Threshold High versus Junction Temperature Tj



Delay Capacitor Charge Current versus Junction Temperature Tj

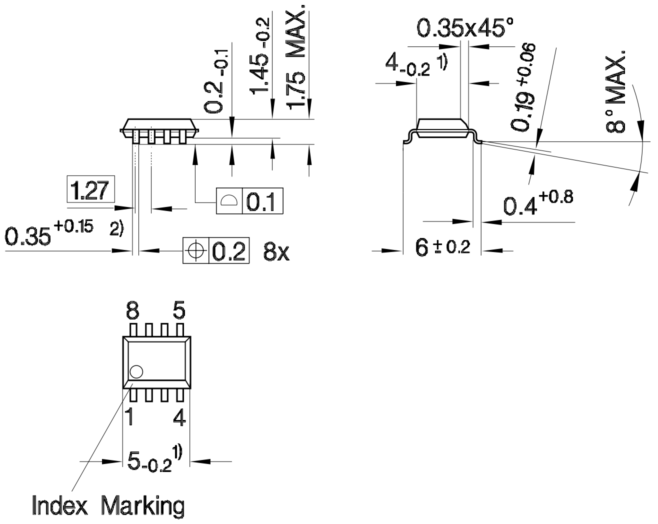


Sense Threshold Low versus Junction Temperature Tj



Package Outlines

P-DSO-8-3 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

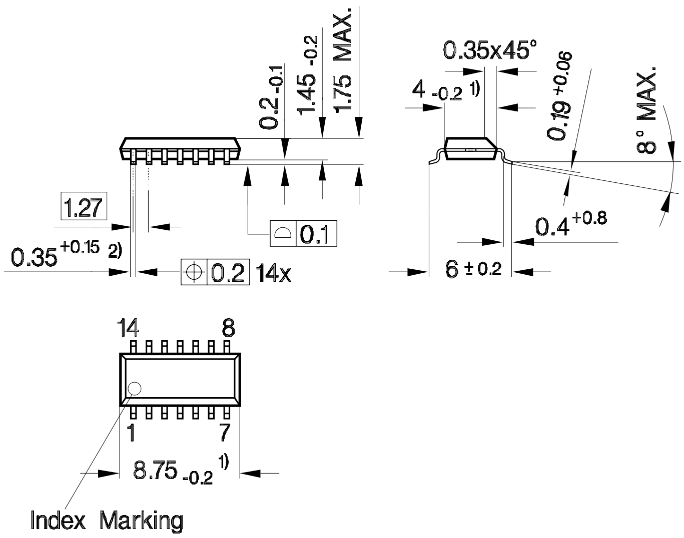
GPS05121

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm

P-DSO-14-8 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS05093

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm

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