NCP5318

Two/Three/Four-Phase Buck CPU Controller

The NCP5318 provides full−featured and flexible control conforming to the Intel® VRM 10.1 specification for high−performance CPUs. The IC can be programmed as a two−, three− or four−phase buck controller, and the per−phase switching frequency can be as high as 1.0 MHz. Combined with external gate drivers and power components, the controller implements a compact, highly integrated multi−phase buck converter.

Enhanced V^{2}™ control inherently compensates for variations in both line and load, and achieves current sharing between phases. This control scheme provides fast transient response, reducing the need for large banks of output capacitors and higher switching frequency.

Features

- Switching Regulator Controller
  - Programmable 2/3/4 Phase Operation
  - Lossless Current Sensing
  - Enhanced V^2 Control Method Provides Fast Transient Response
  - Programmable Up to 1.0 MHz Switching Frequency Per Phase
  - Programmable Adaptive Voltage Positioning
  - Programmable Soft−Start Time
- Current Sharing
  - Differential Current Sense Pins for Each Phase
  - Current Sharing Within 10% Between Phases
- Protection Features
  - Programmable Latching Overcurrent Protection
  - “111110” and “111111” DAC Code Fault
  - Latched Overvoltage Protection
  - Undervoltage Lockout
  - External Enable Control
  - Three−State MOSFET Driver Control through DRVON Signal
- System Power Management
  - 6−Bit DAC with 0.5% Tolerance Compatible with VRM 10.1 Specification
  - Programmable Lower Power Good Threshold
  - Power Good Output with Delay
  - Pre−set No Load Offset Voltage
- Pb−Free Package is Available*

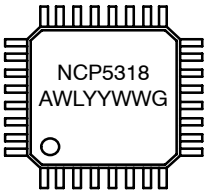
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

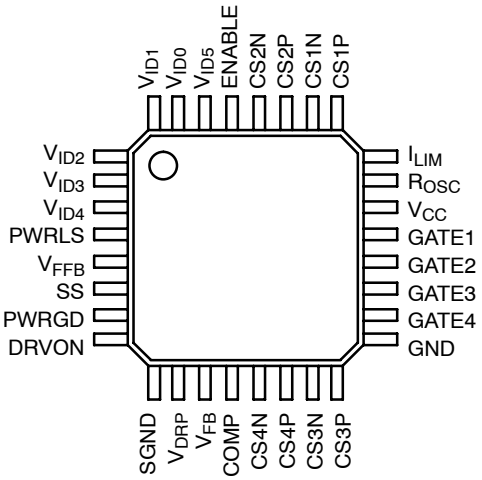
LQFP−32
FT SUFFIX
CASE 873A



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS

(Top View)



ORDERING INFORMATION

Device	Package	Shipping†
NCP5318FTR2	LQFP−32	2000 Tape & Reel
NCP5318FTR2G	LQFP−32 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

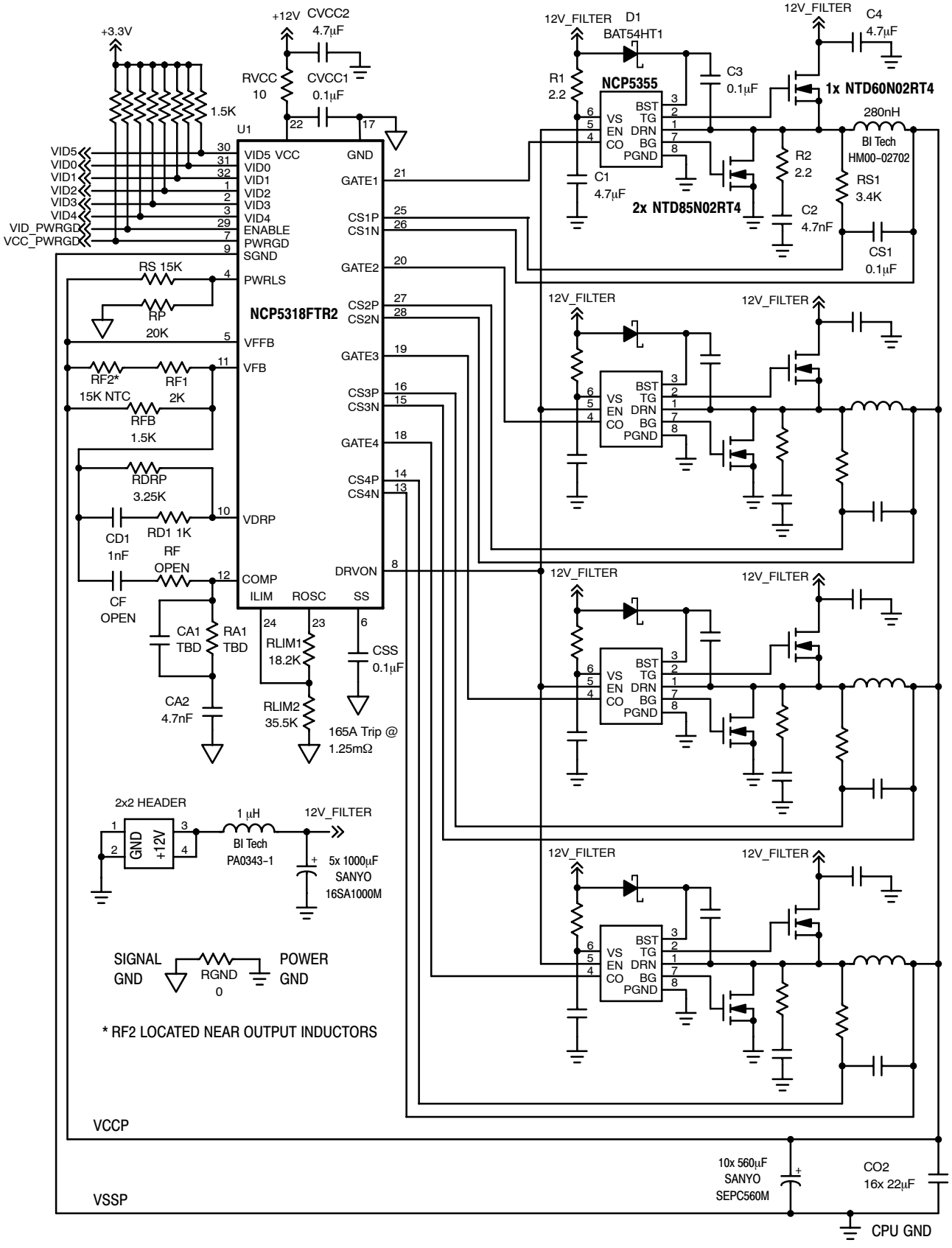


Figure 1. 4−Phase Solution for VRM10.1: 120 A max, 101 A thermals, 1.4 Vo, 400 kHz, 1 mΩ LL

MAXIMUM RATINGS

Rating		Value	Unit
Operating Junction Temperature		150	°C
Lead Temperature Soldering, Reflow (Note 1)	NCP5318FTR2 NCP5318FTR2G	230 peak 260 peak	°C
Storage Temperature Range		−65 to 150	°C
ESD Susceptibility: Human Body Model		2.0	kV
JEDEC Moisture Sensitivity Level	NCP5318FTR2 NCP5318FTR2G	1 3	– –
Package Thermal Resistance: $R_{\theta JA}$		52	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Number	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1−3, 30−32	V_{ID0}−V_{ID5}	18 V	−0.3 V	1.0 mA	1.0 mA
4	PWRLS	7.0 V	−0.3 V	1.0 mA	1.0 mA
5	V_{FFB}	7.0 V	−0.3 V	1.0 mA	1.0 mA
6	SS	7.0 V	−0.3 V	1.0 mA	1.0 mA
7	PWRGD	18 V	−0.3 V	1.0 mA	20 mA
8	DRVON	7.0 V	−0.3 V	1.0 mA	1.0 mA
9	SGND	1.0 V	−1.0 V	1.0 mA	–
10	V_{DRP}	7.0 V	−0.3 V	1.0 mA	1.0 mA
11	V_{FB}	7.0 V	−0.3 V	1.0 mA	1.0 mA
12	COMP	7.0 V	−0.3 V	1.0 mA	1.0 mA
13	CS4N	18 V	−0.3 V	1.0 mA	1.0 mA
14	CS4P	18 V	−0.3 V	1.0 mA	1.0 mA
15	CS3N	18 V	−0.3 V	1.0 mA	1.0 mA
16	CS3P	18 V	−0.3 V	1.0 mA	1.0 mA
17	GND	–	–	0.4 A 1.0 μs, 100 mA DC	–
18−21	GATE4−GATE1	18 V	−0.3 V	0.1 A 1.0 μs, 25 mA DC	0.1 A 1.0 μs, 25 mA DC
22	V_{CC}	18 V	−0.3 V	–	0.4 A 1.0 μs, 100 mA DC
23	R_{OSC}	7.0 V	−0.3 V	1.0 mA	1.0 mA
24	I_{LIM}	7.0 V	−0.3 V	1.0 mA	1.0 mA
25	CS1P	18 V	−0.3 V	1.0 mA	1.0 mA
26	CS1N	18 V	−0.3 V	1.0 mA	1.0 mA
27	CS2P	18 V	−0.3 V	1.0 mA	1.0 mA
28	CS2N	18 V	−0.3 V	1.0 mA	1.0 mA
29	ENABLE	18 V	−0.3 V	1.0 mA	1.0 mA

ELECTRICAL CHARACTERISTICS (0°C < T_A < 70°C; V_{CC} = 12 V; C_{GATEx} = 100 pF, C_{COMP} = 0.01 μF, C_{SS} = 0.1 μF, C_{VCC} = 0.1 μF, R_{ROSC} = 95.3 kΩ, V(I_{LIM}) = 1.0 V, DAC Code 010100; unless otherwise noted)

VOLTAGE IDENTIFICATION (VID)

Voltage Identification Bits (Connect V_{FB} to COMP, measure COMP)						Nominal Voltage (V)	Min	Typ	Max	
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	V_{ID5}		−0.5%	No Load	+0.5%	Units
0	1	0	1	0	0	0.8375	0.8144	0.8185	0.8226	V
0	1	0	0	1	1	0.8500	0.8268	0.8310	0.8352	V
0	1	0	0	1	0	0.8625	0.8393	0.8435	0.8477	V
0	1	0	0	0	1	0.8750	0.8517	0.8560	0.8603	V
0	1	0	0	0	0	0.8875	0.8642	0.8685	0.8728	V
0	0	1	1	1	1	0.9000	0.8766	0.8810	0.8854	V
0	0	1	1	1	0	0.9125	0.8890	0.8935	0.8980	V
0	0	1	1	0	1	0.9250	0.9015	0.9060	0.9105	V
0	0	1	1	0	0	0.9375	0.9139	0.9185	0.9231	V
0	0	1	0	1	1	0.9500	0.9263	0.9310	0.9357	V
0	0	1	0	1	0	0.9625	0.9388	0.9435	0.9482	V
0	0	1	0	0	1	0.9750	0.9512	0.9560	0.9608	V
0	0	1	0	0	0	0.9875	0.9637	0.9685	0.9733	V
0	0	0	1	1	1	1.0000	0.9761	0.9810	0.9859	V
0	0	0	1	1	0	1.0125	0.9885	0.9935	0.9985	V
0	0	0	1	0	1	1.0250	1.0010	1.0060	1.0110	V
0	0	0	1	0	0	1.0375	1.0134	1.0185	1.0236	V
0	0	0	0	1	1	1.0500	1.0258	1.0310	1.0362	V
0	0	0	0	1	0	1.0625	1.0383	1.0435	1.0487	V
0	0	0	0	0	1	1.0750	1.0507	1.0560	1.0613	V
0	0	0	0	0	0	1.0875	1.0632	1.0685	1.0738	V
1	1	1	1	1	1	OFF				V
1	1	1	1	1	0	OFF				V
1	1	1	1	0	1	1.1000	1.0756	1.0810	1.0864	V
1	1	1	1	0	0	1.1125	1.0880	1.0935	1.0990	V
1	1	1	0	1	1	1.1250	1.1005	1.1060	1.1115	V
1	1	1	0	1	0	1.1375	1.1129	1.1185	1.1241	V
1	1	1	0	0	1	1.1500	1.1253	1.1310	1.1367	V
1	1	1	0	0	0	1.1625	1.1378	1.1435	1.1492	V
1	1	0	1	1	1	1.1750	1.1502	1.1560	1.1618	V
1	1	0	1	1	0	1.1875	1.1627	1.1685	1.1743	V
1	1	0	1	0	1	1.2000	1.1751	1.1810	1.1869	V
1	1	0	1	0	0	1.2125	1.1875	1.1935	1.1995	V
1	1	0	0	1	1	1.2250	1.2000	1.2060	1.2120	V
1	1	0	0	1	0	1.2375	1.2124	1.2185	1.2246	V

*VID Code is for reference only.

†V_{OUT} No Load is the input to the error amplifier.

ELECTRICAL CHARACTERISTICS (0°C < T_A < 70°C; V_{CC} = 12 V; C_{GATEx} = 100 pF, C_{COMP} = 0.01 μF, C_{SS} = 0.1 μF, C_{VCC} = 0.1 μF, R_{ROSC} = 95.3 kΩ, V(I_{LIM}) = 1.0 V, DAC Code 010100; unless otherwise noted)

VOLTAGE IDENTIFICATION (VID) (continued)

Voltage Identification Bits (Connect V_{FB} to COMP, measure COMP)						Nominal Voltage (V)	Min	Typ	Max	
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	V_{ID5}		−0.5%	No Load	+0.5%	Units
1	1	0	0	0	1	1.2500	1.2248	1.2310	1.2372	V
1	1	0	0	0	0	1.2625	1.2373	1.2435	1.2497	V
1	0	1	1	1	1	1.2750	1.2497	1.2560	1.2623	V
1	0	1	1	1	0	1.2875	1.2622	1.2685	1.2748	V
1	0	1	1	0	1	1.3000	1.2746	1.2810	1.2874	V
1	0	1	1	0	0	1.3125	1.2870	1.2935	1.3000	V
1	0	1	0	1	1	1.3250	1.2995	1.3060	1.3125	V
1	0	1	0	1	0	1.3375	1.3119	1.3185	1.3251	V
1	0	1	0	0	1	1.3500	1.3243	1.3310	1.3377	V
1	0	1	0	0	0	1.3625	1.3368	1.3435	1.3502	V
1	0	0	1	1	1	1.3750	1.3492	1.3560	1.3628	V
1	0	0	1	1	0	1.3875	1.3617	1.3685	1.3753	V
1	0	0	1	0	1	1.4000	1.3741	1.3810	1.3879	V
1	0	0	1	0	0	1.4125	1.3865	1.3935	1.4005	V
1	0	0	0	1	1	1.4250	1.3990	1.4060	1.4130	V
1	0	0	0	1	0	1.4375	1.4114	1.4185	1.4256	V
1	0	0	0	0	1	1.4500	1.4238	1.4310	1.4382	V
1	0	0	0	0	0	1.4625	1.4363	1.4435	1.4507	V
0	1	1	1	1	1	1.4750	1.4487	1.4560	1.4633	V
0	1	1	1	1	0	1.4875	1.4612	1.4685	1.4758	V
0	1	1	1	0	1	1.5000	1.4736	1.4810	1.4884	V
0	1	1	1	0	0	1.5125	1.4860	1.4935	1.5010	V
0	1	1	0	1	1	1.5250	1.4985	1.5060	1.5135	V
0	1	1	0	1	0	1.5375	1.5109	1.5185	1.5261	V
0	1	1	0	0	1	1.5500	1.5233	1.5310	1.5387	V
0	1	1	0	0	0	1.5625	1.5358	1.5435	1.5512	V
0	1	0	1	1	1	1.5750	1.5482	1.5560	1.5638	V
0	1	0	1	1	0	1.5875	1.5607	1.5685	1.5763	V
0	1	0	1	0	1	1.6000	1.5731	1.5810	1.5889	V

*VID Code is for reference only.
†V_{OUT} No Load is the input to the error amplifier.

ELECTRICAL CHARACTERISTICS (0°C < T_A < 70°C; V_{CC} = 12 V; C_{GATEx} = 100 pF, C_{COMP} = 0.01 μF, C_{SS} = 0.1 μF, C_{VCC} = 0.1 μF, R_{ROSC} = 95.3 kΩ, V(I_{LIM}) = 1.0 V, DAC Code 010100; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
VID Inputs					
Input Threshold	V_{ID5}, V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	400	600	800	mV
VID Pin Current	V_{ID5}, V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0} = 0 V	–	0.2	1.0	μA
SGND Bias Current	SGND < 300 mV, All DAC Codes	10	20	40	μA
SGND Voltage Compliance Range	–	−200	–	300	mV
Power Good					
Upper Threshold, Offset from No Load Set Point		85	97	115	mV
Lower Threshold Constant	PWRGDS/No Load Set Point	0.475	0.505	0.525	V/V
Output Low Voltage	V_{FFB} = 1.0 V, I_{PWRGD} = 4.0 mA	–	0.18	0.40	V
Delay	V_{FFB} high to PWRGD high	1.0	2.0	4.0	ms
Overvoltage Protection					
OVP Threshold above VID	–	170	215	250	mV
Enable Input					
Start Threshold	Gates switching, SS high	–	–	0.8	V
Stop Threshold	Gates not switching, SS low	0.4	–	–	V
Hysteresis	–	100	170	–	mV
Input Pull−Up Voltage	1.0 MΩ to GND	2.7	2.9	3.3	V
Input Pull−Up Resistance	–	7.0	10	20	kΩ
Error Amplifier					
V_{FB} Bias Current	–	–	0.1	1.0	μA
COMP Source Current	COMP = 0.5 V to 2.0 V	40	70	100	μA
COMP Sink Current	–	40	70	100	μA
Transconductance	(Note 2)	1.1	1.3	1.5	mmho
Open Loop DC Gain	(Note 2)	72	80	–	dB
Unity Gain Bandwidth	C_{COMP} = 30 pF (Note 2)	–	4.0	–	MHz
PSRR @ 1.0 kHz	(Note 2)	–	60	–	dB
COMP Max Voltage	V_{FB} = 0 V	2.4	2.9	–	V
COMP Min Voltage	V_{FB} = 1.6 V	–	80	150	mV
PWM Comparators					
Minimum Pulse Width	Measured from CSxP to GATEx, V_{FB} = CSxN = 0.5, COMP = 0.5 V, 60 mV step between CSxP and CSxN; Measure at GATEx = 1.0 V (Note 2)	–	40	100	ns
Transient Response Time	Measured from CSxN to GATEx, COMP = 2.1 V, CSxP = CSxN = 0.5 V, CSxN stepped from 1.2 V to 2.0 V (Note 2)	–	40	60	ns
Channel Startup Offset	CSxP = CSxN = V_{FB} = 0, Measure Vcomp when GATEx switch high	0.35	0.62	0.75	V
Artificial Ramp Amplitude	50% duty cycle	–	175	–	mV
MOSFET Driver Enable (DRVON)					
Output High	DRVON floating	2.3	–	–	V
Output Low	I = 100 μA	–	–	0.2	V
Pull−Down Resistance	DRVON = 1.5 V, ENABLE = 0 V, R = 1.5 V/I(DRVON)	35	70	140	kΩ
Source Current	DRVON = 1.5 V	0.5	3.0	6.5	mA

2. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; V_{CC} = 12 V; C_{GATEx} = 100 pF, C_{COMP} = 0.01 μF, C_{SS} = 0.1 μF, C_{VCC} = 0.1 μF, R_{ROSC} = 95.3 kΩ, V(I_{LIM}) = 1.0 V, DAC Code 010100; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
GATES					
High Voltage	Measure GATEx, I_{GATEx} = 1.0 mA	2.25	–	–	V
Low Voltage	Measure GATEx, I_{GATEx} = 1.0 mA	–	0.1	0.7	V
Rise Time GATE	0.8 V < GATEx < 2.0 V, V_{CC} = 10 V	–	5.0	10	ns
Fall Time GATE	2.0 V > GATEx > 0.8 V, V_{CC} = 10 V	–	5.0	10	ns
Oscillator					
Switching Frequency	R_{OSC} = 95.3 k, 3 Phase R_{OSC} = 95.3 k, 4 Phase	276 213	325 251	374 289	kHz
R_{OSC} Voltage	–	0.95	1.02	1.05	V
Phase Delay, 3 Phases	V_{CC} = CS4P = CS4N	100	120	140	deg
Phase Delay, 4 Phases	–	75	90	105	deg
Phase Disable Threshold	V_{CC} – (CS4P = CS4N)	500	–	–	mV
Adaptive Voltage Positioning					
V_{DRP} Output Voltage to DAC_{OUT} Offset	CSxP = CSxN, V_{FB} = COMP, Measure V_{DRP} – COMP	–20	0	+20	mV
Current Sense Amplifier to V_{DRP} Gain (each channel separately)	CSxP – CSxN = 80 mV, V_{FB} = COMP, Measure V_{DRP} – COMP for 25°C < T_A < 70°C	4.37	4.6	4.83	V/V
V_{DRP} Source Current	–	0.95	1.3	3.0	mA
V_{DRP} Sink Current	–	0.2	0.4	0.6	mA
Soft–Start					
Charge Current	–	30	44	50	μA
Discharge Current	–	90	120	160	μA
COMP Pull–Down Current	–	0.2	0.9	2.1	mA
Current Sensing and Overcurrent Protection					
CSxP Input Bias Current	CSxN = CSxP = 0 V	–	0.1	1.0	μA
CSxN Input Bias Current	CSxN = CSxP = 0 V	–	0.1	1.0	μA
Current Sense Amp to PWM Gain	CSxN = 0 V, CSxP = 80 mV, Measure V(COMP) when GATEx switches high	3.4	4.6	5.8	V/V
Current Sense Amp to PWM Bandwidth	(Note 2)	–	7.0	–	MHz
Current Sense Amp to I_{LIM} Gain	CSxP – CSxN = 20 mV to 60 mV, Ramp I_{LIM} until SS goes low	3.228	3.390	3.526	V/V
Current Sense Amp to I_{LIM} Bandwidth	(Note 2)	–	1.0	–	MHz
Current Limit Filter Slew Rate	(Note 2)	2.0	5.0	13	mV/μs
I_{LIM} Input Bias Current	I_{LIM} = 0 V	–	0.1	1.0	μA
Current Sense Amp to I_{LIM} Output Offset	T = 80°C	–82	–12	58	mV
Current Sense Common Mode Input Range	(Note 2)	0	–	2.0	V
General Electrical Specifications					
V_{CC} Operating Current	COMP = 0.3 V (no switching)	–	27	35	mA
UVLO Start Threshold	SS charging, GATEx switching	8.5	9.0	9.5	V
UVLO Stop Threshold	GATEx not switching, SS and COMP discharging	7.5	8.0	8.5	V
UVLO Hysteresis	Start – Stop	0.8	1.0	1.2	V

2. Guaranteed by design, not tested in production.

PIN DESCRIPTION

Pin No.	Pin Symbol	Pin Name	Description
1−3, 30−32	V_{ID0}−V_{ID5}	DAC VID Inputs	VID−compatible logic input used to program the converter output voltage. All high on V_{ID0}−V_{ID4} generates fault.
4	PWRLS	Power Good Sense	Voltage sensing pin for Power Good lower threshold.
5	V_{FFB}	Fast Voltage Feedback	Input of PWM comparator for fast voltage feedback, and also the inputs of Power Good sense and overvoltage protection comparators
6	SS	Soft−Start	A capacitor between this pin and ground programs the soft−start time.
7	PWRGD	Power Good Output	Open collector output goes high when the converter output is in regulation.
8	DRVON	Drive ON	Logic high enables MOSFET drivers, and logic low turns all MOSFETs off through MOSFET drivers. Pulled to ground through internal 70 k resistor.
9	SGND	Remote Sense Ground	Ground connection for DAC and error amplifier. Provides remote sensing of load ground.
10	V_{DRP}	Output of Current Sense Amplifiers for Adaptive Voltage Positioning	The offset above DAC voltage is proportional to the sum of inductor current. A resistor from this pin to V_{FB} programs the amount of Adaptive Voltage Positioning. Leave this pin open for no Adaptive Voltage Positioning.
11	V_{FB}	Voltage Feedback	Error amplifier inverting input.
12	COMP	Error Amp Output	Provides loop compensation and is clamped by SS during soft−start and fault conditions. It is also the inverting input of PWM comparators.
13	CS4N	Current Sense Reference	Inverting input to current sense amplifier #4.
14	CS4P	Current Sense Input	Non−inverting input to current sense amplifier #4.
15	CS3N	Current Sense Reference	Inverting input to current sense amplifier #3, and Phase 3 disable pin.
16	CS3P	Current Sense Input	Non−inverting input to current sense amplifier #3, and Phase 3 disable pin.
17	GND	Ground	IC power supply return. Connected to IC substrate.
18−21	GATE4−GATE1	Channel Outputs	PWM outputs to drive MOSFET driver ICs.
22	V_{CC}	IC Power Supply	Power Supply Input for IC.
23	R_{OSC}	Oscillator Frequency Adjust	Resistor to ground programs the oscillator frequency.
24	I_{LIM}	Total Current Limit	Resistor divider between R_{OSC} and ground programs the over current limit.
25	CS1P	Current Sense Input	Non−inverting input to current sense amplifier #1.
26	CS1N	Current Sense Reference	Inverting input to current sense amplifier #1.
27	CS2P	Current Sense Input	Non−inverting input to current sense amplifier #2.
28	CS2N	Current Sense Reference	Inverting input to current sense amplifier #2.
29	ENABLE	Enable	A voltage less than the threshold puts the IC in Fault Mode, discharging SS. Connect to system VID_{PWRGD} signal to control powerup sequencing. Hysteresis is provided to prevent chatter.

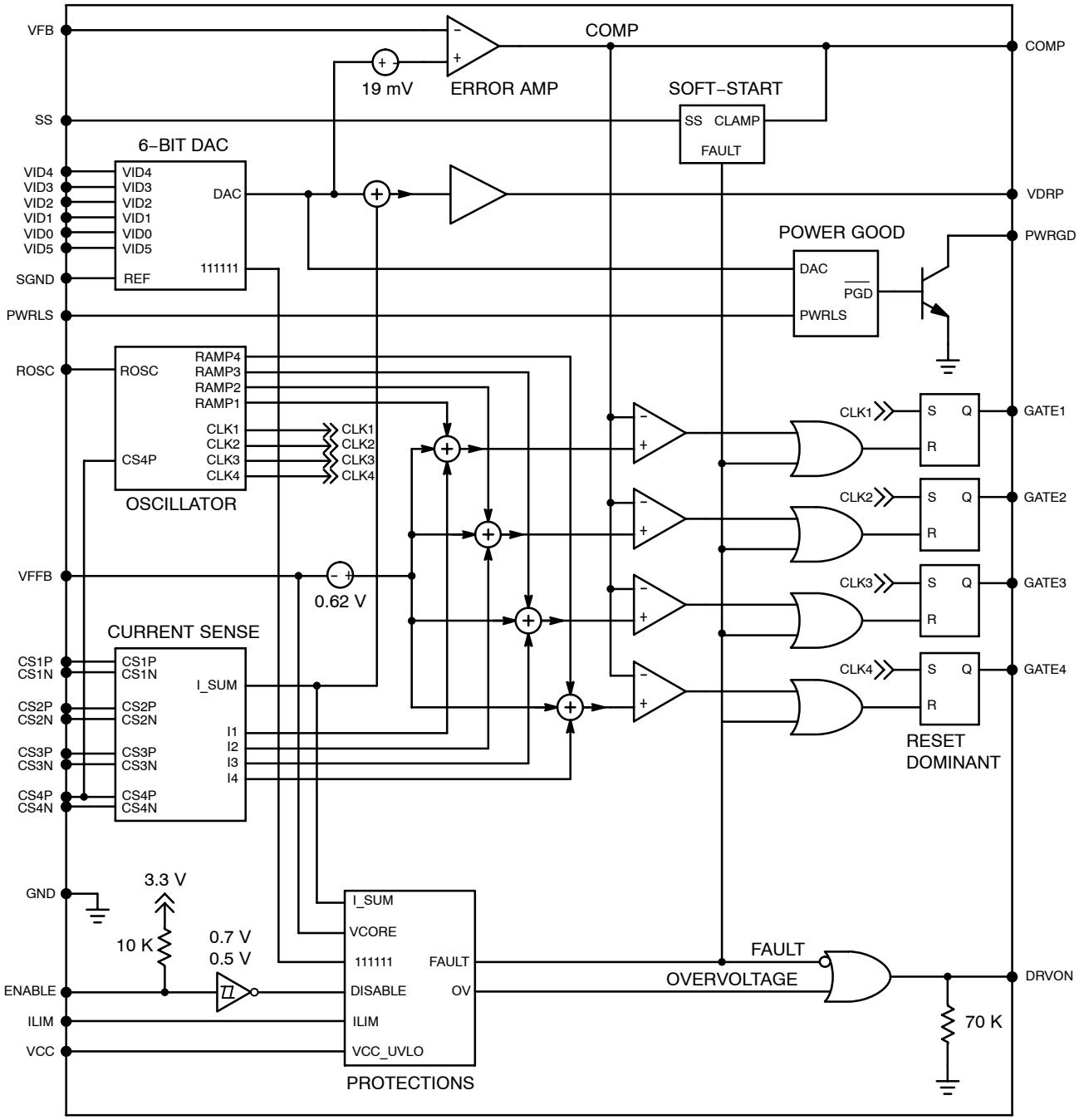


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

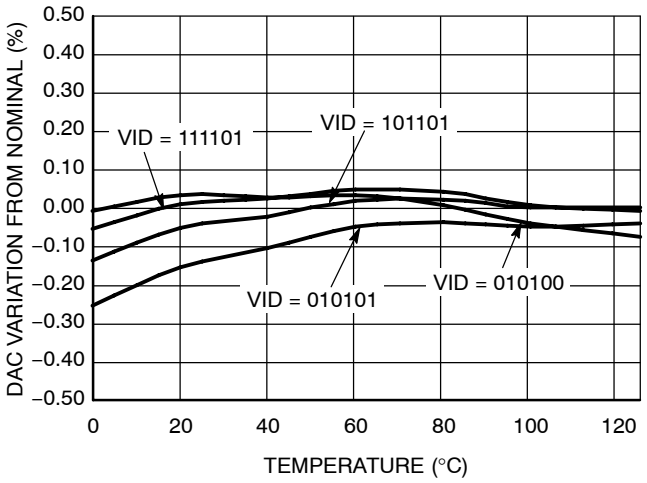


Figure 3. DAC Variation versus Temperature

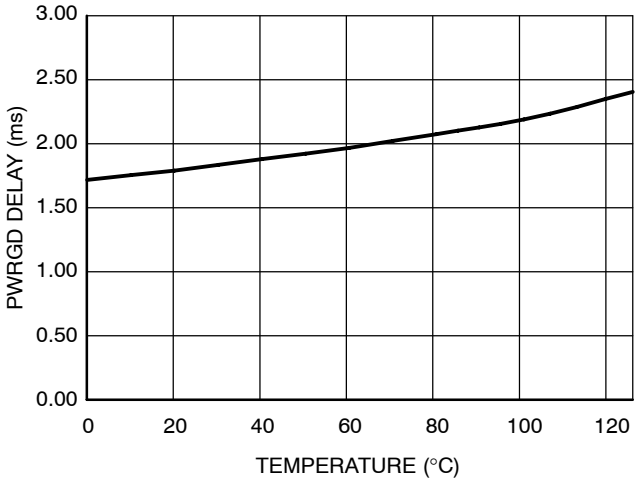


Figure 4. Power Good Delay versus Temperature

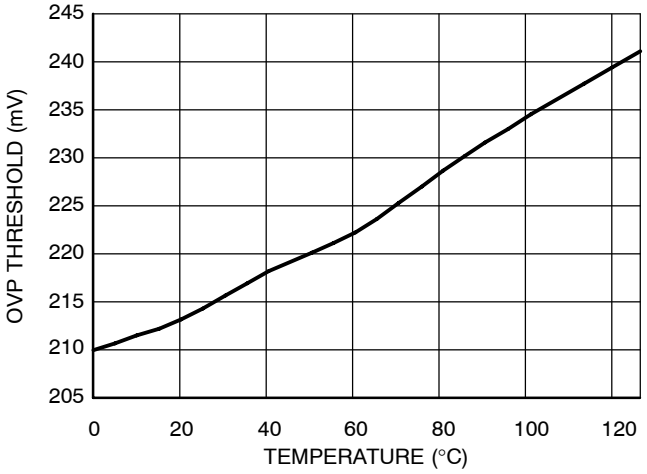


Figure 5. OVP Threshold above VID versus Temperature

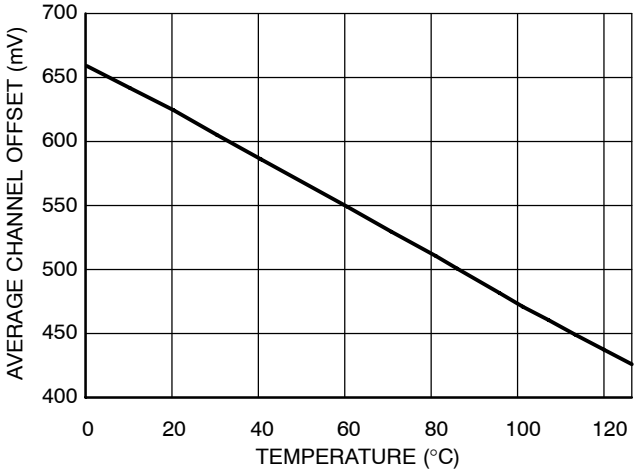


Figure 6. Channel Startup Offset versus Temperature

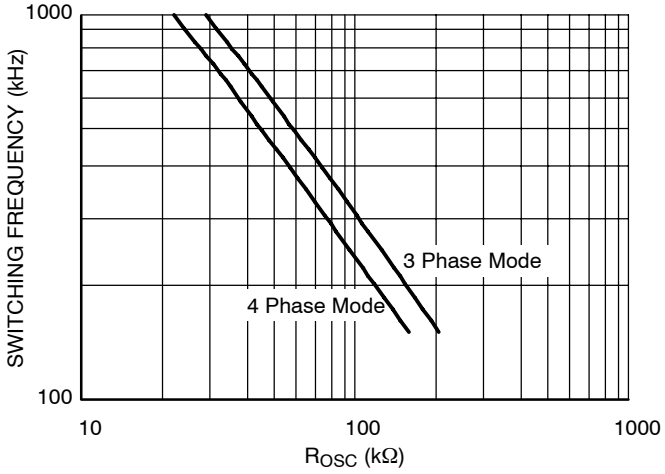


Figure 7. Oscillator Frequency versus Total R_{OSC} Value

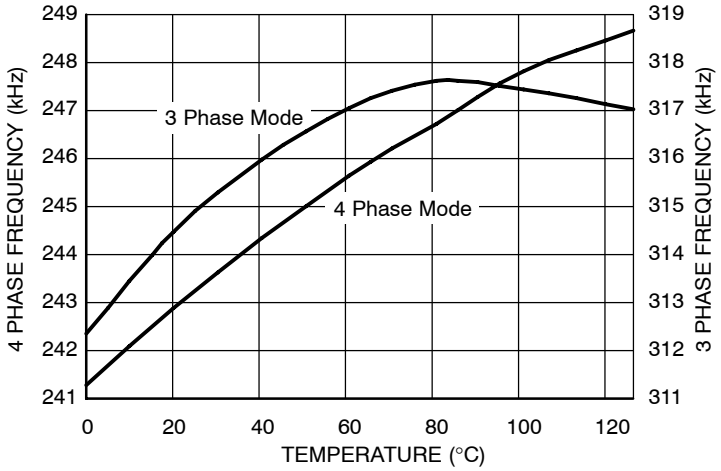


Figure 8. Switching Frequency versus Temperature (R_{OSC} = 95.3 kΩ)

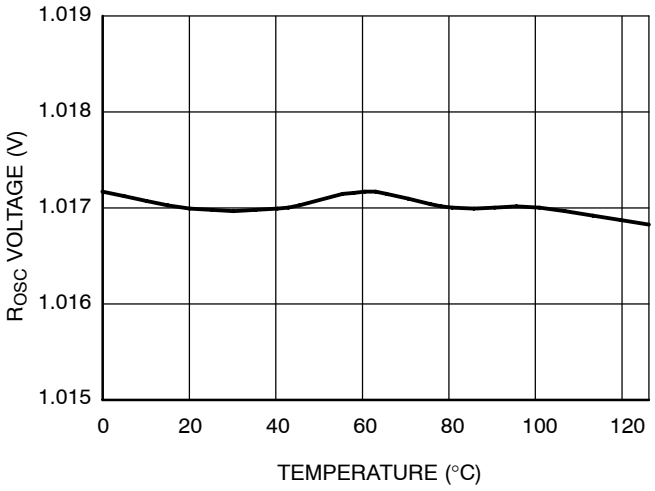


Figure 9. V_{ROSC} versus Temperature

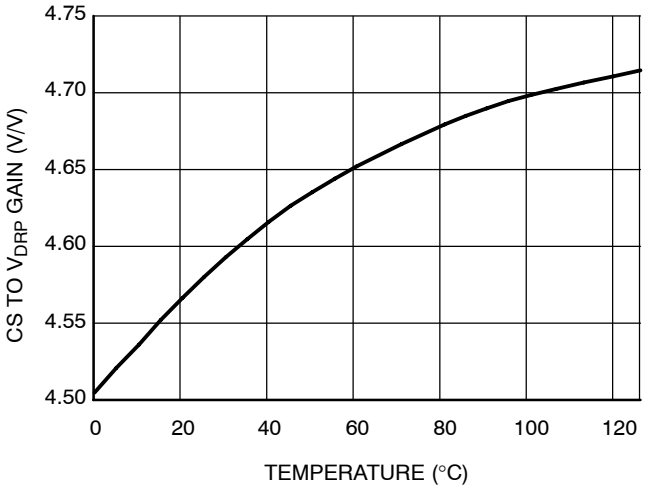


Figure 10. Current Sense to V_{DRP} Gain versus Temperature

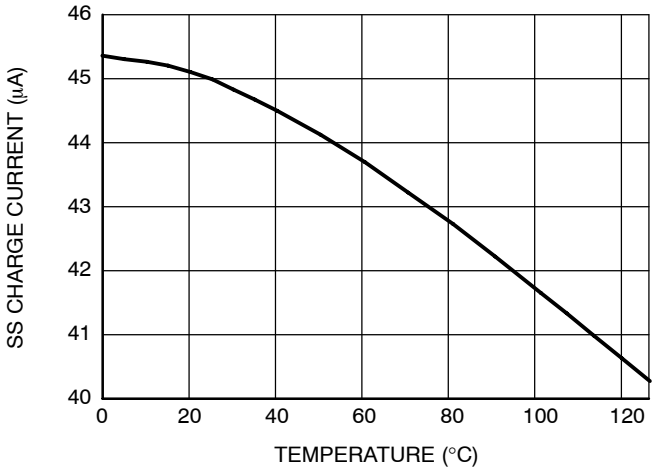


Figure 11. Soft−start Charge Current versus Temperature

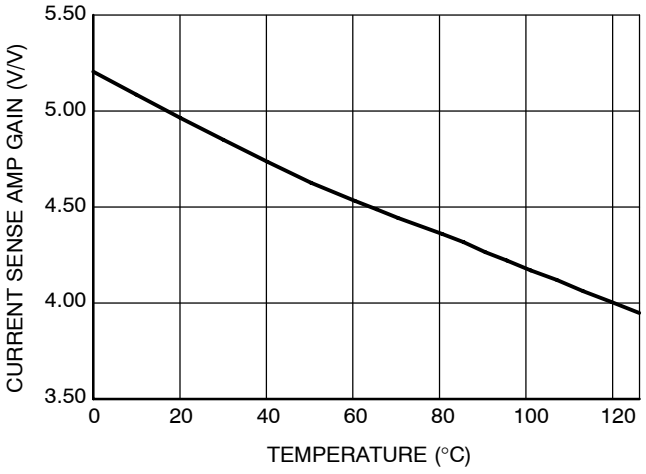


Figure 12. Current Sense Amplifier to PWM Gain versus Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

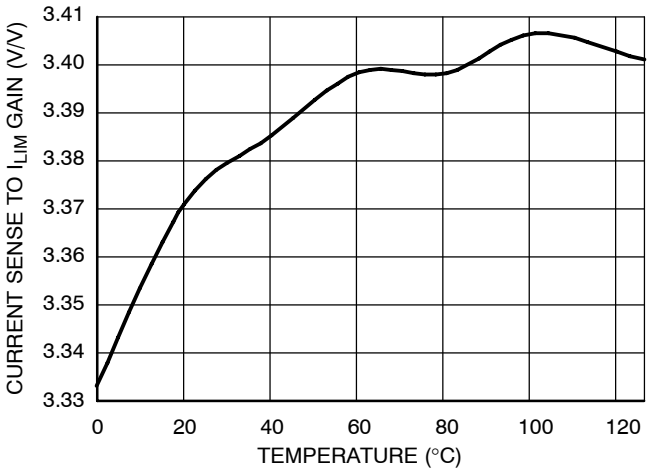


Figure 13. CS Amp to I_{LIM} Gain versus Temperature

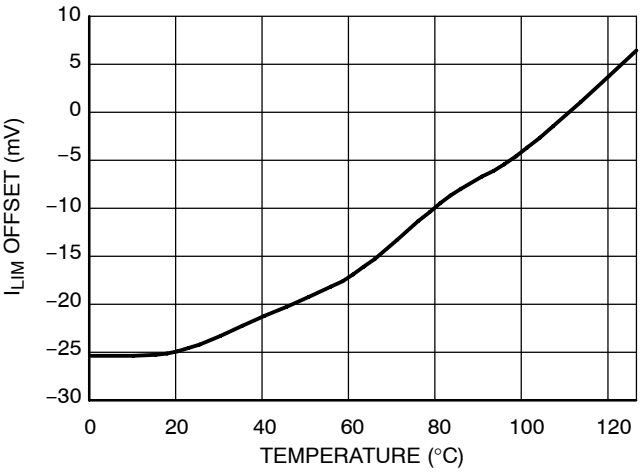


Figure 14. I_{LIM} Offset versus Temperature

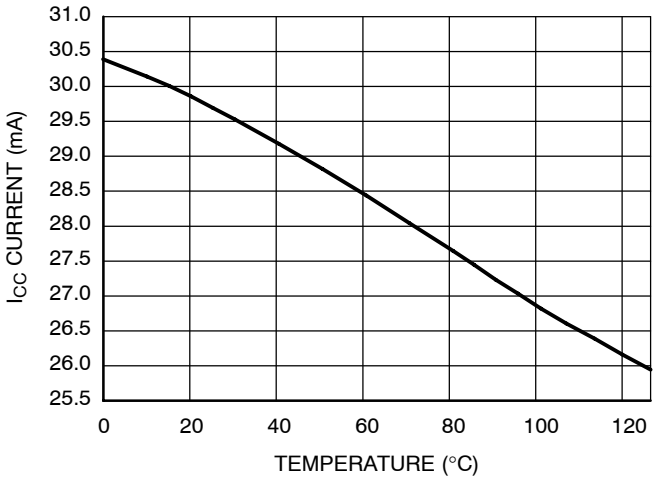


Figure 15. V_{CC} Operating Current versus Temperature

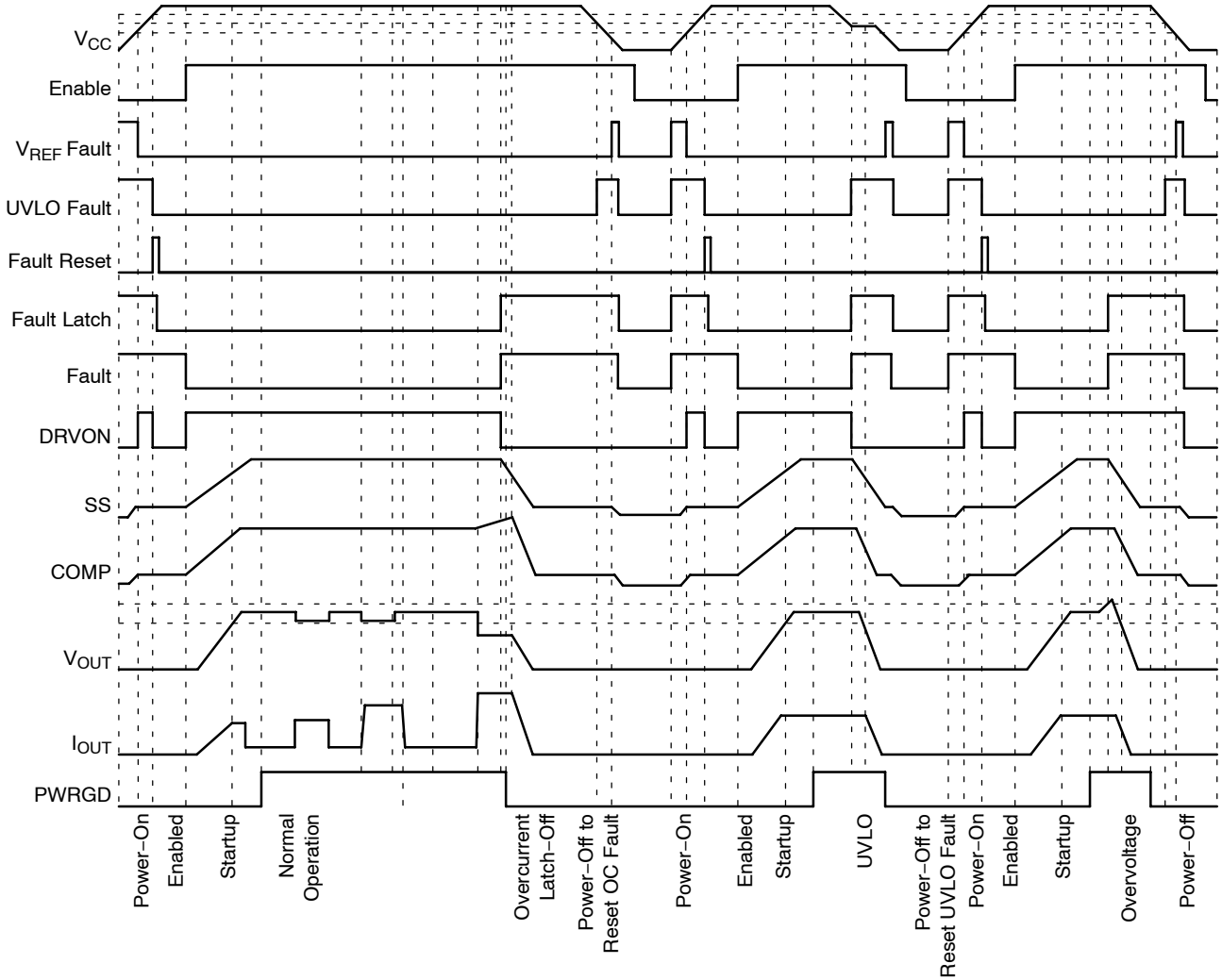


Figure 16. Operating Waveforms

APPLICATIONS INFORMATION

Overview

The NCP5318 is a multiphase, synchronous buck controller using the Enhanced V^2 topology which combines the fast transient response of the original V^2 topology with the load current sharing characteristic of peak current−mode control. The NCP5318 can be operated as an interleaved two/three/four−phase controller. Differential current sensing is incorporated in order to more easily achieve effective current sharing. Converter output is regulated to a voltage corresponding to the logic states at six digital inputs. The NCP5318 incorporates a Power Good (PWRGD) function, providing integrated fault monitoring and sequencing that simplifies design, minimizes circuit board area, and reduces overall system cost.

Fixed Frequency Multi−Phase Control

In a multi−phase buck converter, multiple, synchronously rectified, buck power stages are connected in parallel and are energized at a common frequency but with staggered phasing (interleaving). Each stage carries only part of the total output current. In four−phase mode, each phase oscillator is delayed 360/4 – or 90 – degrees from that of the previous phase. Likewise, for other phase counts, each phase oscillator is delayed 360/N degrees from that of the previous phase, where N is the number of phases.

Advantages of a multiphase converter over a single−phase converter include a better heat distribution and decreased input and output ripple currents. Breaking up heat into a greater number of smaller amounts, reduces PC Board thermal stress. Multiple phases also permits phase inductance to be higher than used in a single−phase converter capable of equal transient response, with correspondingly lower phase ripple current and I^2R losses. In addition to the higher efficiency, input capacitor current appears even lower because of the cancellation achieved by the summation of individual, phase shifted, ripple currents. This often allows the use of fewer input capacitors without exceeding the capacitor RMS current rating. Also due to the decrease in phase ripple current, output di/dt change from positive to negative during switching is reduced. This reduction of output di/dt change decreases the output capacitor ESL component of output ripple voltage − often allowing a reduction in the number of ceramic output capacitors.

Because the inductors are always connected between the output and some low impedance (either the input supply or ground), the effective inductance value seen at the output is the value of all inductors connected in parallel (the value of a single inductor divided by the number of phases). Multiphase output current ramp−up (+di/dt) or ramp−down (−di/dt) exhibits finer granularity due to the summation of the smaller individual phase di/dt produced by the larger individual inductors. Within one switching cycle, however, total converter di/dt can sum to the same di/dt as a power stage with a single inductor of the same effective value.

Enhanced V^2 Control

Enhanced V^2 control measures and adjusts the output current in each phase while simultaneously adjusting the current of all phases to maintain the correct output voltage. Enhanced V^2 responds to output voltage disturbances by the combined effect of two mechanisms. The first mechanism includes the response of the Error Amplifier, and is responsible for maintaining the DC accuracy of the output voltage setting. Depending on the frequency compensation set by the amplifier's external components, the Error Amplifier response begins to change the PWM duty cycle within one to two cycles. The second mechanism is the direct coupling of converter output voltage to all non−inverting PWM comparator inputs, which dominates PWM response at frequencies above the unity−gain crossover frequency of the compensated Error Amplifier. A rapid increase in load current that decreases converter output voltage immediately extends the duty cycle of any phase already on, and will typically increase the duty cycle of several of the following phases for one cycle.

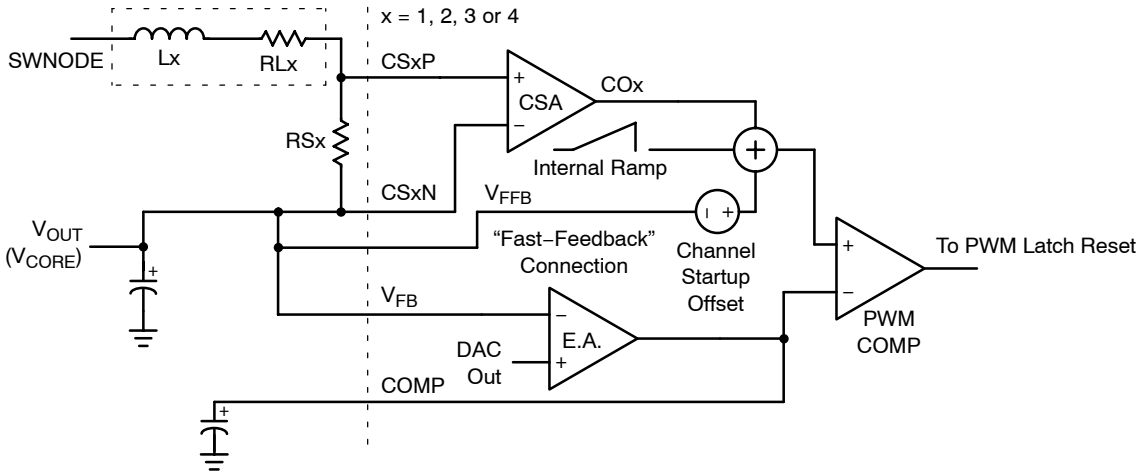


Figure 17. Enhanced V^2 Control Employing Resistive Current Sensing and Internal Ramp

The NCP5318 provides a differential input (CSxN and CSxP) that accepts inductor current information for each phase as shown in Figure 17. The triangular inductor current is measured across R_S and amplified before being summed with the channel startup offset, the internal ramp and the output voltage. The internal ramp provides greater design flexibility by allowing smaller external (current) ramps, lower minimum pulse widths, higher frequency operation and PWM duty cycles above 50% without external slope compensation.

When the controller is enabled, GATEx output (GATE output of any phase) transitions to a high voltage at the start of the oscillator cycle for that phase, commanding a power stage to switch on. Inductor current in that power stage then ramps up until the combination of startup offset voltage, its current sense signal, its internal ramp and the output voltage ripple exceed the compensated feedback signal at the other PWM comparator input. This brings GATEx low, which commands that power stage off. While GATEx is high, the Enhanced V^2 control circuit will respond to line and load variations, but once GATEx is low, that phase cannot respond until the next start of its oscillator cycle. Therefore, the NCP5318 will take, at most, the off−time of the oscillator to respond to disturbances. With multiple phases, the time to respond to disturbances is significantly reduced due to the increased likelihood of a GATEx being high, and closer average proximity of oscillator starts, however the magnitude of that response (for equivalent total inductance) is equivalently reduced.

Turn on of a phase with higher inductor current will terminate the PWM cycle earlier, providing negative feedback. Current sharing is accomplished by referencing the PWM comparators of all phases to the same Error Amplifier signal (COMP pin).

Error Amplifier Output (COMP) Voltage No Load Bias Point

As shown in Figure 17, the voltage present at each PWM comparator's non−inverting input is the sum of the channel startup offset, output voltage, and the inductor current and internal ramps corresponding to that phase. When the average output current is zero, the Error Amplifier output at the COMP pin will be:

$$V_{COMP} = V_{OUT} + Channel\_Startup\_Offset + Int\_Ramp + G_{CSA} \times \frac{Ext\_Ramp}{2}$$

Int_Ramp is the fraction of the internal ramp ("Artificial Ramp Amplitude" = 100 mV at a 50% duty cycle) corresponding to the steady state duty cycle, Ext_Ramp is the peak−to−peak external steady−state current ramp appearing across CSxP to CSxN, G_{CSA} is the current sense amplifier gain ("Current Sense Amp to PWM Gain" = 3.0 V/V).

When the technique known as "lossless inductor current sensing" is used as in Figure 19, the magnitude of Ext_Ramp is:

$$Ext\_Ramp = D \times (V_{IN} - V_{OUT})/(R_{CSx} \times C_{CSx} \cdot f_{SW})$$

where D is duty cycle expressed as a fraction.

For example, if V_{OUT} at zero load is set to 1.480 volts and the input voltage V_{IN} is 12.0 V, the duty cycle (D) will be 1.480/12.0 or 12.3%. Int_Ramp will be 100 mV/50% x 12.3% = 25 mV. Realistic values for R_{CSx}, C_{CSx} and f_{SW} are 2.5 kΩ, 0.1 μF and 350 kHz. Using these and the previously mentioned formula, Ext_Ramp will be 14.8 mV.

$$V_{COMP} = 1.480\ V + 0.60\ V + 25\ mV + \frac{3.0\ V}{V} \times \frac{14.8\ mV}{2} = 2.127\ Vdc.$$

Error Amplifier Output (COMP) Voltage Bias Point Change with Load

In a closed loop configuration, the COMP pin may move in order to maintain the output voltage constant when load current changes. The required change at the COMP pin depends partially on the scaling of the current feedback signal as follows:

$$\Delta V = R_S \times G_{CSA} \times \frac{\Delta I_{OUT}}{N}$$

where R_S is the current sense resistance in each phase and N is the number of phases.

Also, when load current changes, nonideal conversion efficiency causes the change in input power to exceed the change in output power, and the duty cycle becomes:

$$D' = \frac{D}{Efficiency}$$

and

$$\Delta D = D' - D = \frac{D}{Efficiency} - \frac{(D \times Efficiency)}{Efficiency} = \frac{D \times (1 - Efficiency)}{Efficiency}$$

Peak to peak ripple current therefore also changes by nearly (1− Efficiency) / Efficiency, thereby changing the amplitude of the external ramp by this amount. The complete change required at the COMP pin will therefore be:

$$\Delta V = R_S \times G_{CSA} \times \frac{\Delta I_{OUT}}{N} + \frac{(Int\_Ramp + G_{CSA} \times Ext\_Ramp)}{2} \times \frac{(1 - Efficiency)}{Efficiency}$$

For the converter described above with 4 phases and 85% efficiency at 100 A full load, the Error Amplifier output changes by:

$$\Delta V_{COMP} = 1.0\ m\Omega \times \frac{3.0\ V}{V} \times \frac{100\ A}{4} + \frac{(25\ mV + 3.0\ V/V \times 14.8\ mV)}{2} \times \frac{(1 - 0.85)}{0.85}$$

$$= 83\ mV$$

Additionally, if the “Droop” feature is used, the output voltage change resulting from the synthesized, closed loop output impedance (referred to as the output loadline) is as follows:

$$\Delta V = - R_{LL} \times \Delta I_{OUT}$$

where R_{LL} is the value, in ohms, of the output loadline. Summation of this change at the PWM comparator input forces the Error Amplifier output voltage to respond with an identical change which always opposes that forced by the sensed current previously described, which reduces the amount of Error Amplifier output movement required.

Figure 18 shows the open loop response of the PWM comparator and resulting phase current upon an output voltage dip. Before T1, the converter is in steady−state operation. The inductor current provides a portion of the PWM ramp through the current sense amplifier. The PWM cycle ends when the sum of the current ramp, the “partial” internal ramp, the offset and the output voltage exceeds the level of the COMP pin. At T1, the load current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than before until T2, when the current signal has increased enough to make up for the lower voltage at the VFB pin. After T2, the output voltage remains lower, and the average current signal level (CSA output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system, the COMP pin would move higher to restore the output voltage to the original level.

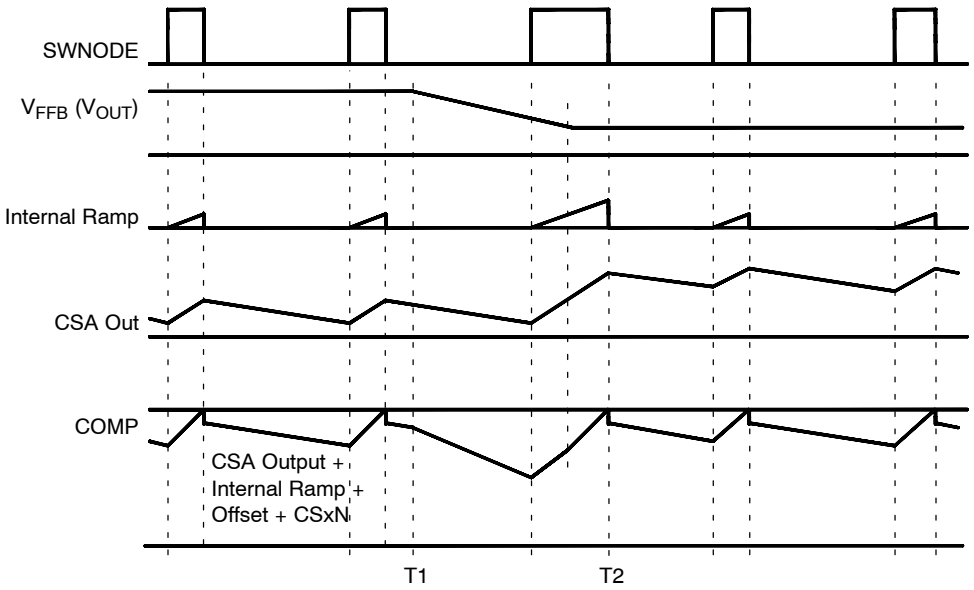


Figure 18. Open Loop Operation

Inductive Current Sensing

For lossless sensing, current can be measured across the inductor as shown in Figure 19. In the diagram, L is the output inductance and R_L is the inherent inductor resistance. To compensate the current sense signal, the values of R_{CSx} and C_{CSx} are chosen so that $L/R_L = R_{CSx} \times C_{CSx}$. If this criteria is met, the current sense signal should be the same shape as the inductor current and the voltage signal between CSxP and CSxN will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value R_L was used. When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of 0.39% per degree C. The increase in winding resistance at higher temperatures should be considered when setting the phase peak current limit threshold. If current sensing more accurate than provided by inductive sensing is required, current can be sensed through a resistor as shown in Figure 17.

Current Sharing Accuracy

For accurate current sharing, the current sense inputs should sense the current at identical points at each phase sense resistance. Printed Circuit Board (PCB) traces that carry inductor current can be used as part of the current sense resistance by selecting where the current sense signal is picked up along a current carrying trace, but variations of PCB copper base thickness, plating, and etching can degrade current sharing and must be well controlled. The total current sense resistance used for calculations must include any PCB trace resistance that carries inductor current between the CSxP input and the CSxN input. Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case CSA input mismatch is ±4 mV and will typically be within 1.5 mV. The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance, a 1.5 mV mismatch with a 1.0 mΩ sense resistance will contribute 1.5 A of current difference between phases.

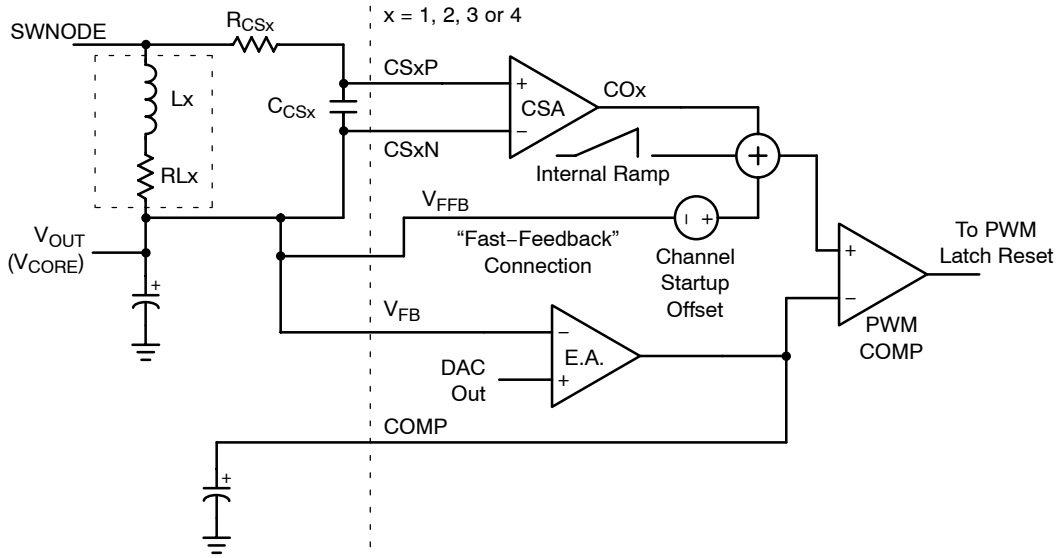


Figure 19. Enhanced V^2 Control Employing Lossless Inductive Current Sensing and Internal Ramp

External Ramp Size and Current Sensing

The internal ramp allows flexibility in setting the current sense time constant. Typically, the current sense $R_{CSx} \times C_{CSx}$ time constant should be equal to or slightly slower than the inductor's time constant. If RC is chosen to be smaller (faster) than L/R_L, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady−state ramp, but transient circuit response will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $R_{CSx} \times C_{CSx}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $R_{CSx} \times C_{CSx}$. Excessive error can degrade transient response, adaptive positioning (droop) and current limit. During a positive current transient, the COMP pin will be required to overshoot in response to the current signal in order to maintain the output voltage. Phase pulse−by−pulse overcurrent protection will trip earlier than it would if compensated correctly. Similarly, the V_{DRP} signal will overshoot which will produce too much transient droop in the output voltage, and also result in hiccup−mode current limit having a lower threshold for fast rising step loads than for slowly rising output currents.

Transient Response and Adaptive Voltage Positioning

For applications with fast transient currents, the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. In addition, adaptive voltage positioning can reduce peak−peak output voltage deviations due to load transients and allow use of a smaller output filter. Adaptive voltage positioning sets output voltage higher than nominal at light loads, and output voltage is allowed limited sag when the load current is applied. Upon removal of the load, output voltage returns no higher than the original level, allowing one output transient peak to be canceled over a load application and release cycle.

For low current applications, a simple dropping resistor in series with the output can provide fast, accurate adaptive positioning. However, at high currents, the loss in a dropping resistor becomes excessive. For example, a 50 A converter with a 1.0 mΩ resistor would provide a 50 mV change in output voltage between no load and full load and would dissipate 2.5 W. Lossless Adaptive Voltage Positioning (AVP) is an alternative to using a droop resistor. Figure 20 shows how AVP works. The waveform labeled “normal” shows a converter without AVP.

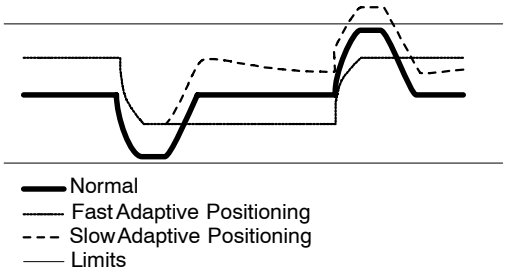


Figure 20. Adaptive Voltage Positioning

On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) AVP, the peak−to−peak excursions are cut in half. In the slow AVP waveform, the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded. The controller can be configured to adjust the output voltage based on the output current of the converter as shown in the application diagram in Figure 1. The no−load positioning is set internally to VID − 19 mV, reducing the potential error due to resistor and bias current mismatches. In order to realize the AVP function, a resistor divider network is connected between V_{FB}, V_{DRP} and V_{OUT}. During no−load conditions, the V_{DRP} pin is at the same voltage as the V_{FB} pin. As the output current increases, the V_{DRP} pin voltage increases proportionally. This drives the V_{FB} voltage higher, causing V_{OUT} to “droop” according to a loadline set by the resistor divider network. The response during the first few microseconds of a load transient is controlled primarily by power stage output impedance, and by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow, there will be a long transition to the final voltage after a transient. This will be most apparent with low capacitance output filters.

Overvoltage Protection

Overvoltage Protection (OVP) in the Enhanced V^2 control topology is provided by operation of the synchronous rectifiers. The control loop responds to an overvoltage condition within 40 ns, causing the GATEx output to shut off. The (external) MOSFET driver should react normally to turn off the top MOSFET and turn on the bottom MOSFET. This acts quickly to discharge the output voltage and prevent damage to the load. The regulator will remain in this state until the fault latch is reset by cycling power at the V_{CC} pin. If the voltage at the V_{FFB} pin exceeds 200 mV above the VID voltage, the converter will latch off.

The OVP circuit begins monitoring the output voltage as soon as the V_{CC} voltage exceeds the UVLO threshold of the part. The OVP circuit is then always active, regardless of operating status.

Power Good

According to the latest specifications, the Power Good (PWRGD) signal must be asserted when the output voltage is within a window defined by the VID code, as shown in Figure 21. The PWRLS pin is provided to allow the PWRGD comparators to accurately sense the output voltage. The effect of the PWRGD lower threshold can be modified using a resistor divider from the output to PWRLS to ground, as shown in Figure 22.

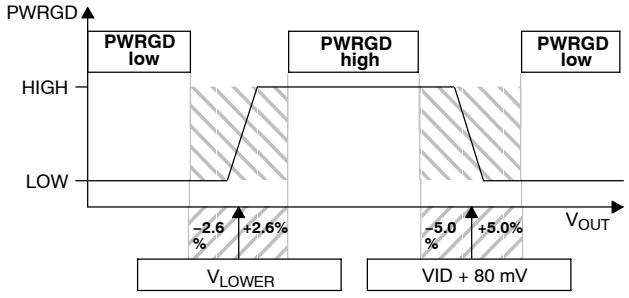


Figure 21. PWRGD Assertion Window

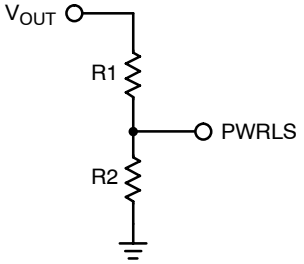


Figure 22. Adjusting the PWRGD Threshold

Since the internally−set thresholds for PWRLS are $V_{OUTNo\ Load}$ /2 for the lower threshold and $V_{OUT\ No\ Load}$ + 100 mV for the upper threshold, a simple equation can be provided to assist the designer in selecting a resistor divider to provide the desired PWRGD performance.

$$V_{LOWER} = \frac{V_{OUTNoLoad}}{2} \times \frac{R_1 + R_2}{R_2}$$

$$V_{UPPER} = V_{OUTNoLoad} + 100\ mV$$

The logic circuitry inside the chip sets PWRGD low only after a delay period has been passed. A “power bad” event does not cause PWRGD to go low unless it is sustained through the delay time of 1 ms. If the anomaly disappears before the end of the delay, the PWRGD output will never be set low. In order to use the PWRGD pin as specified, the user is advised to connect external resistors as necessary to limit the current into this pin to 4.0 mA or less.

Undervoltage Lockout

The NCP5318 includes an undervoltage lockout circuit. This circuit keeps the IC’s output drivers low until V_{CC} applied to the IC reaches 9.0 V. The GATE outputs are disabled when V_{CC} drops below 8.0 V.

Soft−Start

At initial power−up, both SS and COMP voltages are zero. The total SS capacitance will begin to charge with a current of 70 μA. The error amplifier directly charges the COMP capacitance. An internal clamp ensures that the COMP pin voltage will always be less than the voltage at the SS pin, ensuring proper startup behavior. All GATE outputs are held low until the COMP voltage reaches 0.6 V. Once this threshold is reached, the GATE outputs are released to operate normally.

Current Limit

The individual phase currents are summed to compare a total current signal to a user adjustable voltage on the I_{LIM} pin. If the I_{LIM} voltage is exceeded, the fault latch trips and the converter is latched off. V_{CC} must be recycled to reset the latch.

Fault Protection Logic

The NCP5318 includes fault protection circuitry to prevent harmful modes of operation from occurring. The fault logic is described in Table 1.

Gate Outputs

The NCP5318 is designed to operate with external gate drivers. Accordingly, the gate outputs are capable of driving a 100 pF load with typical rise and fall times of 5.0 ns.

An additional signal, DRVON, works in conjunction with the Gate Outputs. The DRVON signal is intended to be used as an enable signal for external gate drivers, such as the NCP3418B. If the DRVON signal is low, the gate driver will be disabled and both MOSFETs in the synchronous rectified phase channel will be held in the off position. If the DRVON signal is high, the gate driver will be enabled. The high side MOSFET will be enabled if the Gate Output is high and DRVON is high. The low side MOSFET will be enabled if the Gate Output is low and DRVON is high. The DRVON signal at power up will initially go high as V_{CC} rises above the power on reset (POR) of the IC, roughly 5 V. It will stay high until the V_{CC} voltage exceeds the UVLO threshold of the part. DRVON will then go to a low state and stay low until the part is enabled or an OVP is detected.

Digital to Analog Converter (DAC)

The output voltage of the NCP5318 is set by means of a 6−bit, 0.5% DAC. The VID pins must be pulled high externally. A 1.0 kΩ pullup to a maximum of 3.3 V is recommended to meet Intel specifications. To ensure valid logic signals, the designer should ensure at least 800 mV will be present at the IC for a logic high. The output of the DAC is described in the Electrical Characteristics section of the data sheet. These outputs are consistent with VR 10.x and processor specifications. The DAC output is equal to the VID code specification minus 19 mV. The latest VR and processor specifications require a power supply to turn its output off in the event of a 11111X VID code. When the DAC sees such a code, the GATE pins stop switching and go low. This condition is described in Table 1.

Table 1. Description of Fault Logic

	Results				
Faults	Stop Switching	PWRGD Level	Driver Enable	SS Character-istics	Reset Method
Overvoltage Lockout	Yes		High	−0.3 mA	Power On
Enable Low	Yes	Depends on output voltage level	Low	−0.3 mA	Not Affected
Module Overcurrent Limit	Yes	Depends on output voltage level	Low	−0.3 mA	Power On
DAC Code = 11111x	Yes	Depends on output voltage level	Low	−0.3 mA	Change VID Code
V_{REF} Undervoltage Lockout	Yes	Depends on output voltage level	Low	−0.3 mA	Power On
PWRLS Out of Range	No	Low	High	Not Affected	Not Affected

Adjusting the Number of Phases

The NCP5318 is designed with a selectable−phase architecture. Designers may choose any number of phases up to four. The phase delay is automatically adjusted to match the number of phases that will be used. This feature allows the designer to select the number of phases required for a particular application.

Four−phase operation is standard. All phases switch with a 90 degree delay between pulses. No special connections are required. Three−phase operation is achieved by disabling phase 4. Tie together CS4N and CS4P, and then pull both pins to V_{CC}. The remaining phases will continue to switch, but now there will be a 120 degree delay between phases. The phase firing order will become 1−2−3.

Two− and single−phase operation may be realized as well. First, the designer must choose the proper phases. Two phase operation must use phases 2 and 4 by tying CS1N, CS1P, CS3N and CS3P to ground. This will then use phases 2 and 4 to control gate drivers. The other gate control outputs may switch, so leave them unconnected.

Single phase is best accomplished by using only Phase 2 as the switch controller. Connect CS2P and CS2N pins to the current sense circuit, and gate control output 2 to the gate driver IC input. Tie all other CSxx pins together and connect them to ground.

Design Procedure

1. Setting the Switching Frequency

The total resistance from R_{OSC} to ground sets the operating frequency for all phases of the converter. The frequency can be set for either the three phase or four phase mode by using Figure 7, “Oscillator Frequency versus Total R_{OSC} Value”. After choosing the desired operating frequency and the number of phases, use the figure to determine the necessary resistance. If two phase operation is desired, use the value given for four phase operation.

The voltage from R_{OSC} is closely regulated at 1.0 V. This voltage can be used as the reference for the overcurrent limit set point on the I_{LIM} pin. Design a voltage divider with the appropriate division ratio to give the desired I_{LIM} voltage and total resistance to set the operating frequency. Since loading by the I_{LIM} pin is very small, the frequency selection will not be affected.

2. Output Capacitor Selection

The output capacitors filter the current from the output inductors and provide a low impedance for transient load current changes. Typically, microprocessor applications require both bulk (polymer, aluminum, or tantalum electrolytic) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide “hold up” during transient loading until phase currents ramp up or down. The low impedance capacitors reduce steady−state ripple voltage and bypass the bulk capacitance for fast output current changes.

The designer must determine the number of bulk capacitors so as to meet the peak transient requirements. The formula below can be used to provide a starting point for the minimum number of bulk capacitors ($NB_{OUT,MIN}$):

$$NB_{OUT,MIN} = \text{ESR per capacitor} \times \frac{\Delta I_{O,MAX}}{\Delta V_{O,MAX}} \quad \text{(eq. 1)}$$

The ESL of the bulk plus ceramic capacitors also affects the voltage change during a load transient according to:

$$\Delta V_{O,MAX} = \left(\frac{\Delta I_{O,MAX}}{\Delta t}\right) \times ESL + \Delta I_{O,MAX} \times \frac{ESR}{NB_{OUT,MIN}} \quad \text{(eq. 2)}$$

where ESL is the equivalent ESL of all bulk and ceramic output capacitors in parallel. Capacitor manufacturers do not always specify the ESL of their components and it is affected by the inductance added by the PCB layout. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk and ceramic capacitors and perform transient testing to determine the final number of bulk capacitors.

Intel processor specifications discuss “DynamicVID” (DVID), by which the VID codes are stepped up or down to a new desired output voltage. Timing requirements for when the output must be in regulation further complicates output capacitor selection. The ideal output capacitor selection has low ESR and low capacitance. Too much output capacitance will make it difficult to meet DVID timing specifications; too much ESR will complicate the transient solution. The Sanyo 4SEPC560 and Panasonic EEU−FL provide a good balance of capacitance vs. ESR.

Microprocessor manufacturers often specify a minimum number of ceramic capacitors, which may need adjustment to meet ripple voltage requirements. The output voltage ripple can be calculated using the output inductor value derived in the following section ($L_{O,MIN}$) and the number of bulk output capacitors ($NB_{OUT,MIN}$) determined above:

$$V_{OUT,P-P} = (ESR\,per\,bulk\,cap./NB_{OUT,MIN}) \times [(V_{IN} - \#Phase \times V_{OUT}) \times D/(L_{O,MIN} \times f_{SW})] + V_{IN} \times (ESL\,per\,ceramic\,cap./NC_{OUT,MIN})/L_{O,MIN} \quad \text{(eq. 3)}$$

This formula assumes steady−state conditions with no more than one phase on at any time. The second term in Equation 3 is the total ripple current seen by the output capacitors. The total output ripple current is the “time summation” of the four individual phase currents that are 90 degrees out−of−phase. As the inductor current in one phase ramps upward, current in the other phases ramp downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multi−phase converter.

3. Output Inductor Selection

The output inductor is a very critical component in the converter because it directly affects the choice of other components and affects both the steady−state and transient performance of the converter. When selecting an inductor, the designer must consider factors such as DC current, peak current, core loss, magnetic saturation, output voltage ripple, load step and release, temperature, physical size and cost.

In general, the output inductance value should be electrically and physically as small as possible in order to provide the best transient response at minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, lower inductance requires more parallel ceramic output capacitors to make the output filter ESL low enough to avoid excessive output voltage ripple. And the higher ripple current in the MOSFETs and input capacitors increases dissipation and lowers converter efficiency (especially at light loads) − possibly requiring the use of higher rated MOSFETs, an oversized thermal solution, and the use of more or higher current rated input capacitors, which increases converter cost. Too high a ripple current may saturate the inductor, further increasing ripple current and all losses including core loss.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 4 may be used to calculate the inductor value to produce a given maximum ripple current (α) per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the selected maximum ripple current.

$$Lo_{MIN} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{(\alpha \times I_{O,MAX} \times V_{IN} \times f_{SW})} \quad \text{(eq. 4)}$$

α is the ripple current as a percentage of the maximum output current *per phase* (α = 0.15 for ±15%, α = 0.25 for ±25%, etc.). If the minimum inductor value is used, the inductor current will swing ± (α/2)% about its value at the center. Therefore, for a four−phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha/2) \cdot I_{O,MAX}/4$.

The maximum inductor value is limited by the transient response required of the converter. If the converter is to have a fast transient response, the inductor should be made as small as will be allowed by other constraints. If the inductor is too large, its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required and the converter cost will be increased. For a given inductor value (L_O), it is useful to determine the time required to increase or decrease the current.

For increasing current:

$$\Delta t_{INC} = Lo \times \frac{\Delta I_O}{(V_{IN} - V_{OUT})} \quad \text{(eq. 5)}$$

For decreasing current:

$$\Delta t_{DEC} = Lo \times \frac{\Delta I_O}{(V_{OUT})} \quad \text{(eq. 6)}$$

For typical processor applications with output voltages less than one quarter of the input voltage, the current can be increased more quickly than it can be decreased. Thus, it may be more difficult for the converter to avoid overshooting the regulation limits when the load is removed than when it is applied.

4. Input Capacitor Selection

Input capacitors must be both bulk electrolytic and ceramic types. Bulk capacitors are needed to ensure converter stability, and can provide some buffering of the ATX power supply from the effects of load step and release. The ceramic capacitors are needed to provide the input ripple current. The choice and number of ceramic input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors, the converter RMS input ripple current must be calculated by the following procedure:

$$I_{IN,AVG} = I_{O,MAX} \times \frac{D}{\eta} \quad \text{(eq. 7)}$$

where:

D is the duty cycle of the converter, $D = V_{OUT}/V_{IN}$;
η is the specified minimum efficiency;
$I_{O,MAX}$ is the maximum converter output current.

The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 23.

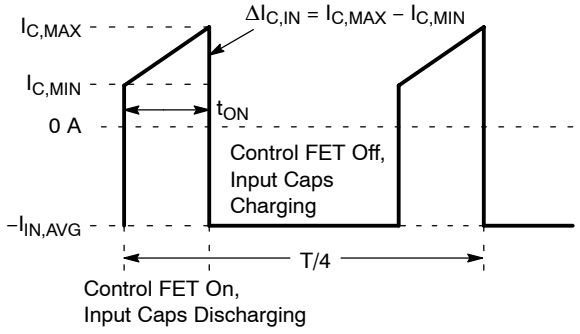


Figure 23. Input Capacitor Current for a Four−Phase Converter

The following equations will determine the maximum and minimum currents delivered by the input capacitors:

$$I_{C,MAX} = \frac{I_{Lo,MAX}}{\eta} - I_{IN,AVG} \quad \text{(eq. 8)}$$

$$I_{C,MIN} = \frac{I_{Lo,MIN}}{\eta} - I_{IN,AVG} \quad \text{(eq. 9)}$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = \frac{I_{O,MAX}}{\phi} + \frac{\Delta I_{Lo}}{2} \quad \text{(eq. 10)}$$

where ϕ is the number of phases in operation.

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = \frac{I_{O,MAX}}{\phi} - \frac{\Delta I_{Lo}}{2} \quad \text{(eq. 11)}$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value Lo:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \times \frac{D}{(Lo \cdot f_{SW})} \quad \text{(eq. 12)}$$

For the four−phase converter, the input capacitor(s) RMS current is then:

$$I_{CIN,RMS} = [4D \times (I_{C,MIN}^2 + I_{C,MIN} \times \Delta I_{C,IN} + \frac{\Delta I_{C,IN}^2}{3}) + I_{IN,AVG}^2 \times (1 - 4D)]^{1/2} \quad \text{(eq. 13)}$$

Select the number of input capacitors (NC_{IN}) to provide the RMS input current ($I_{CIN,RMS}$) based on the RMS ripple current rating per capacitor ($I_{RMS,RATED}$):

$$NC_{IN} = \frac{I_{CIN,RMS}}{I_{RMS,RATED}} \quad \text{(eq. 14)}$$

For a four−phase converter with perfect efficiency ($\eta = 1$), the worst case input ripple−current will occur when the converter is operating at a 12.5% duty cycle. At this operating point, the parallel combination of input capacitors must support an RMS ripple current equal to 12.5% of the converter's DC output current. At other duty cycles, the ripple−current will be less. For example, at a duty cycle of either 6% or 19%, the four−phase input ripple−current will be approximately 10% of the converter's DC output current. In general, capacitor manufacturers require derating to the specified ripple−current based on the ambient temperature. More capacitors will be required because of the current derating.

5. Input Inductor Selection

The use of an inductor between the input capacitors and the power source isolates the voltage source and the system from noise generated by the switching converter, while also reducing the input current slew rate during load transients. The worst case input current slew rate will occur during the first few PWM cycles immediately after a step−load change is applied as shown in Figure 24. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously, so the initial transient load current is conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output current ($I_{O,MAX}$), the per capacitor ESR of the output capacitors (ESR_{OUT}) and the number of bulk electrolytic output capacitors (NB_{OUT}) as shown in Figure 24. The output voltage at full transient load will be:

$$V_{OUT,FULL-LOAD} = V_{OUT,NO-LOAD} - (I_{O,MAX}) \times \frac{ESR_{OUT}}{NB_{OUT}} \quad \text{(eq. 15)}$$

When the control MOSFET (Q1 in Figure 24) turns ON, the input voltage will be applied to the input terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as:

$$\Delta V_{Lo} = V_{IN} - V_{OUT,FULL-LOAD} = V_{IN} - V_{OUT,NO-LOAD} + (I_{O,MAX}) \times \frac{ESR_{OUT}}{NB_{OUT}} \quad \text{(eq. 16)}$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from:

$$\frac{dI_{Lo}}{dt} = \frac{\Delta V_{Lo}}{Lo} \quad \text{(eq. 17)}$$

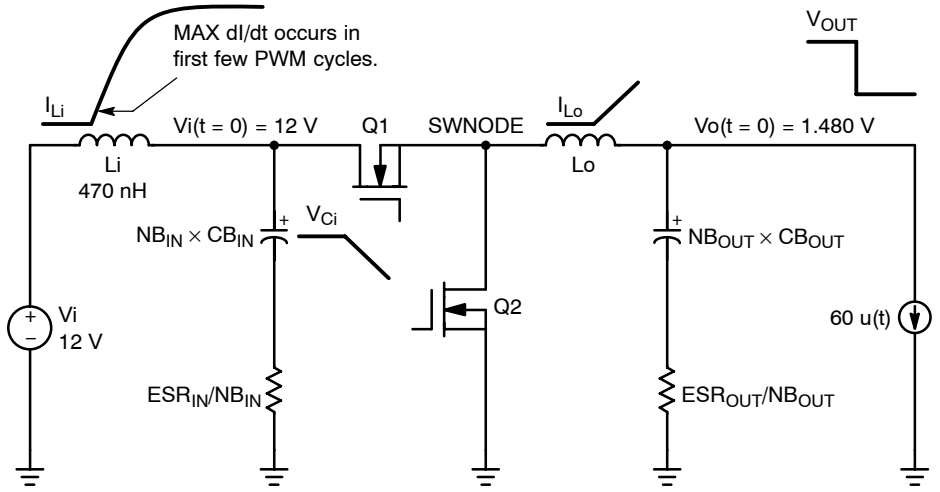


Figure 24. Calculating the Input Inductance

Current changes slowly in the input inductor so the input capacitors must initially deliver most of the input current. The amount of voltage drop across the input capacitors (ΔV_{CIN}) is determined by the number of bulk input capacitors (NB_{IN}), their per capacitor ESR (ESR_{IN}) and the current in the output inductor according to:

$$\Delta V_{CIN} = \frac{ESR_{IN}}{NB_{IN}} \times \frac{dI_{Lo}}{dt} \times \frac{D}{f_{SW}} \qquad \text{(eq. 18)}$$

Before the load is applied, the voltage across the input inductor (V_{LIN}) is very small and the input capacitors charge to the input voltage V_{IN}. After the load is applied, the voltage drop across the input capacitors, ΔV_{CIN}, appears across the input inductor as well. From this, the minimum value of the input inductor can be calculated from:

$$Li_{MIN} = \frac{V_{LIN}}{\left(\frac{dI_{IN}}{dt_{MAX}}\right)} = \frac{\Delta V_{CIN}}{\left(\frac{dI_{IN}}{dt_{MAX}}\right)} \qquad \text{(eq. 19)}$$

dI_{IN}/dt_{MAX} is the maximum allowable input current slew rate.

The input inductance value calculated from Equation 19 is relatively conservative. It assumes the supply voltage is very “stiff” and does not account for any parasitic elements that will limit dI/dt such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer’s data sheets are worst case high limits. In reality, input voltage “sag,” lower capacitor ESRs and stray inductance will further reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating. Also, for an inexpensive iron powder core, such as the −26 or −52 from Micrometals, the inductance “swing” with DC bias must be taken into account since inductance will decrease as the DC input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the dI/dt will be higher than expected.

6. MOSFET and Heatsink Selection

Power dissipation, package size and thermal requirements drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches with nearly zero voltage. However, the body diode in the synchronous MOSFET will incur diode losses during the non−overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$P_{D,CONTROL} = (I_{RMS,CNTL}^2 \times R_{DS(on)}) + (I_{Lo,MAX} \times \frac{Q_{switch}}{I_g} \times V_{IN} \times f_{SW}) + (\frac{Q_{oss}}{2} \times V_{IN} \times f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \qquad \text{(eq. 20)}$$

The first term represents the conduction or I^2R losses when the MOSFET is ON while the second term represents switching OFF losses. The third term is the loss associated with charging the control and synchronous MOSFET output capacitances when the control MOSFET turns ON. The output losses are caused by the output capacitances of both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovered charge of the body diode in the synchronous MOSFET. The first two terms are usually adequate to predict the majority of the losses.

$I_{RMS,CNTL}$ is the RMS value of the current in the control MOSFET:

$$I_{RMS,CNTL} = (D \times (I_{Lo,MAX}^2 - I_{Lo,MAX} \times I_{Lo,MIN} + \frac{I_{Lo,MIN}^2}{3}))^{1/2} \quad \text{(eq. 21)}$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = \frac{I_{O,MAX}}{\phi} + \frac{\Delta I_{Lo}}{2} \quad \text{(eq. 22)}$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = \frac{I_{O,MAX}}{\phi} - \frac{\Delta I_{Lo}}{2} \quad \text{(eq. 23)}$$

$I_{O,MAX}$ is the maximum converter output current.
D is the duty cycle of the converter:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 24)}$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value L_o:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \times \frac{D}{(Lo \times f_{SW})} \quad \text{(eq. 25)}$$

$R_{DS(on)}$ is the ON resistance of the high side MOSFET at the applied gate drive voltage. Q_{switch} is the post gate threshold portion of the gate−to−source charge plus the gate−to−drain charge. This may be specified in the data sheet or approximated from the gate−charge curve as shown in the Figure 25.

$$Q_{switch} = Q_{gs2} + Q_{gd} \quad \text{(eq. 26)}$$

I_g is the output current from the gate driver IC.
V_{IN} is the input voltage to the converter.
f_{sw} is the switching frequency of the converter.
Q_{RR} is the reverse recovery charge of the *lower* MOSFET.
Q_{oss} is the sum of the high and low side MOSFET output charges specified in the data sheets, or estimated from integrating C_{OSS} from zero volts to V_{IN}.

For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$P_{D,SYNCH} = (I_{RMS,SYNCH}^2 \times R_{DS(on)}) + (Vf_{diode} \times I_{O,MAX} \times t_{nonoverlap} \times f_{SW}) \quad \text{(eq. 27)}$$

where:

Vf_{diode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.
$t_{nonoverlap}$ is the non−overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the driver IC.

The first term represents the conduction or I^2R losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non−overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$I_{RMS,SYNCH} = ((1 - D) \times (I_{Lo,MAX}^2 + I_{Lo,MAX} \times I_{Lo,MIN} + \frac{I_{Lo,MIN}^2}{3}))^{1/2} \quad \text{(eq. 28)}$$

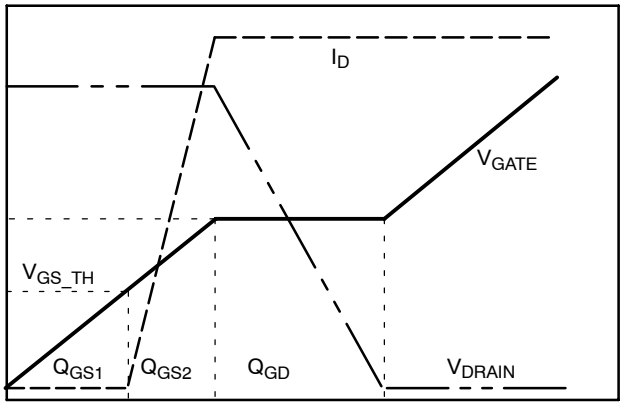


Figure 25. MOSFET Switching Characteristics

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature.

$$\theta_T < (T_J - T_A)/P_D \quad \text{(eq. 29)}$$

where:

θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$);
θ_{JC} is the junction−to−case thermal impedance of the MOSFET;
θ_{SA} is the sink−to−ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET if no thermal "pad" is used;
T_J is the specified maximum allowed junction temperature;
T_A is the worst case ambient operating temperature.

For TO−220 and TO−263 packages, standard FR−4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown below:

Pad Size (in^2/mm^2)	Single−Sided 1 oz. Copper
0.50/323	60−65°C/W
0.75/484	55−60°C/W
1.00/645	50−55°C/W
1.50/968	45−50°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading and component variations (i.e., worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, it is advisable to have as much heatsink area as possible. All too often, new designs are found to be too hot and require re−design to add heatsinking.

7. Error Amplifier Tuning

The high frequency gain of the voltage feedback loop affects transient response and control loop stability. This loop gain can be adjusted by changing the Error Amplifier's high frequency gain, which is done by increasing or decreasing the Error Amplifier output loading capacitor (C_{AMP}). The Error Amplifier has a transconductance characteristic (amplifier output current is proportional to amplifier input voltage), causing amplifier output voltage to be proportional to amplifier output load impedance.

If C_{AMP} is too large, the loop gain at high frequencies will be too low, and the converter output voltage may exhibit an underdamped response to a load transient. On the other hand, if C_{AMP} is too small, there will be too much loop gain at high frequencies, which may decrease converter output voltage stability. For initial prototype startup, C_{AMP} = 10 nF is recommended. When reducing C_{AMP}, peak−to−peak ripple voltage at the COMP pin should remain less than 20 mVp−p. Excessive ripple at the COMP pin will contribute to PWM pulse jitter. In general, the lowest loop gain that achieves acceptable transient response should be used.

Adding a resistor in series with C_{AMP} will increase control loop damping in response to load transients as shown in Figures 26 and 27, where 1430 Ω was added in series with the 1.8 nF C_{AMP} (Adaptive Voltage Positioning not used).

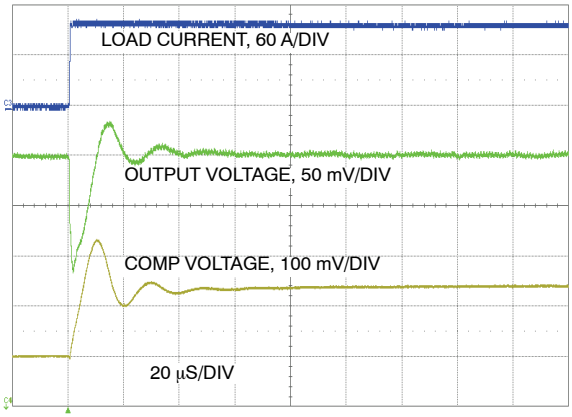


Figure 26. Converter Output and COMP Response to a Load Step (No Droop). 0 Ω in Series with C_{AMP}

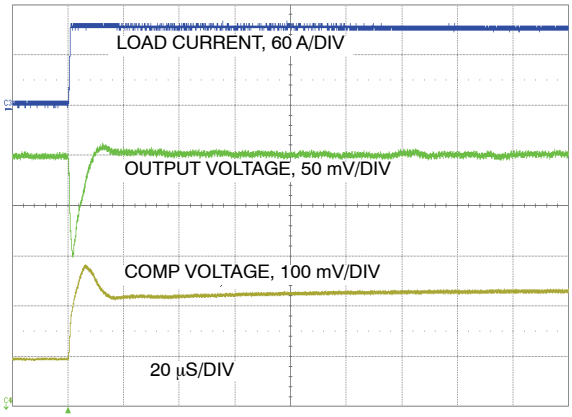
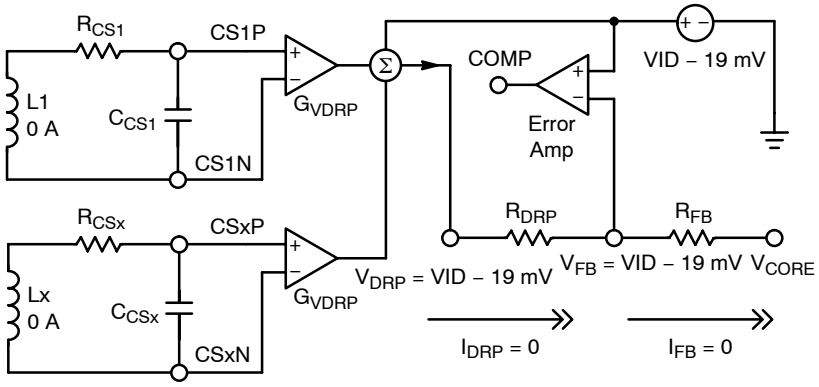


Figure 27. Converter Output and COMP Response to a Load Step (No Droop), Resistance in Series with C_{AMP}

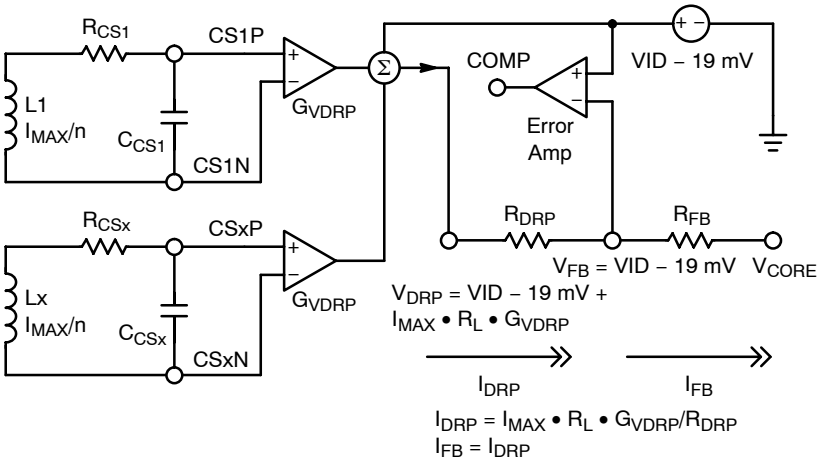
8. Adaptive Voltage Positioning

Two resistors program the Adaptive Voltage Positioning (AVP): R_{FB} and R_{DRP}. These components form a resistor divider, shown in Figures 28 and 29, between V_{DRP}, V_{FB}, and V_{OUT}.



$$V_{CORE} = VID - 19\ mV + IBIAS_{VFB} \bullet R_{FB}$$

Figure 28. AVP Circuitry at No−Load



$$V_{CORE} = VID - 19\ mV - I_{DRP} \bullet R_{FB}$$
$$= VID - 19\ mV - I_{MAX} \bullet R_L \bullet G_{VDRP} \bullet R_{FB}/R_{DRP}$$

Figure 29. AVP Circuitry at Full−Load

Resistor R_{FB} is connected between V_{OUT} and the V_{FB} pin of the controller. At no load, this resistor will conduct the very small internal bias current of the V_{FB} pin. Therefore R_{FB} should be kept below 10 kΩ to avoid output voltage error due to the input bias current. If the R_{FB} resistor is kept small, the V_{FB} bias current can be ignored.

Resistor R_{DRP} is connected between the V_{DRP} and V_{FB} pins of the controller. At no load, V_{DRP} , V_{FB} and V_{OUT} are at the same potential, and no current should flow through R_{DRP} or R_{FB}. As load current increases, the voltage at the V_{DRP} pin rises. The the R_{DRP} and R_{FB} resistors cause the voltage at V_{OUT} to fall in order to keep the voltage at the V_{FB} pin close to the reference voltage. Figure 30 shows the DC effect of AVP.

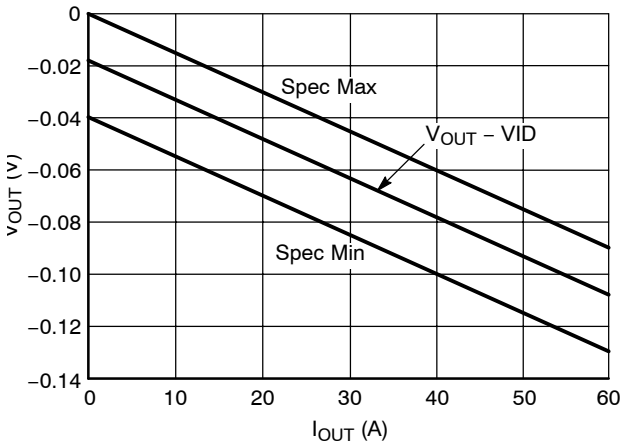


Figure 30. The DC Effects of AVP vs. Load

To choose components, select the appropriate resistor ratio based on the desired loadline and sense resistor. At no load, the output voltage is positioned 19 mV below the DAC output setting. The output voltage droop will follow the equation:

$$\frac{R_{DRP}}{R_{FB}} = g \times \frac{R_{SENSE}}{R_{LL}} \qquad \text{(eq. 30)}$$

where:

g = gain of the current sense amplifiers (V/V);
R_{SENSE} = resistance of the sense element (mΩ);
R_{LL} = load line resistance (mΩ).

It is easiest to select a value for R_{FB} and then evaluate the equation to find R_{DRP}. R_{LL} is simply the desired output voltage droop divided by the output current. If a sense resistor is used to detect inductor current, then R_{SENSE} will be the value of the sense resistor. If inductor sensing is used, R_{SENSE} will be the resistance of the inductor. Refer to the discussion on Current Sensing for further information.

Depending on inductor ESR and the loadline desired, adding a capacitor on the order of 1 nF in parallel with R_{DRP} may improve the transient output voltage waveshape.

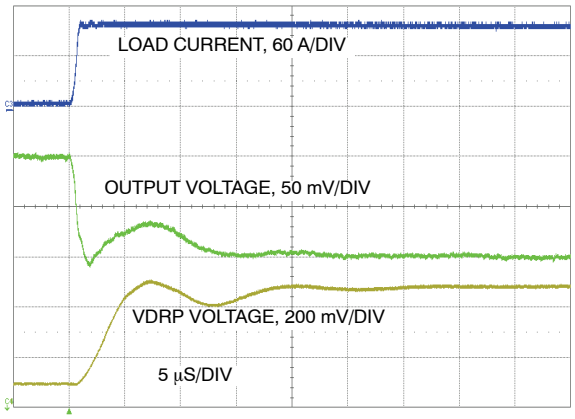


Figure 31. Output Voltage – No Capacitor in Parallel with R_{DRP}

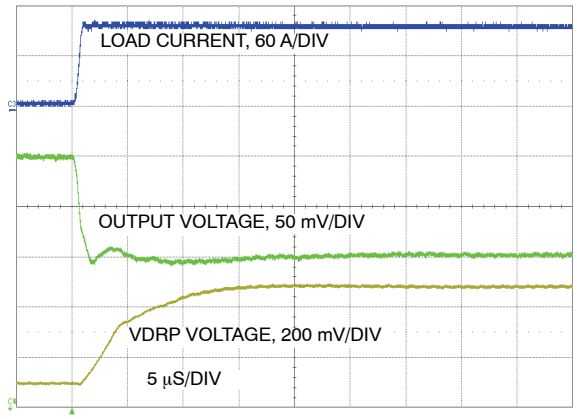


Figure 32. Output Voltage – 1.2 nF Capacitor in Parallel with R_{DRP}

9. Current Sensing

Current sensing is used to balance current between different phases, to limit the maximum phase current and to limit the maximum system current. Since the current information is a part of the control loop, better stability is achieved if the current information is accurate and noise−free. The NCP5318 uses differential current sense amplifiers to achieve the best possible performance.

Two sense lines are routed for each phase, as shown in Figure 29.

For inductive current sensing, choose the current sense network (R_{CSx}, C_{CSx}, x = 1, 2, 3 or 4) to satisfy

$$R_{CSx} \times C_{CSx} = \frac{Lo}{R_L} \qquad \text{(eq. 31)}$$

where R_L is the inductor ESR. This will provide an adequate starting point for R_{CSx} and C_{CSx}. After the converter is constructed, the value of R_{CSx} (and/or C_{CSx}) should be fine−tuned in the lab by observing the V_{DRP} signal during a step change in load current. Tune the R_{CSx} x C_{CSx} network by varying R_{CSx} to provide a “square−wave” at the V_{DRP} output pin with maximum rise time and minimal overshoot as shown in Figure 35.

For resistive current sensing, choose the current sense network (R_{CSx}, C_{CSx}, x = 1, 2, 3, or 4) to reject noise spikes, but maintain the fidelity of the triangular current waveform.

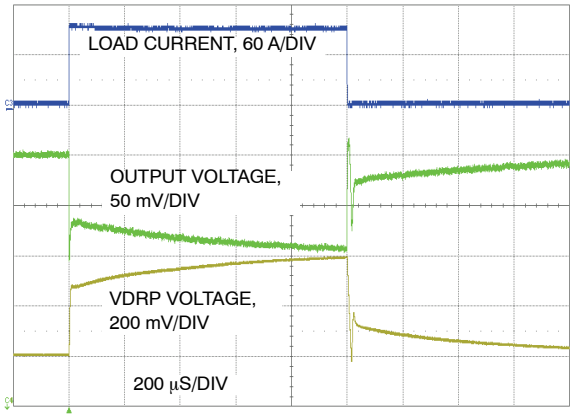


Figure 33. V_{DRP} tuning waveforms. The RC time constant of the current sense network is too long (Slow): V_{DRP} and V_{OUT} respond too slowly.

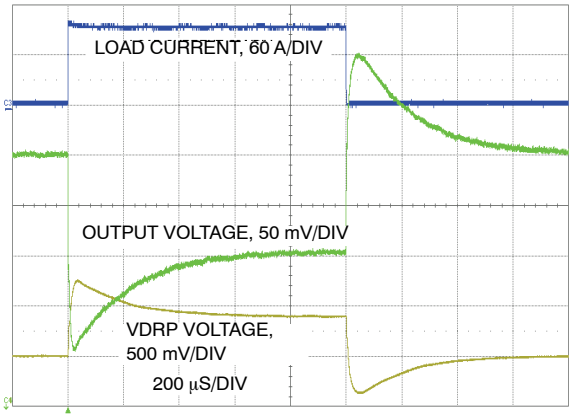


Figure 34. V_{DRP} tuning waveforms. The RC time constant of the current sense network is too short (Fast): V_{DRP} and V_{OUT} both overshoot.

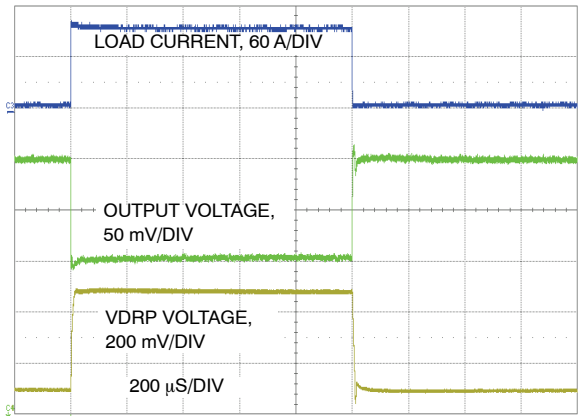


Figure 35. V_{DRP} tuning waveforms. The RC time constant of the current sense network is optimal: V_{DRP} and V_{OUT} respond to the load current quickly without overshooting.

10. Current Limit Setting

When the output of the current sense amplifier (COx in the block diagram) exceeds the voltage on the I_{LIM} pin, the part will latch off. For inductive sensing, the I_{LIM} pin voltage should be set based on the inductor's maximum resistance (R_{LMAX}). The design must consider the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is +0.39% per °C. If using a current sense resistor (R_{SENSE}), the I_{LIM} pin voltage should be set based on the maximum value of the sense resistor.

For the overcurrent protection to avoid false tripping, the voltage at the I_{LIM} pin should be set even higher if the R_{CSx} x C_{CSx} time constant is set faster than the L_O / R_L time constant. A step load change may cause the current signal to appear larger than the actual inductor current and trip the current limit at a lower level than desired. The waveforms in Figure 36 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of L = 500 nH, R_L = 1.6 mΩ, R_{CSx} = 20 kΩ, and C_{CSx} = 0.01 μF. In this case, ideal current signal compensation would require V_{CSx} to be 31 k. Due to the faster than ideal RC time constant, there is an overshoot of 50% and the overshoot decays with a 200 μs time constant. With this compensation, the I_{LIM} pin threshold must be set more than 50% above the full load current to avoid triggering current limit during a large output load step.

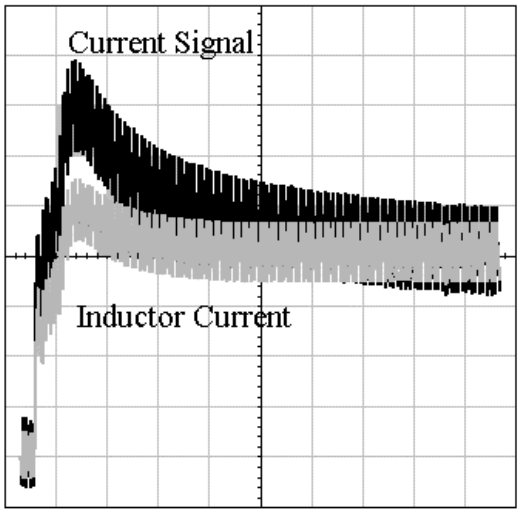


Figure 36. Inductive sensing waveform during a load step with fast RC time constant (50 μs/div)

The proper I_{LIM} pin voltage can be calculated by:

$$V_{ILIM} = (I_{RIPP-P}/(2 \times \#PH) + I_L) \times R_L \times (1 + 0.004 \times (T_L - 25)) \times g + OS_{ILIM}$$

where:

I_L = maximum converter current (A)
R_L = maximum 25°C sense element resistance (Ω)
g = maximum current sense to I_{LIM} gain (see tabulated specs)
I_{RIPP-P} = peak−to−peak phase ripple current (A)
#PH = number of phases
T_L = inductor temperature at overload (°C)
OS_{ILIM} = maximum I_{LIM} offset (see tabulated specs) (V)

This voltage can be programmed by a resistor divider from the R_{OSC} pin, as shown in Figure 37.

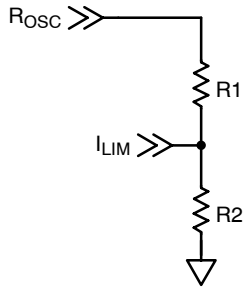


Figure 37. Programming the Current Limit

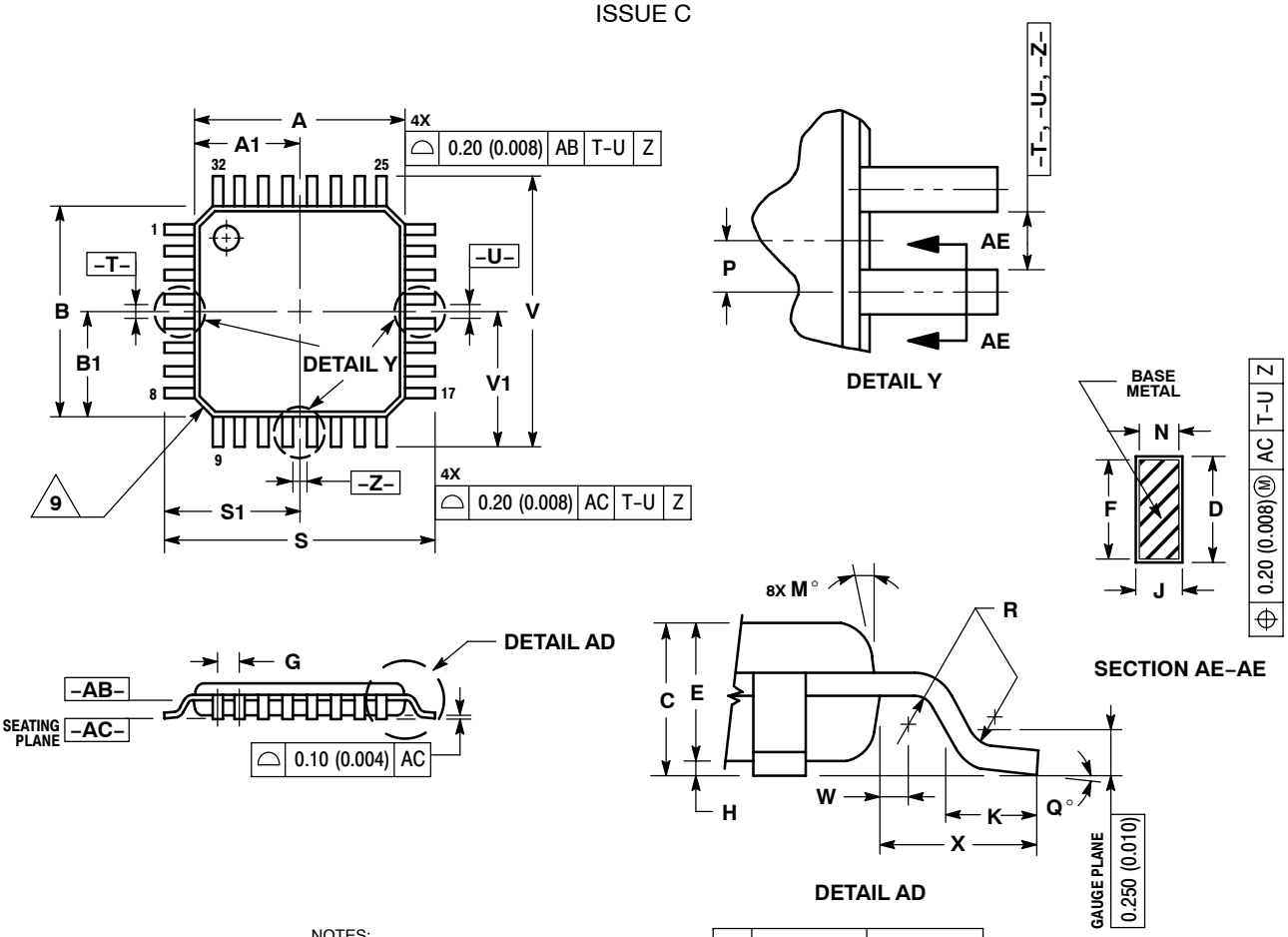
When the NCP5318 is powered up, the R_{OSC} pin will be 1.0 V. This allows the user to determine the resistor divider above by:

$R2 = R_{TOTAL}$ x V_{LIM} / 1.0 V
$R1 = R_{TOTAL} - R2$

Where R_{TOTAL} is determined as in Section 1 above.

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A–02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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