

## FTG for VIA PL133T and PLE133T

### Features

- Single-chip system frequency synthesizer for VIA PL133T and PLE133T chipsets
- Programmable clock output frequency with less than 1 MHz increment
- Integrated fail-safe Watchdog Timer for system recovery
- Automatically switches to HW-selected or SW-programmed clock frequency when Watchdog Timer time-out occurs
- Capable of generating system RESET after a Watchdog Timer time-out occurs or a change in output frequency via SMBus interface
- Supports SMBus byte Read/Write and block Read/Write operations to simplify system BIOS development

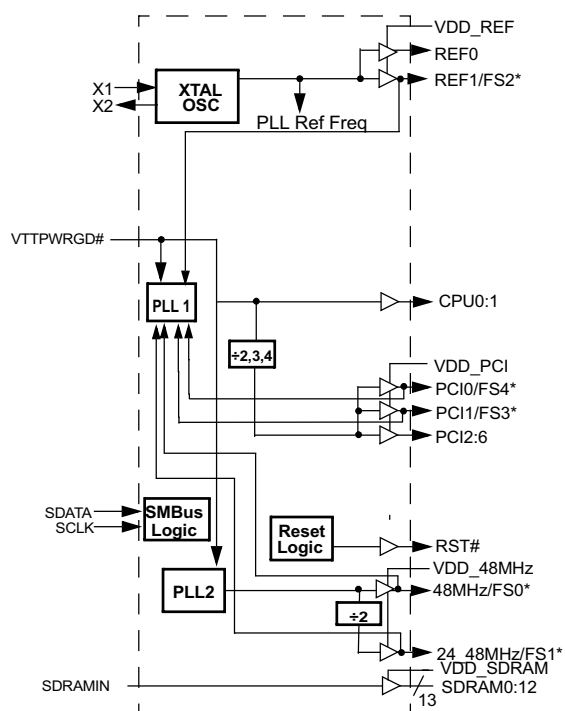
- Vendor ID and Revision ID support
- Programmable drive strength for SDRAM and PCI output clocks
- Programmable output skew for CPU, PCI, and SDRAM
- Maximized electromagnetic interference (EMI) suppression using Cypress's Spread Spectrum technology
- Available in 48-pin SSOP

### Key Specifications

CPU to CPU Output Skew: ..... 175 ps

PCI to PCI Output Skew: ..... 500 ps

### Block Diagram



### Pin Configuration<sup>[1]</sup>

|               |    |    |               |
|---------------|----|----|---------------|
| VDD_REF       | 1  | 48 | VTT_PWRGD#    |
| GND_REF       | 2  | 47 | REF0          |
| X1            | 3  | 46 | REF1/FS2*     |
| X2            | 4  | 45 | GND_CPU       |
| VDD_PCI       | 5  | 44 | CPU0          |
| *FS4/PCI0     | 6  | 43 | CPU1          |
| *FS3/PCI1     | 7  | 42 | VDD_CPU       |
| GND_PCI       | 8  | 41 | RST#          |
| PCI2          | 9  | 40 | SDRAM_12      |
| PCI3          | 10 | 39 | GND_SDRAM     |
| PCI4          | 11 | 38 | SDRAM0        |
| PCI5          | 12 | 37 | SDRAM1        |
| PCI6          | 13 | 36 | VDD_SDRAM     |
| VDD_PCI       | 14 | 35 | SDRAM2        |
| SDRAMIN       | 15 | 34 | SDRAM3        |
| GND_SDRAM     | 16 | 33 | GND_SDRAM     |
| SDRAM11       | 17 | 32 | SDRAM4        |
| SDRAM10       | 18 | 31 | SDRAM5        |
| VDD_SDRAM     | 19 | 30 | VDD_SDRAM     |
| SDRAM9        | 20 | 29 | SDRAM6        |
| SDRAM8        | 21 | 28 | SDRAM7        |
| GND_SDRAM     | 22 | 27 | VDD_48MHz     |
| SMBus { SDATA | 23 | 26 | 48MHz/FS0*    |
| SMBus { SCLK  | 24 | 25 | 24_48MHz/FS1* |

#### Note:

1. Signals marked with '\*' have internal pull-up resistors.

## Pin Definitions

| Pin Name                                                    | Pin No.                                            | Pin Type          | Pin Description                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------|----------------------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CPU0:1                                                      | 44, 43                                             | O                 | <b>CPU Clock Output 0 through 1:</b> CPU clocks for processor and chipset.                                                                                                                                                                                                                   |
| PCI2:6                                                      | 9, 10, 11, 12, 13                                  | O                 | <b>PCI Clock Outputs 2 through 6:</b> 3.3V 33-MHz PCI clock outputs. Frequency is set by FS0:4 inputs or through serial data interface.                                                                                                                                                      |
| PCI1/FS3                                                    | 7                                                  | I/O               | <b>Fixed PCI Clock Output/Frequency Select 3:</b> 3.3V PCI clock outputs. As an output, frequency is set by FS0:4 inputs or through the serial data interface. This pin also serves as a power-on strap option to determine the device operating frequency, as described in <i>Table 5</i> . |
| PCI0/FS4                                                    | 6                                                  | I/O               | <b>Fixed PCI Clock Output/Frequency Select 4:</b> 3.3V PCI clock outputs. This pin also serves as a power-on strap option to determine the device operating frequency, as described in <i>Table 5</i> .                                                                                      |
| RST#                                                        | 41                                                 | O<br>(open-drain) | <b>Reset# Output:</b> Open drain system reset output.                                                                                                                                                                                                                                        |
| 48MHz/FS0                                                   | 26                                                 | I/O               | <b>48-MHz Output/Frequency Select 0:</b> 3.3V 48-MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine the device operating frequency as described in <i>Table 5</i> .                                                                                |
| 24_48MHz/<br>FS1                                            | 25                                                 | I/O               | <b>24_48MHz Output/Frequency Select 1:</b> 3.3V 24- or 48-MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine the device operating frequency, as described in <i>Table 5</i> .                                                                      |
| REF1/FS2                                                    | 46                                                 | I/O               | <b>Reference Clock Output 1/Frequency Select 2:</b> 3.3V 14.318-MHz output clock. This pin also serves as a power-on strap option to determine the device operating frequency as described in <i>Table 5</i> .                                                                               |
| REF0                                                        | 47                                                 | O                 | <b>Reference Clock Output 0:</b> 3.3V 14.318-MHz output clock.                                                                                                                                                                                                                               |
| SDRAMIN                                                     | 15                                                 | I                 | <b>SDRAM Buffer Input Pin:</b> Reference input for SDRAM buffer.                                                                                                                                                                                                                             |
| SDRAM0:12                                                   | 38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17, 40 | O                 | <b>SDRAM Outputs:</b> These thirteen dedicated outputs provide copies of the signal provided at the SDRAMIN input.                                                                                                                                                                           |
| SCLK                                                        | 24                                                 | I                 | <b>Clock pin for SMBus circuitry.</b>                                                                                                                                                                                                                                                        |
| SDATA                                                       | 23                                                 | I/O               | <b>Data pin for SMBus circuitry.</b>                                                                                                                                                                                                                                                         |
| X1                                                          | 3                                                  | I                 | <b>Crystal Connection or External Reference Frequency Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.                                                                                       |
| X2                                                          | 4                                                  | O                 | <b>Crystal Connection:</b> An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.                                                                                                                                       |
| VTT_PWRGD#                                                  | 48                                                 | I                 | <b>VTT_PWRGD#:</b> 3.3V LVTTTL compatible input that controls the FS0:4 to be latched and enables all outputs. CY28316 will sample the FS0:4 inputs and enable all clock outputs after all V <sub>DD</sub> become valid and VTT_PWRGD# is held LOW.                                          |
| VDD_REF,<br>VDD_PCI,<br>VDD_SDRAM,<br>VDD_48MHz             | 1, 5, 14, 19, 27, 30, 36                           | P                 | <b>Power Connection:</b> Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48-MHz output, and 24_48-MHz output. Connect to 3.3V supply.                                                                                                             |
| VDD_CPU                                                     | 42                                                 | P                 | <b>Power Connection:</b> Power supply for CPU outputs. Connect to 2.5V supply.                                                                                                                                                                                                               |
| GND_REF,<br>GND_PCI,<br>GND_SDRAM,<br>VDD_48MHz,<br>VDD_CPU | 2, 8, 16, 22, 33, 39, 45                           | G                 | <b>Ground Connections:</b> Connect all ground pins to the common system ground plane.                                                                                                                                                                                                        |

## Serial Data Interface

The CY28316 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

## Data Protocol

The clock driver serial protocol supports byte/word Write, byte/word Read, block Write and block Read operations from the controller. For block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte, with the ability to stop after any complete byte has been transferred. For byte/word Write and byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code.

The definition for the command code is defined in *Table 1*.

**Table 1. Command Code Definition**

| Bit | Descriptions                                                                                                                   |
|-----|--------------------------------------------------------------------------------------------------------------------------------|
| 7   | 0 = Block read or block write operation<br>1 = Byte/Word read or byte/word write operation                                     |
| 6:0 | Byte offset for byte/word read or write operation. For block read or write operations, these bits need to be set at '0000000.' |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol |                                                                | Block Read Protocol |                                                                |
|----------------------|----------------------------------------------------------------|---------------------|----------------------------------------------------------------|
| Bit                  | Description                                                    | Bit                 | Description                                                    |
| 1                    | Start                                                          | 1                   | Start                                                          |
| 2:8                  | Slave address – 7 bits                                         | 2:8                 | Slave address – 7 bits                                         |
| 9                    | Write                                                          | 9                   | Write                                                          |
| 10                   | Acknowledge from slave                                         | 10                  | Acknowledge from slave                                         |
| 11:18                | Command Code – 8 bits<br>'00000000' stands for block operation | 11:18               | Command Code – 8 bits<br>'00000000' stands for block operation |
| 19                   | Acknowledge from slave                                         | 19                  | Acknowledge from slave                                         |
| 20:27                | Byte Count – 8 bits                                            | 20                  | Repeat start                                                   |
| 28                   | Acknowledge from slave                                         | 21:27               | Slave address – 7 bits                                         |
| 29:36                | Data byte 0 – 8 bits                                           | 28                  | Read                                                           |
| 37                   | Acknowledge from slave                                         | 29                  | Acknowledge from slave                                         |
| 38:45                | Data byte 1 – 8 bits                                           | 30:37               | Byte count from slave – 8 bits                                 |
| 46                   | Acknowledge from slave                                         | 38                  | Acknowledge                                                    |
| ...                  | Data Byte N/Slave Acknowledge...                               | 39:46               | Data byte from slave – 8 bits                                  |
| ...                  | Data Byte N – 8 bits                                           | 47                  | Acknowledge                                                    |
| ...                  | Acknowledge from slave                                         | 48:55               | Data byte from slave – 8 bits                                  |
| ...                  | Stop                                                           | 56                  | Acknowledge                                                    |
|                      |                                                                | ...                 | Data bytes from slave/Acknowledge                              |
|                      |                                                                | ...                 | Data byte N from slave – 8 bits                                |
|                      |                                                                | ...                 | Not acknowledge                                                |
|                      |                                                                | ...                 | Stop                                                           |

**Table 3. Word Read and Word Write Protocol**

| Word Write Protocol |                        | Word Read Protocol |                        |
|---------------------|------------------------|--------------------|------------------------|
| Bit                 | Description            | Bit                | Description            |
| 1                   | Start                  | 1                  | Start                  |
| 2:8                 | Slave address – 7 bits | 2:8                | Slave address – 7 bits |
| 9                   | Write                  | 9                  | Write                  |
| 10                  | Acknowledge from slave | 10                 | Acknowledge from slave |

**Table 3. Word Read and Word Write Protocol (continued)**

| Word Write Protocol |                                                                                                                                                           | Word Read Protocol |                                                                                                                                                           |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                 | Description                                                                                                                                               | Bit                | Description                                                                                                                                               |
| 11:18               | Command Code – 8 bits<br>'1xxxxxxx' stands for byte or word operation<br>bit[6:0] of the command code represents the offset<br>of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'1xxxxxxx' stands for byte or word operation<br>bit[6:0] of the command code represents the offset<br>of the byte to be accessed |
| 19                  | Acknowledge from slave                                                                                                                                    | 19                 | Acknowledge from slave                                                                                                                                    |
| 20:27               | Data byte low – 8 bits                                                                                                                                    | 20                 | Repeat start                                                                                                                                              |
| 28                  | Acknowledge from slave                                                                                                                                    | 21:27              | Slave address – 7 bits                                                                                                                                    |
| 29:36               | Data byte high – 8 bits                                                                                                                                   | 28                 | Read                                                                                                                                                      |
| 37                  | Acknowledge from slave                                                                                                                                    | 29                 | Acknowledge from slave                                                                                                                                    |
| 38                  | Stop                                                                                                                                                      | 30:37              | Data byte low from slave – 8 bits                                                                                                                         |
|                     |                                                                                                                                                           | 38                 | Acknowledge                                                                                                                                               |
|                     |                                                                                                                                                           | 39:46              | Data byte high from slave – 8 bits                                                                                                                        |
|                     |                                                                                                                                                           | 47                 | Not acknowledge                                                                                                                                           |
|                     |                                                                                                                                                           | 48                 | Stop                                                                                                                                                      |

**Table 4. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                                                                                                                                                   | Byte Read Protocol |                                                                                                                                                   |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                 | Description                                                                                                                                       | Bit                | Description                                                                                                                                       |
| 1                   | Start                                                                                                                                             | 1                  | Start                                                                                                                                             |
| 2:8                 | Slave address – 7 bits                                                                                                                            | 2:8                | Slave address – 7 bits                                                                                                                            |
| 9                   | Write                                                                                                                                             | 9                  | Write                                                                                                                                             |
| 10                  | Acknowledge from slave                                                                                                                            | 10                 | Acknowledge from slave                                                                                                                            |
| 11:18               | Command Code – 8 bits<br>'1xxxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset<br>of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'1xxxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset<br>of the byte to be accessed |
| 19                  | Acknowledge from slave                                                                                                                            | 19                 | Acknowledge from slave                                                                                                                            |
| 20:27               | Data byte – 8 bits                                                                                                                                | 20                 | Repeat start                                                                                                                                      |
| 28                  | Acknowledge from slave                                                                                                                            | 21:27              | Slave address – 7 bits                                                                                                                            |
| 29                  | Stop                                                                                                                                              | 28                 | Read                                                                                                                                              |
|                     |                                                                                                                                                   | 29                 | Acknowledge from slave                                                                                                                            |
|                     |                                                                                                                                                   | 30:37              | Data byte from slave – 8 bits                                                                                                                     |
|                     |                                                                                                                                                   | 38                 | Not acknowledge                                                                                                                                   |
|                     |                                                                                                                                                   | 39                 | Stop                                                                                                                                              |

## CY28316 Serial Configuration Map

1. The serial bits will be read by the clock driver in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a “0” level.

3. All register bits labeled “Write with 1” must be written to “1” during initialization.

### Byte 0: Control Register 0

| Bit   | Pin# | Name           | Default | Description                                                                                                   |
|-------|------|----------------|---------|---------------------------------------------------------------------------------------------------------------|
| Bit 7 | –    | Spread Select1 | 0       | See definition in Bit[0].                                                                                     |
| Bit 6 | –    | SEL2           | 0       | See Table 5.                                                                                                  |
| Bit 5 | –    | SEL1           | 0       | See Table 5.                                                                                                  |
| Bit 4 | –    | SEL0           | 0       | See Table 5.                                                                                                  |
| Bit 3 | –    | FS_Override    | 0       | 0 = Select operating frequency by FS[4:0] input pins.<br>1 = Select operating frequency by SEL[4:0] settings. |
| Bit 2 | –    | SEL4           | 0       | See Table 5.                                                                                                  |
| Bit 1 | –    | SEL3           | 0       | See Table 5.                                                                                                  |
| Bit 0 | –    | Spread Select0 | 0       | ‘00’ = OFF.<br>‘01’ = – 0.5%.<br>‘10’ = ± 0.5%.<br>‘11’ = ± 0.25%.                                            |

### Byte 1: Control Register 1

| Bit   | Pin# | Name              | Default | Description                                       |
|-------|------|-------------------|---------|---------------------------------------------------|
| Bit 7 | 6    | Latched FS4 input | X       | Latched FS[4:0] inputs. These bits are read-only. |
| Bit 6 | 7    | Latched FS3 input | X       |                                                   |
| Bit 5 | 46   | Latched FS2 input | X       |                                                   |
| Bit 4 | 25   | Latched FS1 input | X       |                                                   |
| Bit 3 | 26   | Latched FS0 input | X       |                                                   |
| Bit 2 | 44   | CPU0              | 1       | (Active/Inactive).                                |
| Bit 1 | 43   | CPU1              | 1       | (Active/Inactive).                                |
| Bit 0 | –    | Vendor Test Mode  | 1       | Write with ‘1.’                                   |

### Byte 2: Control Register 2

| Bit   | Pin# | Name    | Default | Description        |
|-------|------|---------|---------|--------------------|
| Bit 7 | 40   | SDRAM12 | 1       | (Active/Inactive). |
| Bit 6 | 6    | PCI0    | 1       | (Active/Inactive). |
| Bit 5 | 13   | PCI6    | 1       | (Active/Inactive). |
| Bit 4 | 12   | PCI5    | 1       | (Active/Inactive). |
| Bit 3 | 11   | PCI4    | 1       | (Active/Inactive). |
| Bit 2 | 10   | PCI3    | 1       | (Active/Inactive). |
| Bit 1 | 9    | PCI2    | 1       | (Active/Inactive). |
| Bit 0 | 7    | PCI1    | 1       | (Active/Inactive). |

**Byte 3: Control Register 3**

| Bit   | Pin#           | Name      | Default | Description                |
|-------|----------------|-----------|---------|----------------------------|
| Bit 7 | 21, 20, 18, 17 | SDRAM8:11 | 1       | (Active/Inactive).         |
| Bit 6 | –              | SEL_48MHz | 0       | 0 = 24 MHz.<br>1 = 48 MHz. |
| Bit 5 | 26             | 48MHz     | 1       | (Active/Inactive).         |
| Bit 4 | 25             | 24_48MHz  | 1       | (Active/Inactive).         |
| Bit 3 | 29, 28         | SDRAM6:7  | 1       | (Active/Inactive).         |
| Bit 2 | 32, 31         | SDRAM4:5  | 1       | (Active/Inactive).         |
| Bit 1 | 35, 34         | SDRAM2:3  | 1       | (Active/Inactive).         |
| Bit 0 | 38, 37         | SDRAM0:1  | 1       | (Active/Inactive).         |

**Byte 4: Control Register 4**

| Bit   | Pin# | Name     | Default | Description |
|-------|------|----------|---------|-------------|
| Bit 7 | –    | Reserved | 0       | Reserved.   |
| Bit 6 | –    | Reserved | 0       | Reserved.   |
| Bit 5 | –    | Reserved | 0       | Reserved.   |
| Bit 4 | –    | Reserved | 0       | Reserved.   |
| Bit 3 | –    | Reserved | 0       | Reserved.   |
| Bit 2 | –    | Reserved | 0       | Reserved.   |
| Bit 1 | –    | Reserved | 0       | Reserved.   |
| Bit 0 | –    | Reserved | 0       | Reserved.   |

**Byte 5: Control Register 5**

| Bit   | Pin# | Name     | Default | Description        |
|-------|------|----------|---------|--------------------|
| Bit 7 | –    | Reserved | 0       | Reserved.          |
| Bit 6 | –    | Reserved | 0       | Reserved.          |
| Bit 5 | –    | Reserved | 0       | Reserved.          |
| Bit 4 | –    | Reserved | 0       | Reserved.          |
| Bit 3 | –    | Reserved | 0       | Reserved.          |
| Bit 2 | –    | Reserved | 0       | Reserved.          |
| Bit 1 | 46   | REF1     | 1       | (Active/Inactive). |
| Bit 0 | 47   | REF0     | 1       | (Active/Inactive). |

**Byte 6: Watchdog Timer Register**

| Bit   | Name          | Default | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | PCI_Skew1     | 0       | PCI skew control.<br>00 = Normal.<br>01 = –500 ps.<br>10 = Reserved.<br>11 = +500 ps.                                                                                                                                                                                                                                                                                                                          |
| Bit 6 | PCI_Skew0     | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 5 | WD_TIMER4     | 1       |                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 4 | WD_TIMER3     | 1       |                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 3 | WD_TIMER2     | 1       | These bits store the time-out value of the Watchdog Timer. The scale of the timer is determined by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches “0,” it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled. |
| Bit 2 | WD_TIMER1     | 1       |                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 1 | WD_TIMER0     | 1       |                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 0 | WD_PRE_SCALER | 0       | 0 = 150 ms.<br>1 = 2.5 sec.                                                                                                                                                                                                                                                                                                                                                                                    |

**Byte 7: Control Register 7**

| Bit   | Pin# | Name         | Default | Pin Description           |
|-------|------|--------------|---------|---------------------------|
| Bit 7 | –    | Reserved     | 0       | Reserved.                 |
| Bit 6 | 25   | 24_48MHz_DRV | 1       | 0 = Norm, 1 = High Drive. |
| Bit 5 | 26   | 48MHz_DRV    | 1       | 0 = Norm, 1 = High Drive. |
| Bit 4 | –    | Reserved     | 0       | Reserved.                 |
| Bit 3 | –    | Reserved     | 0       | Reserved.                 |
| Bit 2 | –    | Reserved     | 0       | Reserved.                 |
| Bit 1 | –    | Reserved     | 0       | Reserved.                 |
| Bit 0 | –    | Reserved     | 0       | Reserved.                 |

**Byte 8: Vendor ID and Revision ID Register (Read Only)**

| Bit   | Name         | Default | Pin Description                                       |
|-------|--------------|---------|-------------------------------------------------------|
| Bit 7 | Revision_ID3 | 0       | Revision ID bit[3].                                   |
| Bit 6 | Revision_ID2 | 0       | Revision ID bit[2].                                   |
| Bit 5 | Revision_ID1 | 0       | Revision ID bit[1].                                   |
| Bit 4 | Revision_ID0 | 0       | Revision ID bit[0].                                   |
| Bit 3 | Vendor_ID3   | 1       | Bit[3] of Cypress's Vendor ID. This bit is read-only. |
| Bit 2 | Vendor_ID2   | 0       | Bit[2] of Cypress's Vendor ID. This bit is read-only. |
| Bit 1 | Vendor_ID1   | 0       | Bit[1] of Cypress's Vendor ID. This bit is read-only. |
| Bit 0 | Vendor_ID0   | 0       | Bit[0] of Cypress's Vendor ID. This bit is read-only. |

**Byte 9: System RESET and Watchdog Timer Register**

| Bit   | Name         | Default | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|--------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | SDRAM_DRV    | 0       | SDRAM clock output drive strength.<br>0 = Normal.<br>1 = High Drive.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 6 | PCI_DRV      | 0       | PCI clock output drive strength.<br>0 = Normal.<br>1 = High Drive.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Bit 5 | Reserved     | 0       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 4 | RST_EN_WD    | 0       | This bit will enable the generation of a Reset pulse when a Watchdog Timer time-out occurs.<br>0 = Disabled.<br>1 = Enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Bit 3 | RST_EN_FC    | 0       | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled.<br>1 = Enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Bit 2 | WD_TO_STATUS | 0       | Watchdog Timer Time-out Status bit.<br>0 = No time-out occurs (Read); Ignore (Write).<br>1 = Time-out occurred (Read); Clear WD_TO_STATUS (Write).                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Bit 1 | WD_EN        | 0       | 0 = Stop and reload Watchdog Timer. Unlock CY28316 from recovery frequency mode.<br>1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs.<br><b>Note:</b> CY28316 will generate a system Reset, reload a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog Timer time-out occurs. Under recovery frequency mode, CY28316 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28316 from its recovery frequency mode by clearing the WD_EN bit. |

**Byte 9: System RESET and Watchdog Timer Register (continued)**

| Bit   | Name       | Default | Pin Description                                                       |
|-------|------------|---------|-----------------------------------------------------------------------|
| Bit 0 | CPU0:1_DRV | 0       | CPU0:1 clock output drive strength.<br>0 = Normal.<br>1 = High Drive. |

**Byte 10: Skew Control Register**

| Bit   | Name         | Default | Description                                                                                                                                                                |
|-------|--------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | CPU0:1_Skew2 | 0       | CPU0:1 output skew control.<br>000 = Normal.<br>001 = -150 ps.<br>010 = -300 ps.<br>011 = -450 ps.<br>100 = +150 ps.<br>101 = +300 ps.<br>110 = +450 ps.<br>111 = +600 ps. |
| Bit 6 | CPU0:1_Skew1 | 0       |                                                                                                                                                                            |
| Bit 5 | CPU0:1_Skew0 | 0       |                                                                                                                                                                            |
| Bit 4 | Reserved     | 0       |                                                                                                                                                                            |
| Bit 3 | Reserved     | 0       | Reserved.                                                                                                                                                                  |
| Bit 2 | Reserved     | 0       | Reserved.                                                                                                                                                                  |
| Bit 1 | Reserved     | 0       | Reserved.                                                                                                                                                                  |
| Bit 0 | Reserved     | 0       | Reserved.                                                                                                                                                                  |

**Byte 11: Recovery Frequency N-Value Register**

| Bit   | Name         | Default | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|--------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | ROCV_FREQ_N7 | 0       | If ROCV_FREQ_SEL is set, CY28316 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU and PCI. When it is cleared, CY28316 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28316 will use the frequency ratio stated in the SEL[4:0] register. CY28316 supports programmable CPU frequencies ranging from 50 MHz to 248 MHz. CY28316 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] or ROCV_FREQ_M[6:0]. Therefore it is recommended to use word or block Write to update both registers within the same SMBus bus operation. |
| Bit 6 | ROCV_FREQ_N6 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Bit 5 | ROCV_FREQ_N5 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Bit 4 | ROCV_FREQ_N4 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Bit 3 | ROCV_FREQ_N3 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Bit 2 | ROCV_FREQ_N2 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Bit 1 | ROCV_FREQ_N1 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Bit 0 | ROCV_FREQ_N0 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Byte 12: Recovery Frequency M-Value Register**

| Bit   | Name          | Default | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | ROCV_FREQ_SEL | 0       | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0].<br>1 = From the settings of ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0].                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Bit 6 | ROCV_FREQ_M6  | 0       | If ROCV_FREQ_SEL is set, CY28316 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of the FS_Override bit determines the frequency ratio for CPU, SDRAM, and PCI. When it is cleared, CY28316 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28316 will use the frequency ratio stated in the SEL[4:0] register. CY28316 supports programmable CPU frequencies ranging from 50 MHz to 248 MHz. CY28316 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] or ROCV_FREQ_M[6:0]. Therefore, it is recommended to use word or block Write to update both registers within the same SMBus bus operation. |
| Bit 5 | ROCV_FREQ_M5  | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 4 | ROCV_FREQ_M4  | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 3 | ROCV_FREQ_M3  | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 2 | ROCV_FREQ_M2  | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 1 | ROCV_FREQ_M1  | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Bit 0 | ROCV_FREQ_M0  | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Byte 13: Programmable Frequency Select N-Value Register**

| Bit   | Name        | Default | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | CPU_FSEL_N7 | 0       | If Prog_Freq_EN is set, CY28316 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of the FS_Override bit determines the frequency ratio for CPU, SDRAM, and PCI. When it is cleared, CY28316 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28316 will use the frequency ratio stated in the SEL[4:0] register. CY28316 supports programmable CPU frequencies ranging from 50 MHz to 248 MHz. |
| Bit 6 | CPU_FSEL_N6 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 5 | CPU_FSEL_N5 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 4 | CPU_FSEL_N4 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 3 | CPU_FSEL_N3 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 2 | CPU_FSEL_N2 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 1 | CPU_FSEL_N1 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 0 | CPU_FSEL_N0 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Byte 14: Programmable Frequency Select M-Value Register**

| Bit   | Name        | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 7 | Pro_Freq_EN | 0       | Programmable output frequencies enabled.<br>0 = Disabled.<br>1 = Enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Bit 6 | CPU_FSEL_M6 | 0       | If Prog_Freq_EN is set, CY28316 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of the FS_Override bit determines the frequency ratio for CPU, SDRAM, and PCI. When it is cleared, CY28316 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28316 will use the frequency ratio stated in the SEL[4:0] register. CY28316 supports programmable CPU frequencies ranging from 50 MHz to 248 MHz. |
| Bit 5 | CPU_FSEL_M5 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 4 | CPU_FSEL_M4 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 3 | CPU_FSEL_M3 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 2 | CPU_FSEL_M2 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 1 | CPU_FSEL_M1 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bit 0 | CPU_FSEL_M0 | 0       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Byte 15: Reserved Register**

| Bit   | Pin# | Name             | Default | Description                |
|-------|------|------------------|---------|----------------------------|
| Bit 7 | –    | Reserved         | 0       | Reserved.                  |
| Bit 6 | –    | Reserved         | 0       | Reserved.                  |
| Bit 5 | –    | Reserved         | 0       | Reserved.                  |
| Bit 4 | –    | Reserved         | 0       | Reserved.                  |
| Bit 3 | –    | Reserved         | 0       | Reserved.                  |
| Bit 2 | –    | Vendor test mode | 0       | Reserved. Write with '0.'  |
| Bit 1 | –    | Vendor test mode | 1       | Test mode. Write with '1.' |
| Bit 0 | –    | Vendor test mode | 1       | Test mode. Write with '1.' |

**Byte 16: Reserved Register**

| Bit   | Pin# | Name     | Default | Description |
|-------|------|----------|---------|-------------|
| Bit 7 | –    | Reserved | 0       | Reserved.   |
| Bit 6 | –    | Reserved | 0       | Reserved.   |
| Bit 5 | –    | Reserved | 0       | Reserved.   |
| Bit 4 | –    | Reserved | 0       | Reserved.   |
| Bit 3 | –    | Reserved | 0       | Reserved.   |
| Bit 2 | –    | Reserved | 0       | Reserved.   |
| Bit 1 | –    | Reserved | 0       | Reserved.   |

**Byte 17: Reserved Register**

| Bit   | Pin# | Name     | Default | Description |
|-------|------|----------|---------|-------------|
| Bit 7 | –    | Reserved | 0       | Reserved.   |
| Bit 6 | –    | Reserved | 0       | Reserved.   |

**Byte 17: Reserved Register (continued)**

| Bit   | Pin# | Name     | Default | Description |
|-------|------|----------|---------|-------------|
| Bit 5 | –    | Reserved | 0       | Reserved.   |
| Bit 4 | –    | Reserved | 0       | Reserved.   |
| Bit 3 | –    | Reserved | 0       | Reserved.   |
| Bit 2 | –    | Reserved | 0       | Reserved.   |
| Bit 1 | -    | Reserved | 0       | Reserved.   |

**Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes**

| Input Conditions |             |             |             |             | Output Frequency |      | PLL Gear Constant (G) |
|------------------|-------------|-------------|-------------|-------------|------------------|------|-----------------------|
| FS4<br>SEL4      | FS3<br>SEL3 | FS2<br>SEL2 | FS1<br>SEL1 | FS0<br>SEL0 | CPU              | PCI  |                       |
| 0                | 0           | 0           | 0           | 0           | 200.0            | 33.3 | 48.000741             |
| 0                | 0           | 0           | 0           | 1           | 190.0            | 38.0 | 48.000741             |
| 0                | 0           | 0           | 1           | 0           | 180.0            | 36.0 | 48.000741             |
| 0                | 0           | 0           | 1           | 1           | 170.0            | 34.0 | 48.000741             |
| 0                | 0           | 1           | 0           | 0           | 166.0            | 33.2 | 48.000741             |
| 0                | 0           | 1           | 0           | 1           | 160.0            | 32.0 | 48.000741             |
| 0                | 0           | 1           | 1           | 0           | 150.0            | 37.5 | 48.000741             |
| 0                | 0           | 1           | 1           | 1           | 145.0            | 36.3 | 48.000741             |
| 0                | 1           | 0           | 0           | 0           | 140.0            | 35.0 | 48.000741             |
| 0                | 1           | 0           | 0           | 1           | 136.0            | 34.0 | 48.000741             |
| 0                | 1           | 0           | 1           | 0           | 130.0            | 32.5 | 48.000741             |
| 0                | 1           | 0           | 1           | 1           | 124.0            | 31.0 | 48.000741             |
| 0                | 1           | 1           | 0           | 0           | 67.2             | 33.6 | 48.000741             |
| 0                | 1           | 1           | 0           | 1           | 100.8            | 33.6 | 48.000741             |
| 0                | 1           | 1           | 1           | 0           | 118.0            | 39.3 | 48.000741             |
| 0                | 1           | 1           | 1           | 1           | 134.4            | 33.6 | 48.000741             |
| 1                | 0           | 0           | 0           | 0           | 67.0             | 33.5 | 48.000741             |
| 1                | 0           | 0           | 0           | 1           | 100.5            | 33.5 | 48.000741             |
| 1                | 0           | 0           | 1           | 0           | 115.0            | 38.3 | 48.000741             |
| 1                | 0           | 0           | 1           | 1           | 134.0            | 33.5 | 48.000741             |
| 1                | 0           | 1           | 0           | 0           | 66.8             | 33.4 | 48.000741             |
| 1                | 0           | 1           | 0           | 1           | 100.2            | 33.4 | 48.000741             |
| 1                | 0           | 1           | 1           | 0           | 110.0            | 36.7 | 48.000741             |
| 1                | 0           | 1           | 1           | 1           | 133.6            | 33.4 | 48.000741             |
| 1                | 1           | 0           | 0           | 0           | 105.0            | 35.0 | 48.000741             |
| 1                | 1           | 0           | 0           | 1           | 90.0             | 30.0 | 48.000741             |
| 1                | 1           | 0           | 1           | 0           | 85.0             | 28.3 | 48.000741             |
| 1                | 1           | 0           | 1           | 1           | 78.0             | 39.0 | 48.000741             |
| 1                | 1           | 1           | 0           | 0           | 66.6             | 33.3 | 48.000741             |
| 1                | 1           | 1           | 0           | 1           | 100.0            | 33.3 | 48.000741             |
| 1                | 1           | 1           | 1           | 0           | 75.0             | 37.5 | 48.000741             |
| 1                | 1           | 1           | 1           | 1           | 133.3            | 33.3 | 48.000741             |

## Programmable Output Frequency, Watchdog Timer, and Recovery Output Frequency Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency in the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism

when the system hangs or gets unstable. System BIOS or other control software can enable the Watchdog Timer before it attempts to make a frequency change. If the system hangs and a Watchdog Timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All the related registers are summarized in *Table 6*.

**Table 6. Register Summary**

| Name                                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pro_Freq_EN                           | Programmable output frequencies enabled.<br>0 = Disabled (default).<br>1 = Enabled.<br>When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If the FS_Override bit is set, the programmed value of SEL[4:0] will be used. When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M, and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs. |
| FS_Override                           | When Pro_Freq_EN is cleared or disabled,<br>0 = Select operating frequency by FS input pins (default).<br>1 = Select operating frequency by SEL bits in SMBus control bytes.<br>When Pro_Freq_EN is set or enabled,<br>0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default).<br>1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes.                                                                                                                                                                            |
| CPU_FSEL_N,<br>CPU_FSEL_M             | When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determine the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use word or block Write to update both registers within the same SMBus bus operation. The setting of the FS_Override bit determines the frequency ratio for CPU and PCI. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.                           |
| ROCV_FREQ_SEL                         | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0].<br>1 = From the settings of ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0].                                                                                                                                                                                                                                                                                                                                                                                                      |
| ROCV_FREQ_N[7:0],<br>ROCV_FREQ_M[6:0] | When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of the FS_Override bit determines the frequency ratio for CPU and SDRAM. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use word or block Write to update both registers within the same SMBus bus operation.                 |
| WD_EN                                 | 0 = Stop and reload Watchdog Timer. Unlock CY28316 from recovery frequency mode.<br>1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs.<br><b>Note:</b> CY28316 will generate system reset, reload a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog Timer time-out occurs. Under recovery frequency mode, CY28316 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28316 from its recovery frequency mode by clearing the WD_EN bit.                                                                                                                                             |
| WD_TO_STATUS                          | Watchdog Timer Time-out Status bit.<br>0 = No time-out occurs (Read); Ignore (Write).<br>1 = Time-out occurred (Read); Clear WD_TO_STATUS (Write).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 6. Register Summary**

| Name          | Description                                                                                                                                                                                                                                                                                                                                                        |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WD_TIMER[4:0] | These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit. |
| WD_PRE_SCALER | 0 = 150 ms.<br>1 = 2.5 sec.                                                                                                                                                                                                                                                                                                                                        |
| RST_EN_WD     | This bit will enable the generation of a Reset pulse when a watchdog timer time-out occurs.<br>0 = Disabled.<br>1 = Enabled.                                                                                                                                                                                                                                       |
| RST_EN_FC     | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled.<br>1 = Enabled.                                                                                                                                                                                                                                             |

### How to Program CPU Output Frequency?

When the programmable output frequency feature is enabled (Pro\_Freq\_EN bit is set), the CPU output frequency is determined by the following equation:

$$F_{cpu} = G * (N+3)/(M+3).$$

"N" and "M" are the values programmed in the Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 3*.

The ratio of (N+3) and (M+3) needs to be greater than "1"  $[(N+3)/(M+3) > 1]$ .

*Table* lists set of N and M values for different frequency output ranges. This example uses a fixed value for the M-Value Register and selects the CPU output frequency by changing the value of the N-Value Register.

**Table 7. Examples of N and M Value for Different CPU Frequency Range**

| Frequency Ranges  | Gear Constants | Fixed Value for M-Value Register | Range of N-Value Register for Different CPU Frequency |
|-------------------|----------------|----------------------------------|-------------------------------------------------------|
| 50 MHz – 129 MHz  | 48.00741       | 93                               | 97–255                                                |
| 130 MHz – 248 MHz | 48.00741       | 45                               | 127–245                                               |

## Absolute Maximum Ratings<sup>[2.]</sup>

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other condi-

tions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter        | Description                            | Rating       | Unit |
|------------------|----------------------------------------|--------------|------|
| $V_{DD}, V_{IN}$ | Voltage on any pin with respect to GND | -0.5 to +7.0 | V    |
| $T_{STG}$        | Storage Temperature                    | -65 to +150  | °C   |
| $T_B$            | Ambient Temperature under Bias         | -55 to +125  | °C   |
| $T_A$            | Operating Temperature                  | 0 to +70     | °C   |
| $ESD_{PROT}$     | Input ESD Protection                   | 2 (min.)     | kV   |

## DC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{DDQ3} = 3.3\text{V} \pm 5\%$ <sup>[3]</sup>

| Parameter                  | Description                                                  | Test Condition           | Min.                   | Typ. | Max.                  | Unit |    |
|----------------------------|--------------------------------------------------------------|--------------------------|------------------------|------|-----------------------|------|----|
| Supply Current             |                                                              |                          |                        |      |                       |      |    |
| I <sub>DD</sub>            | 3.3V Supply Current                                          |                          |                        | 260  |                       | mA   |    |
| I <sub>DD</sub>            | 2.5V Supply Current                                          |                          |                        | 25   |                       | mA   |    |
| Logic Inputs               |                                                              |                          |                        |      |                       |      |    |
| V <sub>IL</sub>            | Input Low Voltage                                            |                          | GND – 0.3              |      | 0.8                   | V    |    |
| V <sub>IH</sub>            | Input High Voltage                                           |                          | 2.0                    |      | V <sub>DD</sub> + 0.3 | V    |    |
| I <sub>IL</sub>            | Input Low Current <sup>[4]</sup>                             |                          |                        |      | –25                   | μA   |    |
| I <sub>IH</sub>            | Input High Current <sup>[4]</sup>                            |                          |                        |      | 10                    | μA   |    |
| Clock Outputs              |                                                              |                          |                        |      |                       |      |    |
| V <sub>OL</sub>            | Output Low Voltage                                           | I <sub>OL</sub> = 1 mA   |                        |      | 50                    | mV   |    |
| V <sub>OH</sub>            | Output High Voltage                                          | I <sub>OH</sub> = –1 mA  | 3.1                    |      |                       | V    |    |
| I <sub>OL</sub>            | Output Low Current                                           | PCI                      | V <sub>OL</sub> = 1.5V | 70   | 110                   | 135  | mA |
|                            |                                                              | REF                      | V <sub>OL</sub> = 1.5V | 50   | 70                    | 100  | mA |
|                            |                                                              | 48 MHz                   | V <sub>OL</sub> = 1.5V | 50   | 70                    | 100  | mA |
|                            |                                                              | 24 MHz                   | V <sub>OL</sub> = 1.5V | 50   | 70                    | 100  | mA |
|                            |                                                              | SDRAM                    | V <sub>OL</sub> = 1.5V | 70   | 110                   | 135  | mA |
| I <sub>OH</sub>            | Output High Current                                          | PCI                      | V <sub>OH</sub> = 1.5V | 70   | 110                   | 135  | mA |
|                            |                                                              | REF                      | V <sub>OH</sub> = 1.5V | 50   | 70                    | 100  | mA |
|                            |                                                              | 48 MHz                   | V <sub>OH</sub> = 1.5V | 50   | 70                    | 100  | mA |
|                            |                                                              | 24 MHz                   | V <sub>OH</sub> = 1.5V | 50   | 70                    | 100  | mA |
|                            |                                                              | SDRAM                    | V <sub>OH</sub> = 1.5V | 70   | 110                   | 135  | mA |
| Crystal Oscillator         |                                                              |                          |                        |      |                       |      |    |
| V <sub>TH</sub>            | X1 Input Threshold Voltage <sup>[5]</sup>                    | V <sub>DDQ3</sub> = 3.3V |                        | 1.65 |                       | V    |    |
| C <sub>LOAD</sub>          | Load Capacitance, Imposed on External Crystal <sup>[6]</sup> |                          |                        | 18   |                       | pF   |    |
| C <sub>IN,X1</sub>         | X1 Input Capacitance <sup>[7]</sup>                          | Pin X2 unconnected       |                        | TBD  |                       | pF   |    |
| Pin Capacitance/Inductance |                                                              |                          |                        |      |                       |      |    |
| C <sub>IN</sub>            | Input Pin Capacitance                                        | Except X1 and X2         |                        |      | 5                     | pF   |    |
| C <sub>OUT</sub>           | Output Pin Capacitance                                       |                          |                        |      | 6                     | pF   |    |
| L <sub>IN</sub>            | Input Pin Inductance                                         |                          |                        |      | 7                     | nH   |    |

### Notes:

2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

3. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.

4. CY28316 logic inputs (except FS3) have internal pull-up devices (pull-ups not full CMOS level). Logic input FS3 has an internal pull-down device.

5. X1 input threshold voltage (typical) is  $V_{DD}/2$ .

6. The CY28316 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. The total load placed on the crystal is 18 pF; this includes typical stray capacitance of short PCB traces to the crystal.

7. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

**AC Electrical Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$ )

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum is disabled.

**CPU Clock Outputs (CPUT0, CPUC0, CPU\_CS)<sup>[8]</sup>**

| Parameter | Description                                        | Test Condition/Comments                                                                                             | CPU = 100 MHz |      |      | CPU = 133 MHz |      |      | Unit     |
|-----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|---------------|------|------|---------------|------|------|----------|
|           |                                                    |                                                                                                                     | Min.          | Typ. | Max. | Min.          | Typ. | Max. |          |
| $t_R$     | Output Rise Edge Rate                              |                                                                                                                     | 1.0           |      | 4.0  | 1.0           |      | 4.0  | V/ns     |
| $t_F$     | Output Fall Edge Rate                              |                                                                                                                     | 1.0           |      | 4.0  | 1.0           |      | 4.0  | V/ns     |
| $t_D$     | Duty Cycle                                         | Measured at 50% point                                                                                               | 45            |      | 55   | 45            |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle to Cycle                             |                                                                                                                     |               |      | 375  |               |      | 375  | ps       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |               | 3    |      |               | 3    |      | ms       |
| $Z_o$     | AC Output Impedance                                | $V_O = V_X$                                                                                                         |               | 50   |      |               | 50   |      | $\Omega$ |

**PCI Clock Outputs, PCI0:5 (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description                                        | Test Condition/Comments                                                                                             | Min. | Typ. | Max. | Unit     |
|-----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $t_P$     | Period                                             | Measured on the rising edge at 1.5V                                                                                 | 30   |      |      | ns       |
| $t_H$     | High Time                                          | Duration of clock cycle above 2.4V                                                                                  | 12   |      |      | ns       |
| $t_L$     | Low Time                                           | Duration of clock cycle below 0.4V                                                                                  | 12   |      |      | ns       |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1    |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1    |      | 4    | V/ns     |
| $t_D$     | Duty Cycle                                         | Measured on the rising and falling edges at 1.5V                                                                    | 45   |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle-to-Cycle                             | Measured on the rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                  |      |      | 250  | ps       |
| $t_{SK}$  | Output Skew                                        | Measured on the rising edge at 1.5V                                                                                 |      |      | 500  | ps       |
| $t_O$     | CPU to PCI Clock Skew                              | Covers all CPU/PCI outputs. Measured on the rising edge at 1.5V. CPU leads PCI output.                              | 1.5  |      | 4    | ns       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 30   |      | $\Omega$ |

**REF0:1 Clock Outputs (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description                                        | Test Condition/Comments                                                                                             | Min. | Typ.   | Max. | Unit     |
|-----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|------|--------|------|----------|
| $f$       | Frequency, Actual                                  | Frequency generated by the crystal oscillator                                                                       |      | 14.318 |      | MHz      |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 0.5  |        | 2    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 0.5  |        | 2    | V/ns     |
| $t_D$     | Duty Cycle                                         | Measured on the rising and falling edges at 1.5V                                                                    | 45   |        | 55   | %        |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |        | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 40     |      | $\Omega$ |

**Note:**

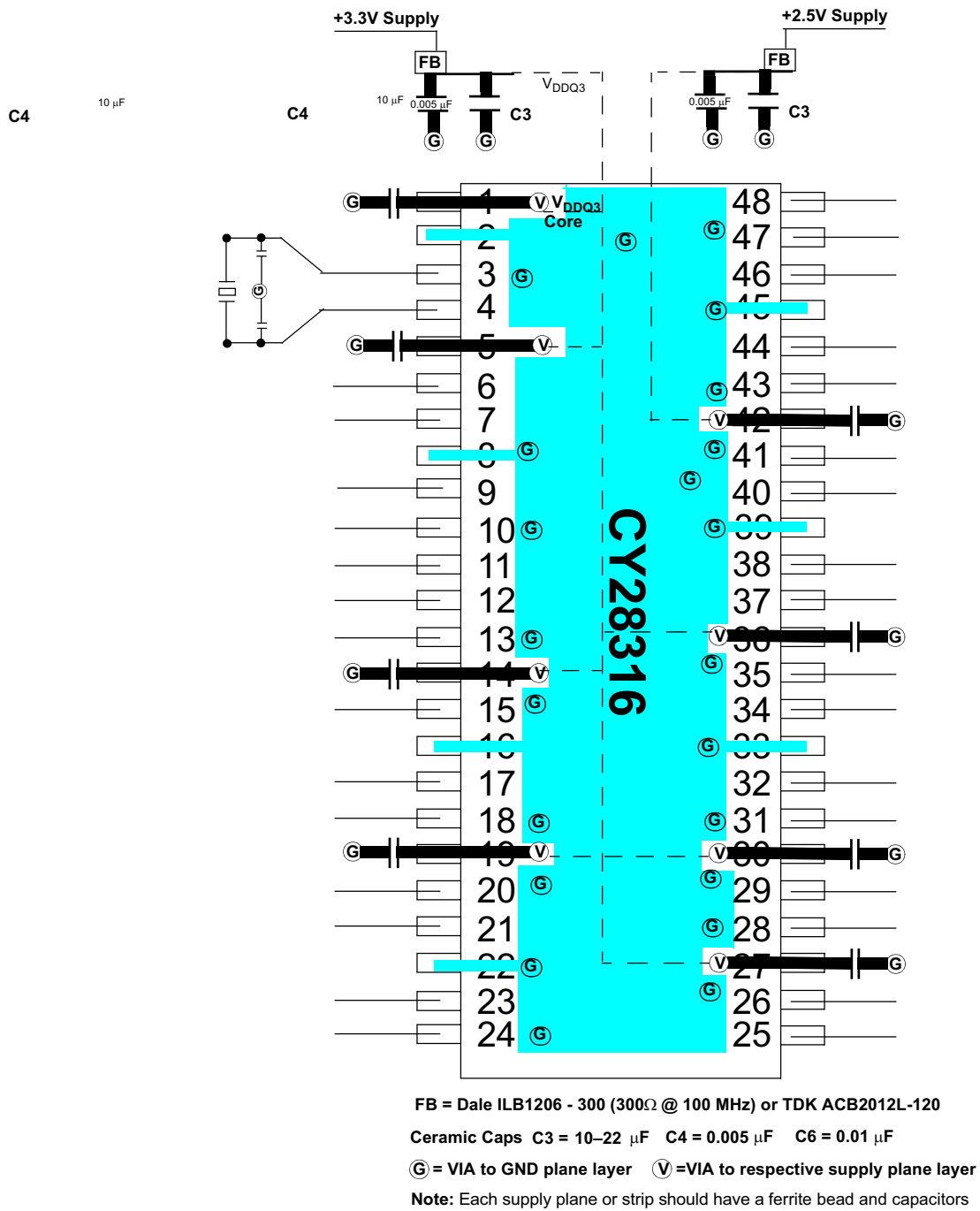
8. Refer to Figure 1 for K7 operation clock driver test circuit.

**48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | Min.   | Typ. | Max. | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|--------|------|------|------|
| f               | Frequency, Actual                                  | Determined by PLL divider ratio (see m/n below)                                                                     | 48.008 |      |      | MHz  |
| f <sub>D</sub>  | Deviation from 48 MHz                              | (48.008 – 48)/48                                                                                                    | +167   |      |      | ppm  |
| m/n             | PLL Ratio                                          | (14.31818 MHz × 57/17 = 48.008 MHz)                                                                                 | 57/17  |      |      |      |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 0.5    |      | 2    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 0.5    |      | 2    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on the rising and falling edges at 1.5V                                                                    | 45     |      | 55   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |        |      | 3    | ms   |
| Z <sub>o</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |        | 40   |      | Ω    |

**24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | Min.   | Typ. | Max. | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|--------|------|------|------|
| f               | Frequency, Actual                                  | Determined by PLL divider ratio (see m/n below)                                                                     | 24.004 |      |      | MHz  |
| f <sub>D</sub>  | Deviation from 24 MHz                              | (24.004 – 24)/24                                                                                                    | +167   |      |      | ppm  |
| m/n             | PLL Ratio                                          | (14.31818 MHz × 57/34 = 24.004 MHz)                                                                                 | 57/34  |      |      |      |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 0.5    |      | 2    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 0.5    |      | 2    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on the rising and falling edges at 1.5V                                                                    | 45     |      | 55   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |        |      | 3    | ms   |
| Z <sub>o</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |        | 40   |      | Ω    |

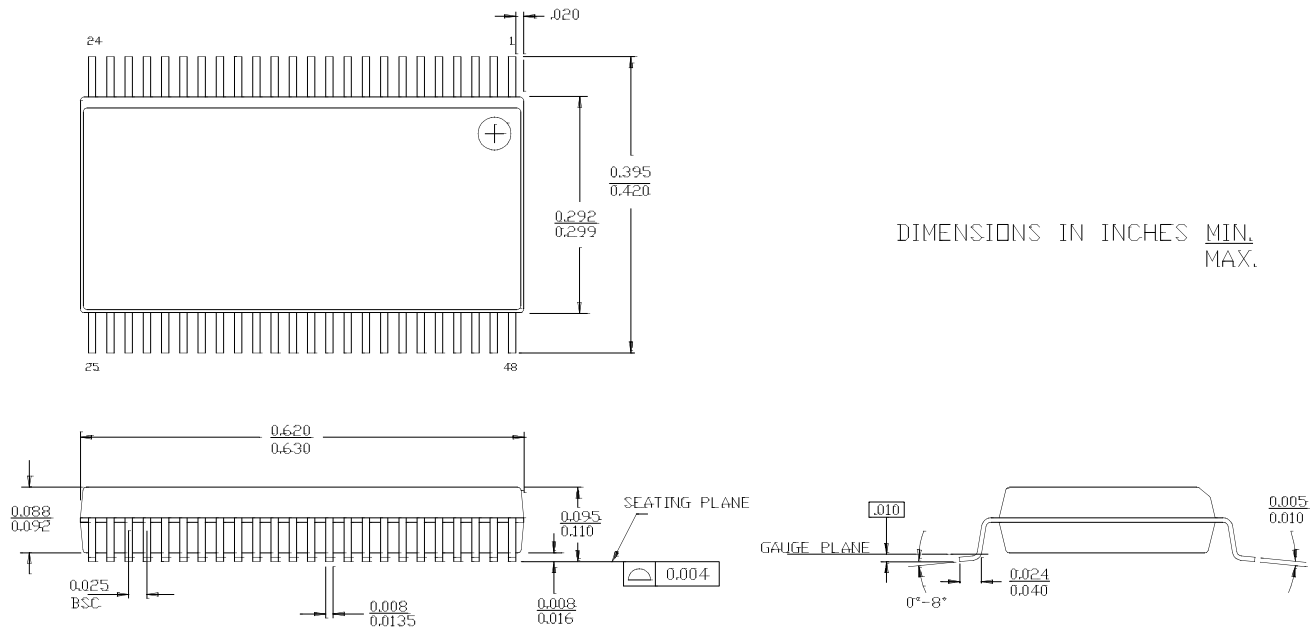
**Layout Diagram**


## Ordering Information

| Ordering Code | Package Type                           | Operating Range          |
|---------------|----------------------------------------|--------------------------|
| CY28316PVC    | 48-pin SSOP (300 mils)                 | Commercial, 0°C to +70°C |
| CY28316PVCT   | 48-pin SSOP (300 mils) – Tape and Reel | Commercial, 0°C to +70°C |

## Package Drawing and Dimensions

### 48-lead Shrink Small Outline Package O48



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