

OKI Semiconductor

MSM6778B

120-DOT COMMON DRIVER (TAB)

GENERAL DESCRIPTION

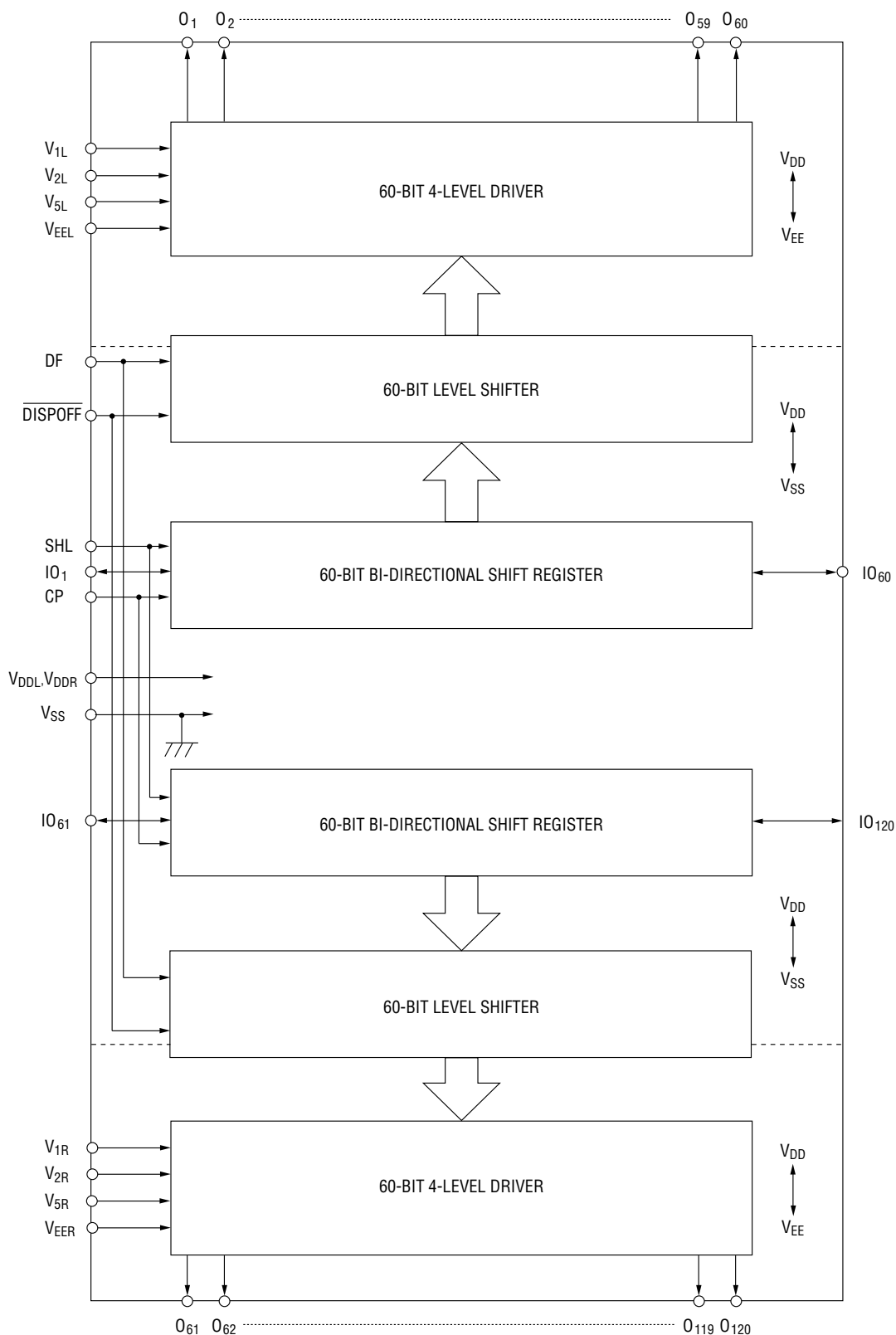
The MSM6778B is a dot-matrix LCD common driver. Fabricated in CMOS technology, the device contains two 60-bit bidirectional shift registers, two 60-bit level shifters, and two 60-bit 4-level drivers.

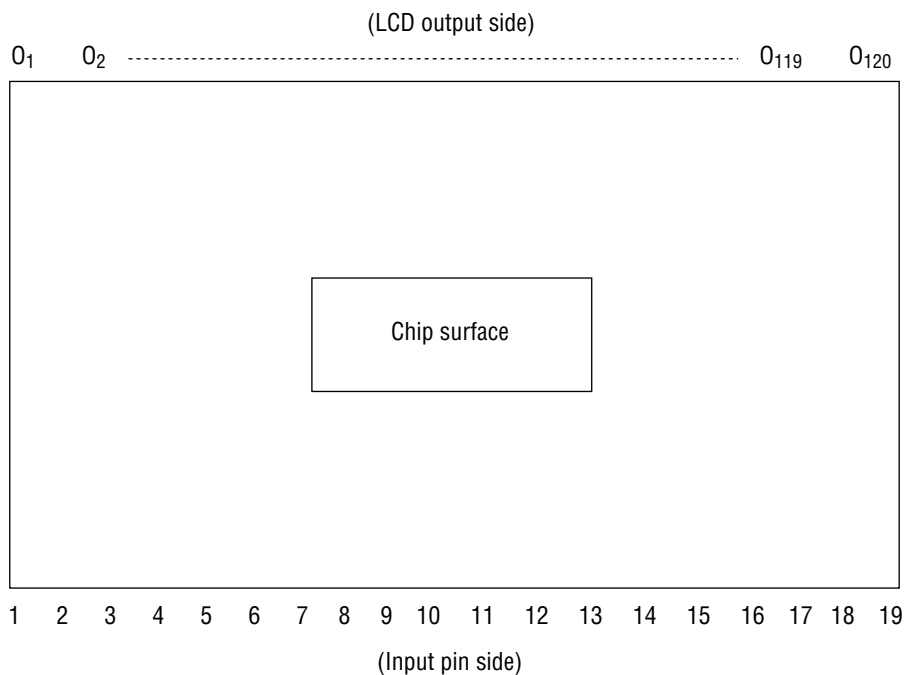
The MSM6778B has 120 LCD outputs. The number of LCD outputs can be increased by cascading MSM6778B devices, using cascade-connected I/O pins. The bias voltage which specifies a drive level can optionally be supplied externally. The MSM6778B is suitable for various types of LCD panel.

FEATURES

- Logic supply voltage : 2.7 V to 5.5 V
- LCD drive voltage : A wide range from 18 V to 28 V
- Applicable LCD duty : 1/100 to 1/256
- The bias voltage can be externally supplied.
- Structure:
 - 35mm-wide Tape Automated Bonding (TAB) film (Product name: MSM6778BAV-Z-01)
 - Tin-plating

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)**Input Pin Name**

Pin	Symbol	Pin	Symbol
1	V _{1L}	11	IO ₆₁
2	V _{2L}	12	IO ₁₂₀
3	V _{5L}	13	DF
4	V _{EEL}	14	CP
5	V _{DDL}	15	V _{DDR}
6	SHL	16	V _{EER}
7	V _{SS}	17	V _{5R}
8	DISPOFF	18	V _{2R}
9	IO ₁	19	V _{1R}
10	IO ₆₀		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage (1)	V_{DD}	$T_a=25^{\circ}\text{C}$	-0.3 to +6.5	V
Power Supply Voltage (2)	$V_{DD}-V_{EE}^{*}$	$T_a=25^{\circ}\text{C}$	0 to 30	V
Input Voltage	V_I	$T_a=25^{\circ}\text{C}$	-0.3 to $V_{DD}+0.3$	V
Storage Temperature	T_{STG}	—	-30 to +85	$^{\circ}\text{C}$

* $V_1 > V_2 > V_5 > V_{EE}$, $V_{DD} \geq V_1 > V_2 \geq V_{DD}-10\text{V}$, $V_{EE}+10\text{V} \geq V_5 > V_{EE}$
 $V_{DD}=V_{DDL}=V_{DDR}$, $V_1=V_{1L}=V_{1R}$, $V_2=V_{2L}=V_{2R}$, $V_5=V_{5L}=V_{5R}$, $V_{EE}=V_{EEL}=V_{EER}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage (1)	V_{DD}	—	2.7 to 5.5	V
Power Supply Voltage (2)	$V_{DD}-V_{EE}^{*}$	No load	14 to 28	V
		During liquid crystal driving	18 to 28	V
Operating temperature	T_{op}	—	-20 to +75	$^{\circ}\text{C}$

* $V_1 > V_2 > V_5 > V_{EE}$, $V_{DD} \geq V_1 > V_2 \geq V_{DD}-7\text{V}$, $V_{EE}+7\text{V} \geq V_5 > V_{EE}$
 $V_{DD}=V_{DDL}=V_{DDR}$, $V_1=V_{1L}=V_{1R}$, $V_2=V_{2L}=V_{2R}$, $V_5=V_{5L}=V_{5R}$, $V_{EE}=V_{EEL}=V_{EER}$

Note: Unlike mold packages, The Tape Carrier Package (TCP) cannot shield a light. Please shield a light to secure the electrical characteristics.

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD}=2.7$ to 5.5V , $T_a=-20$ to $+75^{\circ}\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}^{*1}	—	$0.8 V_{DD}$	—	—	V
"L" Input Voltage	V_{IL}^{*1}	—	—	—	$0.2 V_{DD}$	V
"H" Input Current	I_{IH}^{*1}	$V_I=V_{DD}$, $V_{DD}=5.5\text{V}$	—	—	1	μA
"L" Input Current	I_{IL}^{*1}	$V_I=0\text{V}$, $V_{DD}=5.5\text{V}$	—	—	-1	μA
"H" Output Voltage	V_{OH}^{*2}	$I_O=-0.2\text{mA}$, $V_{DD}=2.7\text{V}$	$V_{DD}-0.4$	—	—	V
"L" Output Voltage	V_{OL}^{*2}	$I_O=0.2\text{mA}$, $V_{DD}=2.7\text{V}$	—	—	0.4	V
ON Resistance	R_{ON}^{*4}	$V_{DD}-V_{EE}=25\text{V}$, *3 $I_{V_N-V_O}=0.25\text{V}$	—	—	2.0	$\text{k}\Omega$
Supply Current	I_{DD}^{*5}	$CP=28\text{kHz}$, $V_{DD}=3.0\text{V}$	—	—	60	μA
	I_{EE}^{*5}	$V_{DD}-V_{EE}=25\text{V}$, No load	—	—	400	μA
Input Capacitance	C_I	$f=1\text{MHz}$	—	—	—	pF

*1 Applicable to pins CP, IO₁, IO₆₀, IO₆₁, IO₁₂₀, SHL, DF, $\overline{\text{DISPOFF}}$

*2 Applicable to pins IO₁, IO₆₀, IO₆₁, IO₁₂₀

*3 $V_N=V_1$, V_2 , V_5 , V_{EE} , $V_2=1/16 (V_{DD}-V_{EE})$, $V_5=15/16 (V_{DD}-V_{EE})$

*4 Applicable to pins O₁ to O₁₂₀

*5 I_{DD} shows the supply current between V_{DD} and V_{SS} . I_{EE} shows the supply current between V_{DD} and V_{EE} .

Note: The above values are guaranteed when TCP is protected from light.

Switching Characteristics

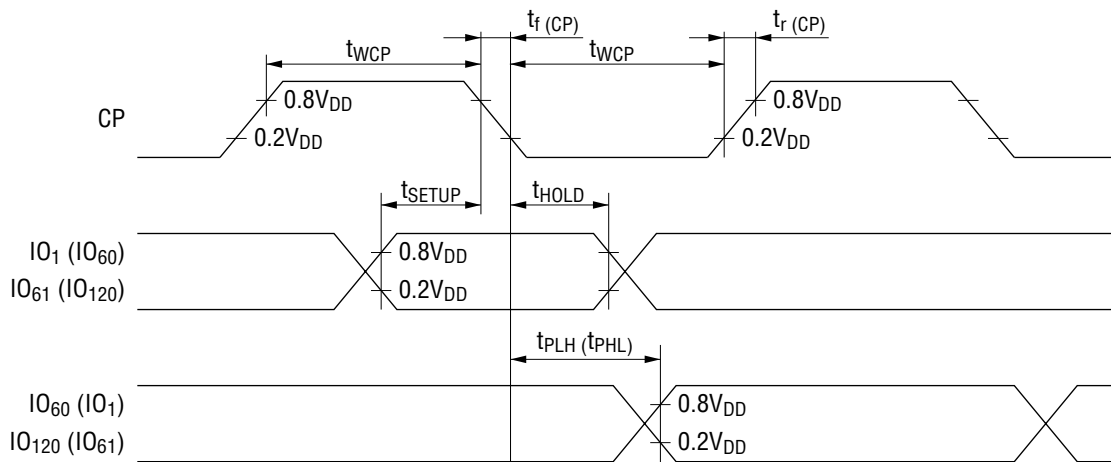
(V_{DD}=2.7 to 5.5 V, T_a= -20 to +75°C, C_L=15 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
IO ₁ , IO ₆₁ (IO ₆₀ , IO ₁₂₀) "H", "L" Propagation Delay Time	t _{PLH} t _{PHL}	—	*1	—	3	μs
Clock Frequency	f _{CP}	—	—	—	1	MHz
CP Pulse Width	t _{WCP}	—	45	—	—	ns
Data Setup Time IO ₁ , IO ₆₁ → CP (IO ₆₀ , IO ₁₂₀ → CP)	t _{SETUP}	—	70	—	—	ns
Data Hold Time CP → IO ₁ , IO ₆₁ (CP → IO ₆₀ , IO ₁₂₀)	t _{HOLD}	—	70	—	—	ns
CP Rise, Fall Time	t _r (CP) t _f (CP)	—	—	—	20	ns

*1 The relationship between t_{PLH} (t_{PLH}) Min. and t_{HOLD} Min. satisfies the operation in a cascade connection state.

Note 1: When display is controlled by DISPOFF pin, CP rise and fall time must be ≤ 1 μs.

Note 2: The above values are guaranteed when TCP is protected from light.



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **IO₁, IO₆₀, IO₆₁, IO₁₂₀**

These are I/O pins of the two 60-bit bidirectional shift registers.

- **SHL**

This pin selects the shift direction of the two 60-bit bidirectional shift registers. Set this pin to "H" or "L" level during power-on.

SHL	Shift Direction	I/O pins		Function
L	O ₁ → O ₆₀	IO ₁ , IO ₆₁	Input	IO ₁ and IO ₆₁ are data input pins for the shift register. The entered data is read in at the falling edge of a clock pulse. The data is output from IO ₆₀ and IO ₁₂₀ behind the number of bits (60) of the shift register.
	O ₆₁ → O ₁₂₀	IO ₆₀ , IO ₁₂₀	Output	
H	O ₆₀ → O ₁	IO ₆₀ , IO ₁₂₀	Input	IO ₆₀ and IO ₁₂₀ are data input pins for the shift register. The entered data is read in at the falling edge of a clock pulse. The data is output from IO ₁ and IO ₆₁ behind the number of bits (60) of the shift register.
	O ₁₂₀ → O ₆₁	IO ₁ , IO ₆₁	Output	

- **CP**

This is a clock pulse input for the two 60-bit bidirectional shift registers. Scan data is shifted at the falling edge of a clock pulse.

- **DF**

This is a synchronous signal input for alternate signal for LCD driving.

- **DISPOFF**

This is an input used to control the output levels of O₁ to O₁₂₀. During low level input, the V₁ level is output from the output pins O₁ to O₁₂₀ independently of the data of the shift register. See the truth table.

- **O₁ to O₁₂₀**

These are outputs for the 4-level drivers, which correspond directly to each bit of the shift register. One of the four levels V₁, V₂, V₅, and V_{EE} is selected and output depending on the combination of the shift register data and a DF signal. See the Truth Table.

- **V_{1L}, V_{2L}, V_{5L}, V_{EE}L, V_{1R}, V_{2R}, V_{5R}, V_{EE}R**

These are LCD drive bias voltage inputs.

- **V_{DDL}, V_{DDR}, V_{SS}**

These are power supply pins for the device. V_{DD} is usually from 2.7 V to 5.5 V and V_{SS} is 0 V.

Truth Table

DF	SHIFT REGISTER DATA	DISPOFF	DRIVER OUTPUT (O ₁ to O ₁₂₀)
L	L	H	V ₂
L	H	H	V _{EE}
H	L	H	V ₅
H	H	H	V ₁
X	X	L	V ₁

X : Don't care

NOTES ON USE (when turning the power ON or OFF)

The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC.

Be sure to follow the sequence below when turning the power ON or OFF.

Power ON : Logic circuits ON → LCD drivers ON, or both ON at a time

Power OFF : LCD drivers OFF → logic circuits OFF, or both OFF at a time

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