

DTC144TT1

Preferred Devices

Bias Resistor Transistor

NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-59 package which is designed for low power surface mount applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- ESD Rating: Human Body Model: Class 1
Machine Model: Class B
- The SC-59 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Pb-Free Package is Available

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW $^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	540 (Note 1) 370 (Note 2)	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	264 (Note 1) 287 (Note 2)	$^\circ\text{C/W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

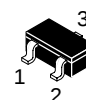
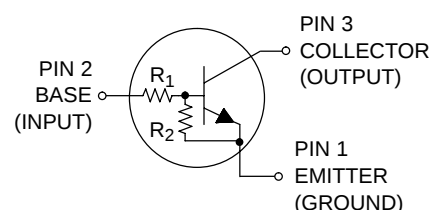
1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad



ON Semiconductor®

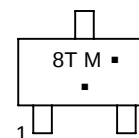
<http://onsemi.com>

NPN SILICON BIAS RESISTOR TRANSISTOR



SC-59
CASE 318D
STYLE 1

MARKING DIAGRAM



8T = Specific Device Code
M = Date Code*
■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

DTC144TT1

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping [†]
DTC144TT1	8T	47	∞	SC-59	3000/Tape & Reel
DTC144TT1G	8T	47	∞	SC-59 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V _{CE} = 50 V, I _B = 0)	I _{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0)	I _{EBO}	–	–	0.2	mAdc
Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	–	–	Vdc

ON CHARACTERISTICS (Note 3)

DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	h _{FE}	160	350	–	
Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 1 mA)	V _{CE(sat)}	–	–	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 3.5 V, R _L = 1.0 kΩ)	V _{OL}	–	–	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.25 V, R _L = 1.0 kΩ)	V _{OH}	4.9	–	–	Vdc
Input Resistor	R ₁	32.9	47	61.1	kΩ

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

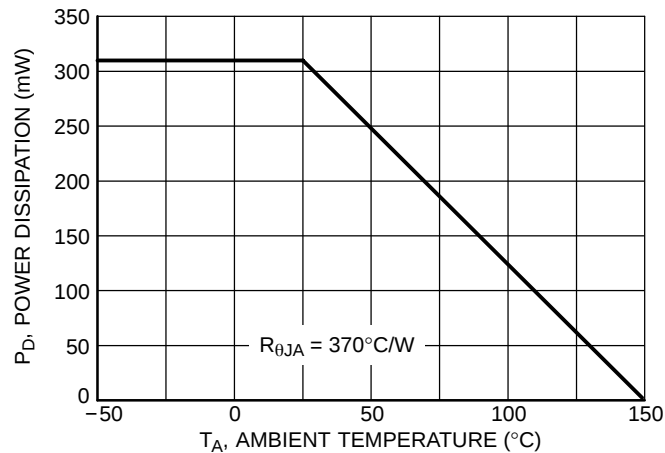


Figure 1. Derating Curve

TYPICAL APPLICATIONS FOR NPN BRTs

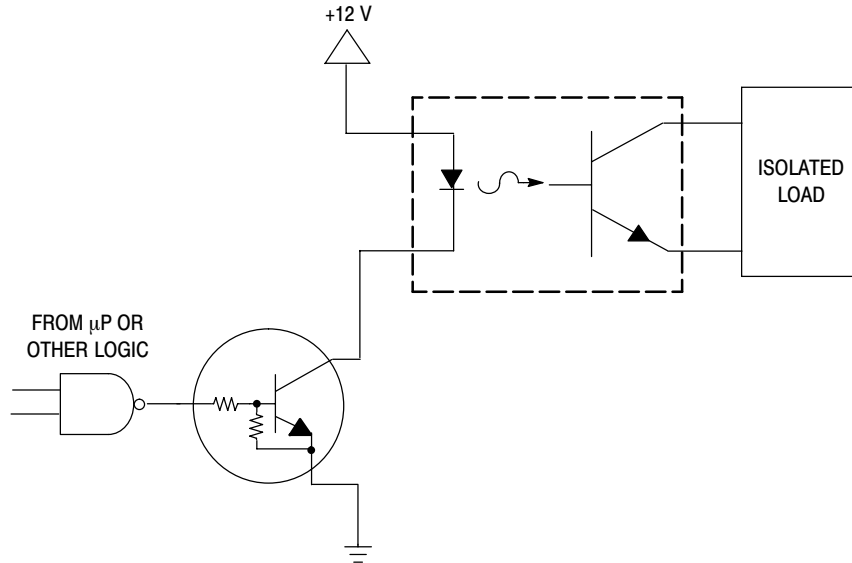


Figure 2. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

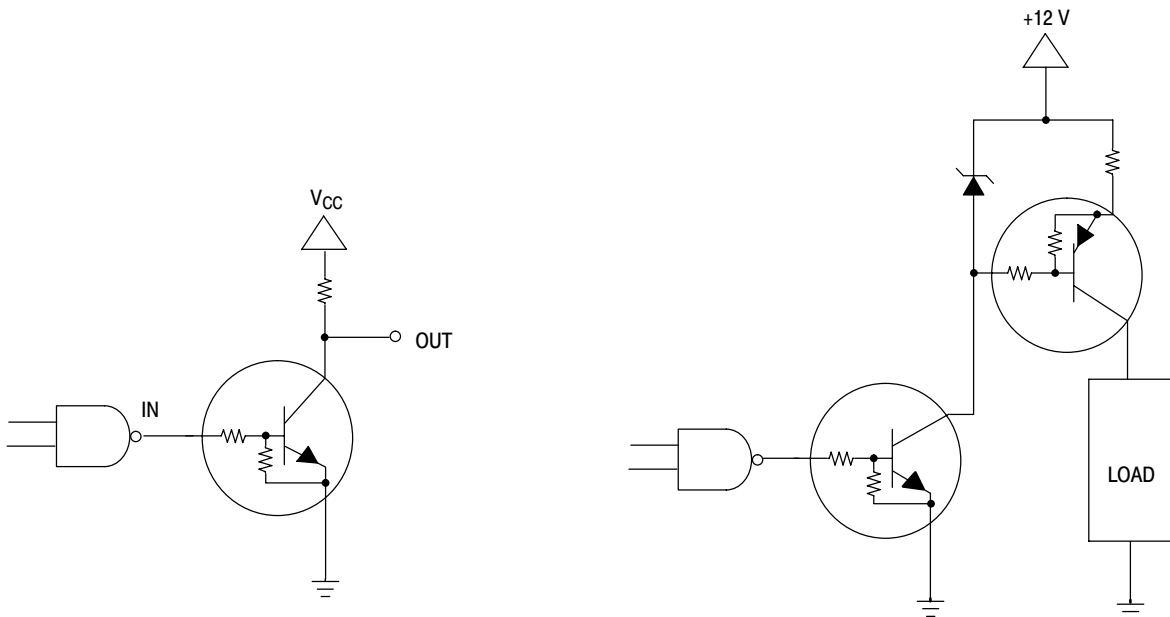


Figure 3. Open Collector Inverter:
Inverts the Input Signal

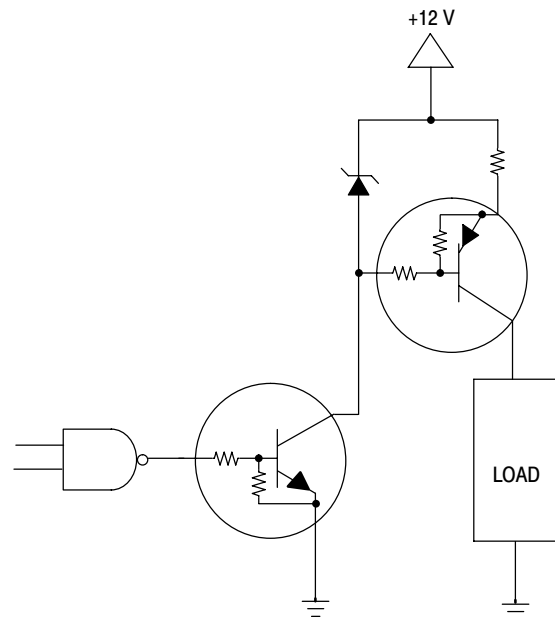
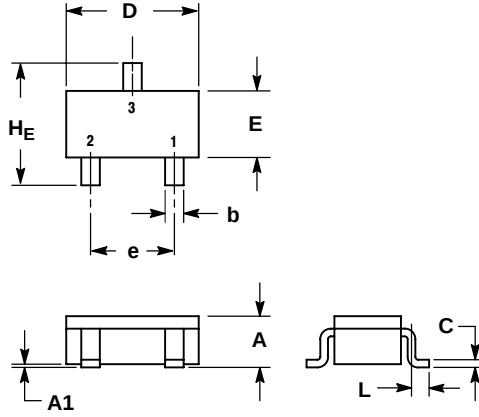


Figure 4. Inexpensive, Unregulated Current Source

DTC144TT1

PACKAGE DIMENSIONS

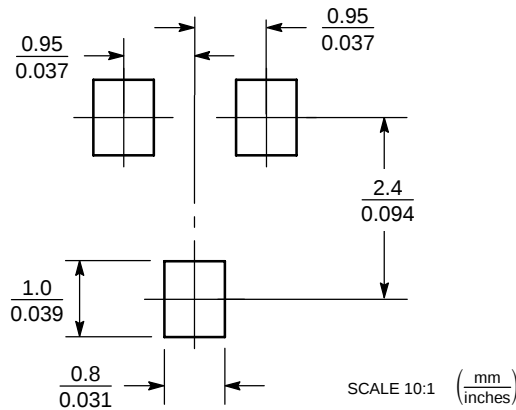
SC-59
CASE 318D-04
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.15	1.30	0.039	0.045	0.051
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.35	0.43	0.50	0.014	0.017	0.020
c	0.09	0.14	0.18	0.003	0.005	0.007
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	1.70	1.90	2.10	0.067	0.075	0.083
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.80	3.00	0.099	0.110	0.118

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.