# MIC4120/4129

## 6A-Peak Low-Side MOSFET Driver

## Bipolar/CMOS/DMOS Process

## General Description

MIC4120 and MIC4129 MOSFET drivers are resilient, efficient, and easy to use. The MIC4129 is an inverting driver, while the MIC4120 is a non-inverting driver. The MIC4120 and MIC4129 are improved versions of the MIC4420 and MIC4429.

The drivers are capable of 6A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4120/4129 accept any logic input from 2.4V to $V_S$ without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4120/4129 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern BiCMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability insures adequate gate voltage to the MOSFET during power up/down sequencing.

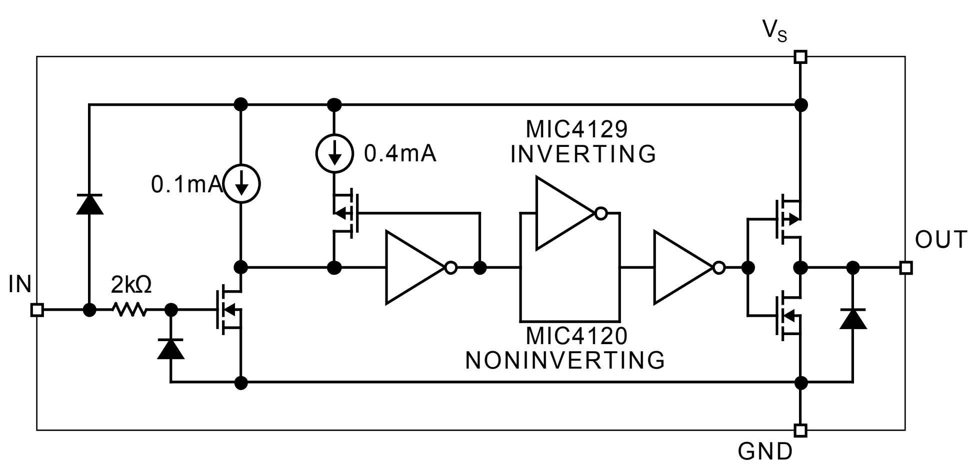
## Features

- CMOS Construction
- Latch-Up Protected: Will Withstand >200mA Reverse Output Current
- Logic Input Withstands Negative Swing of Up to 5V
- Matched Rise and Fall Times ................................ 25ns
- High Peak Output Current .............................. 6A Peak
- Wide Operating Range .............................. 4.5V to 20V
- High Capacitive Load Drive ........................... 10,000pF
- Low Delay Time ............................................ 55ns Typ
- Logic High Input for Any Voltage From 2.4V to $V_S$
- Low Equivalent Input Capacitance (typ) ................. 6pF
- Low Supply Current ............... 450µA With Logic 1 Input
- Low Output Impedance ....................................... 2.5Ω
- Output Voltage Swing Within 25mV of Ground or $V_S$
- Exposed backside pad packaging reduces heat
  - ePAD SOIC-8L ($\theta_{JA}$ = 58°C/W)
  - 3mm x 3mm MFL™-8L ($\theta_{JA}$ = 60°C/W)

## Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class-D Switching Amplifiers

## Functional Diagram

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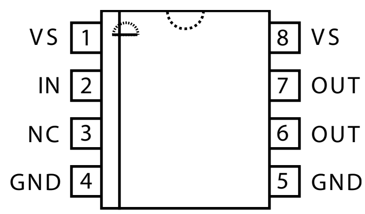
## Ordering Information

| Part Number | Package | Configuration | Lead Finish |
|---|---|---|---|
| MIC4120YME | EPAD 8-Pin SOIC | Non-Inverting | Pb-Free |
| MIC4120YML | 8-Pin MLF | Non-Inverting | Pb-Free |
| MIC4129YME | EPAD 8-Pin SOIC | Inverting | Pb-Free |
| MIC4129YML | 8-Pin MLF | Inverting | Pb-Free |

## Pin Configurations




**EPAD SOIC-8 (ME)**
**MLF-8 (ML)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 2 | IN | Control Input |
| 4, 5 | GND | Ground: Duplicate pins must be externally connected together |
| 1, 8 | VS | Supply Input: Duplicate pins must be externally connected together |
| 6, 7 | OUT | Output: Duplicate pins must be externally connected together |
| 3 | NC | Not connected |
| EP | GND | Ground: Backside |

## Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage ........................................................24V
Input Voltage ............................. $V_S$ + 0.3V to GND – 5V
Input Current ($V_{IN} > V_S$) ........................................50mA
Storage Temperature............................–65°C to +150°C
Lead Temperature (10 sec.) .................................. 300°C
ESD Rating, **Note 4**

## Operating Ratings

Supply Voltage ............................................ 4.5V to 20V
Junction Temperature...........................–40°C to +125°C
Package Thermal Resistance
3x3 MLF™ ($\theta_{JA}$) ...............................................60°C/W
EPAD SOIC-8 ($\theta_{JA}$) ........................................58°C/W

## Electrical Characteristics: ($T_A$ = 25°C with 4.5V ≤ $V_S$ ≤ 20V unless otherwise specified. Note 3.) Input Voltage slew rate >1V/µs

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $V_{IH}$ | Logic 1 Input Voltage | | **2.4** | 1.9 | | V |
| $V_{IL}$ | Logic 0 Input Voltage | | | 1.5 | **0.8** | V |
| $V_{IN}$ | Input Voltage Range | | –5 | | $V_S$ + 0.3 | V |
| $I_{IN}$ | Input Current | 0 V ≤ $V_{IN}$ ≤ $V_S$ | –10 | | 10 | µA |
| **OUTPUT** | | | | | | |
| $V_{OH}$ | High Output Voltage | See Figure 1 | **$V_S$–0.025** | | | V |
| $V_{OL}$ | Low Output Voltage | See Figure 1 | | | **0.025** | V |
| $R_O$ | Output Resistance, Output Low | $I_{OUT}$ = 10 mA, $V_S$ = 20 V | | 1.4 | **5** | Ω |
| $R_O$ | Output Resistance, Output High | $I_{OUT}$ = 10 mA, $V_S$ = 20 V | | 1.5 | **5** | Ω |
| $I_{PK}$ | Peak Output Current | $V_S$ = 20 V (See Figure 6) | | 6 | | A |
| $I_R$ | Latch-Up Protection Withstand Reverse Current | | 200 | | | mA |
| **SWITCHING TIME** | | | | | | |
| $t_R$ | Rise Time | Test Figure 1, $C_L$ = 2200 pF | | 12 | 30<br>**35** | ns<br>ns |
| $t_F$ | Fall Time | Test Figure 1, $C_L$ = 2200 pF | | 13 | 30<br>**35** | ns<br>ns |
| $t_{D1}$ | Delay Time | Test Figure 1 | | 45 | 75<br>**100** | ns<br>ns |
| $t_{D2}$ | Delay Time | Test Figure 1 | | 50 | 75<br>**100** | ns<br>ns |
| **POWER SUPPLY** | | | | | | |
| $I_S$ | Power Supply Current | $V_{IN}$ = 3 V<br>$V_{IN}$ = 0 V | | 0.45<br>60 | **3**<br>**400** | mA<br>µA |
| $V_S$ | Operating Input Voltage | | 4.5 | | 20 | V |

**Notes:**
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
3. Specification for packaged product only.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF.

## Test Circuits

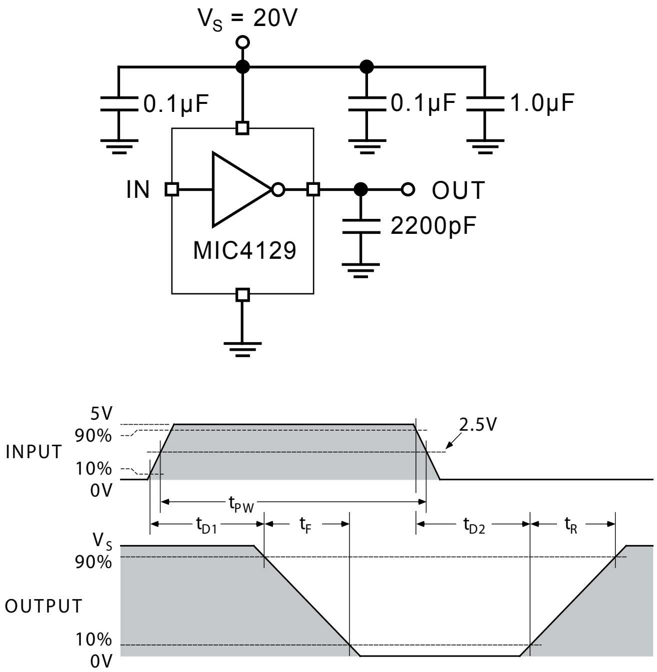



**Figure 1. Inverting Driver Switching Time**

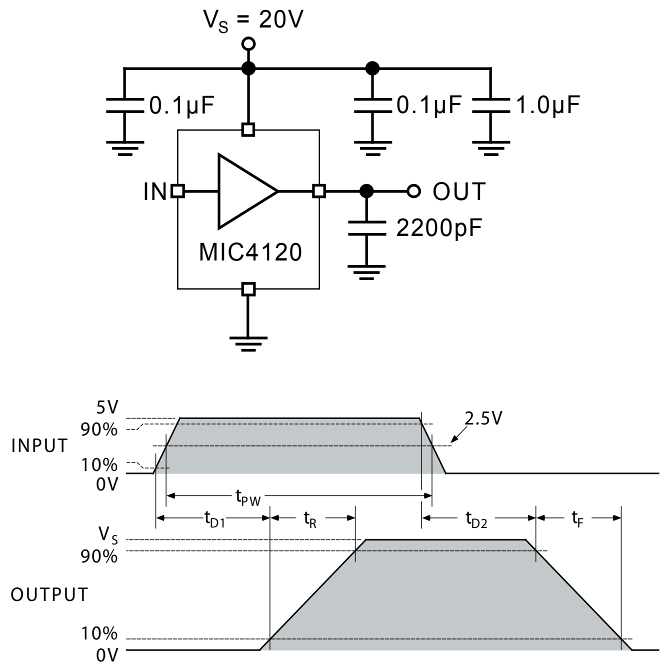
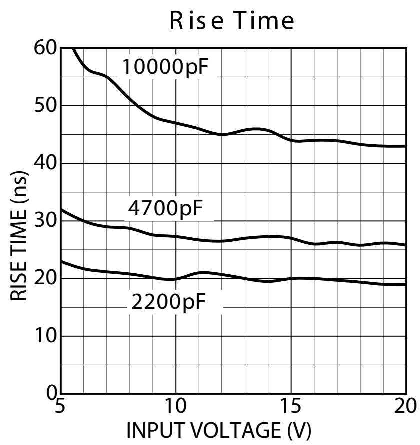
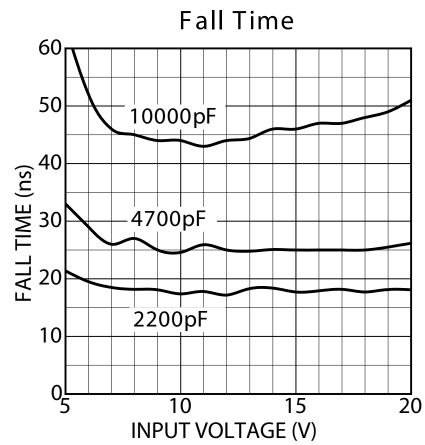
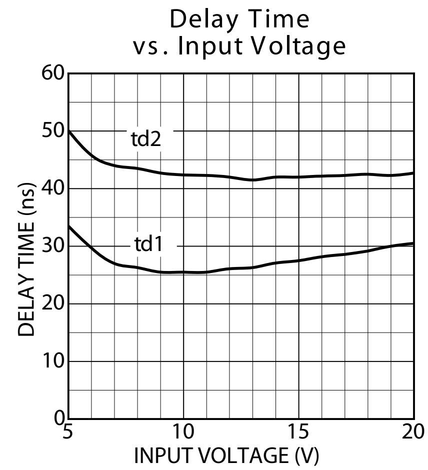


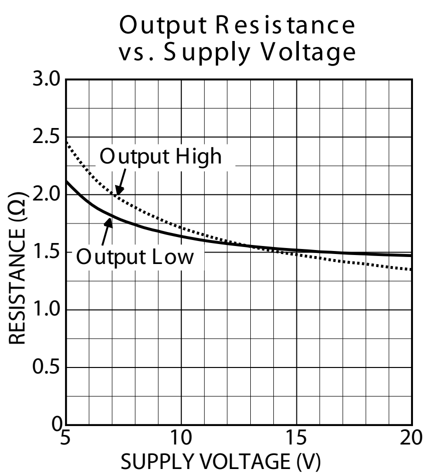

**Figure 2. Non-inverting Driver Switching Time**

## Typical Characteristics



## Applications Information

### Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500pF load to 18V in 25ns requires a 1.8 A current from the device power supply.

The MIC4120/4129 has double bonding on the supply pins, the ground pins and output pins This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic capacitors should be used. A 1µF low ESR film capacitor in parallel with two 0.1 µF low ESR ceramic capacitors provide adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

### Grounding

The high current capability of the MIC4120/4129 demands careful PC board layout for best performance. Since the MIC4129 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs.

Figure 3 shows the feedback effect in detail. As the MIC4129 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4129 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4129 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4129 GND pins should, however, still be connected to power ground.

The E-Pad and MLF packages have an exposed pad under the package. It's important for good thermal performance that this pad is connected to a ground plane.

## Input Stage

The input voltage level of the 4129 changes the quiescent supply current. The N channel MOSFET input stage transistor drives a 450µA current source load. With a logic “1” input, the maximum quiescent supply current is 450µA. Logic “0” input level signals reduce quiescent current to 55µA maximum.

The MIC4120/4129 input is designed to provide hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the 4.5V to 20V operating supply voltage range. Input current is less than 10µA over this range.

The MIC4129 can be directly driven by the MIC9130, MIC3808, MIC38HC42 and similar switch mode power supply. By offloading the power-driving duties to the MIC4120/4129, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the $^{+}V_S$ supply, however, current will flow into the input lead. The propagation delay for $T_{D2}$ will increase to as much as 400ns at room temperature. The input currents can be as high as 30mA p-p (6.4$mA_{RMS}$) with the input, 6 V greater than the supply voltage. No damage will occur to MIC4120/4129 however, and it will not latch.

The input appears as a 7pF capacitance, and does not change even if the input is driven from an AC source. Care should be taken so that the input does not go more than 5 volts below the negative rail.

## Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs-to-ground will not force enough current to destroy the device. The MIC4120/4129, on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current vs frequency and supply current vs capacitive load characteristic curves aid in determining power dissipation calculations. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 2500pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin EPAD MSOP package, from the data sheet, is 60°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 2W.

Accurate power dissipation numbers can be obtained by totaling the three sources of power dissipation in the device:

- Load Power Dissipation ($P_L$)
- Quiescent power dissipation ($P_Q$)
- Transition power dissipation ($P_T$)

Calculation of load power dissipation differs depending upon whether the load is capacitive, resistive or inductive.

### Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load

$R_O$ = the output resistance of the driver when the output is high, at the power supply voltage used. (See data sheet)

D = fraction of time the load is conducting (duty cycle)

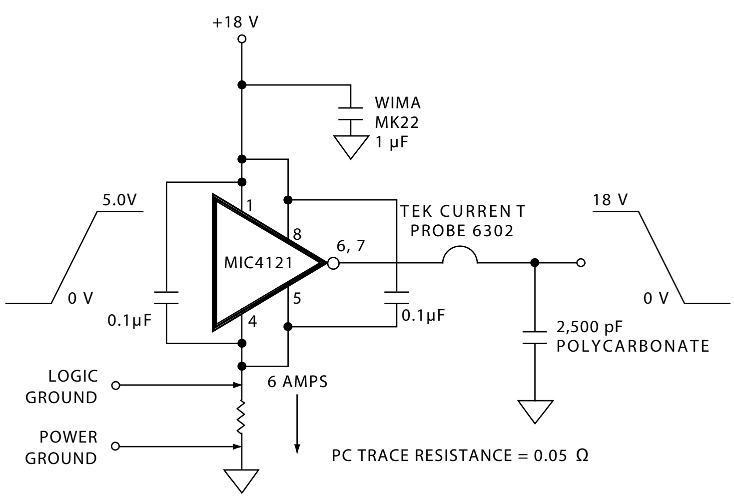



**Figure 3. Switching Time Degradation Due to Negative Feedback**

**Table 1: MIC4129 Maximum Operating Frequency**

| $V_S$ | Max Frequency |
|---|---|
| 20V | 1MHz |
| 15V | 1.5MHz |
| 10V | 3.5MHz |

**Conditions:** $T_A$ **= 25°C, 3.** $C_L$ **= 2500pF**

### Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = f\ C\ (V_S)^2$$

where:

f = Operating Frequency
C = Load Capacitance
$V_S$ =Driver Supply Voltage

### Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2\ R_O\ D$$

However, in this instance the $R_O$ required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1\text{-}D)$$

where $V_D$ is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce $P_L$

$$P_L = P_{L1} + P_{L2}$$

### Quiescent Power Dissipation

Quiescent power dissipation ($P_Q$, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2mA; a logic high will result in a current drain of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1\text{-}D)\ I_L]$$

where:

$I_H$ = quiescent current with input high
$I_L$ = quiescent current with input low
D = fraction of time input is high (duty cycle)
$V_S$ = power supply voltage

### Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from $V^+{}_S$ to ground. The transition power dissipation is approximately:

$$P_T = 2\ f\ V_S\ (A\bullet s)$$

where (A•s) is a time-current factor derived from the typical characteristic curves.

Total power ($P_D$) then, as previously described is:

$$P_D = P_L + P_Q + P_T$$

### Definitions

$C_L$ = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

$I_H$ = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

$I_L$ = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

$I_D$ = Output current from a driver in Amps.

$P_D$ = Total power dissipated in a driver in Watts.

$P_L$ = Power dissipated in the driver due to the driver's load in Watts.

$P_Q$ = Power dissipated in a quiescent driver in Watts.

$P_T$ = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is shown by the "Typical Characteristic Curve": Crossover Area vs. Supply Voltage and is in ampere-seconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.

$R_O$ = Output resistance of a driver in Ohms.

$V_S$ = Power supply voltage to the IC in Volts.

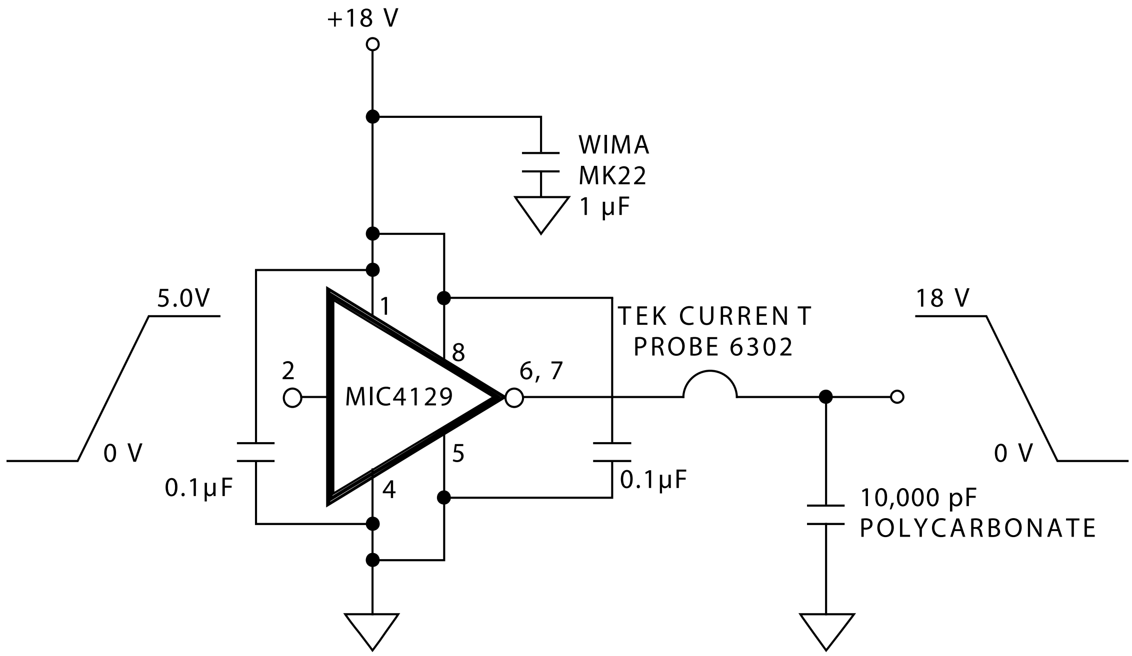
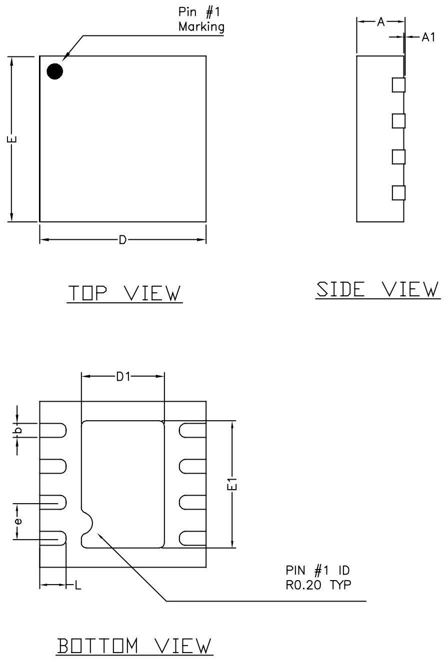


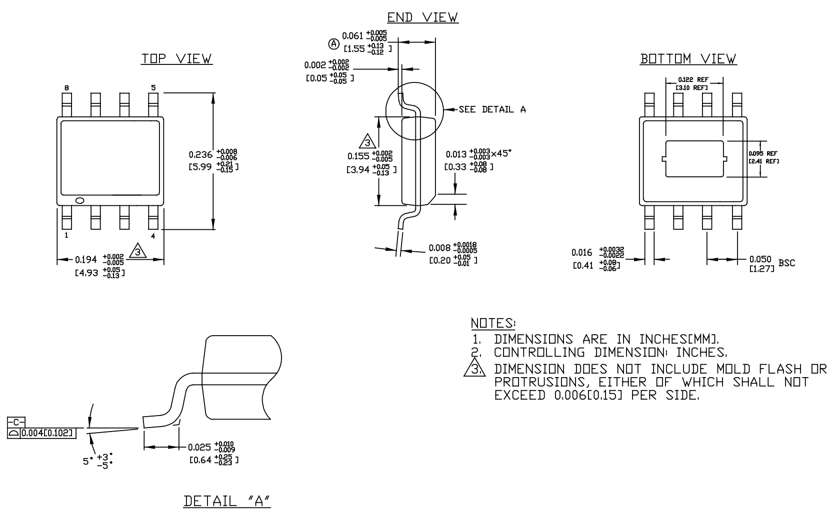

**Figure 4. Peak Output Current Test Circuit**

## Package Information




| | MILIMETERS | | |
|---|---|---|---|
| POS | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| D | 3.00 BSC | | |
| D1 | 2.20 | 2.30 | 2.40 |
| E | 3.00 BSC | | |
| E1 | 1.45 | 1.55 | 1.70 |
| b | 0.20 | 0.275 | 0.35 |
| e | 0.65 BSC | | |
| L | 0.35 | 0.45 | 0.52 |

**8-Pin 3x3 MLF (ML)**




**8-Pin Exposed Pad SOIC (ME)**

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