

RD30LDT3595

24-bit Serial-in Parallel-out LED Driver IC

REJ03D0896-0300

Rev.3.00

Jun 16, 2008

Description

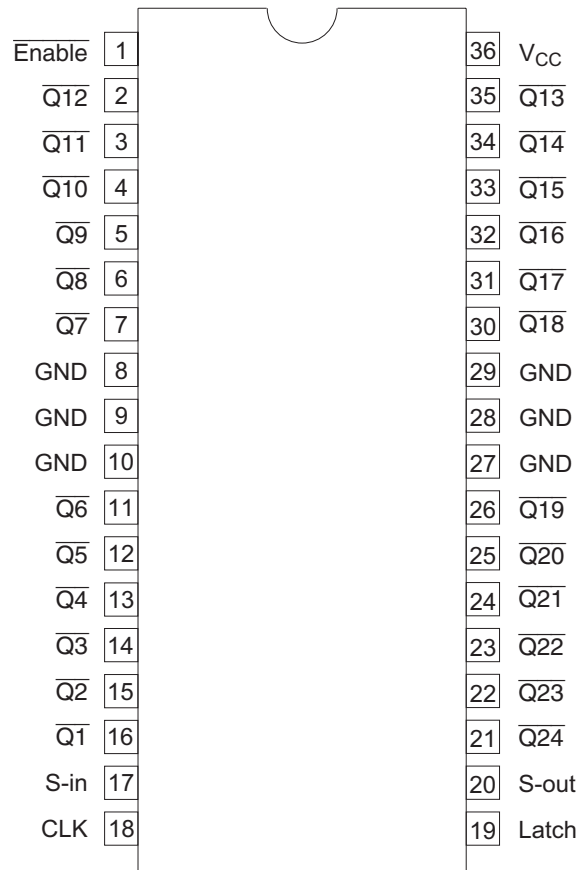
The RD30LDT3595 has twenty-four edge trigger D-type Flip-Flops with twenty-four latches in 36-pin package. Data is input to the serial data input and the clock pulse is input to the clock input. When the clock is changed from "L" to "H", the signal of the data input enters an internal shift register. The data of the shift register is shifted one by one. In addition, output load circuit is added so that power supply prevents a wrong action in on/off. When V_{CC} is less than a fixed level, the output ($\overline{Q1}$ to $\overline{Q24}$) compulsorily is off state. Low-voltage and high-speed operation is suitable for battery-powered product (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- Supply voltage range : 4.5 to 5.5 V, $V_O = 30$ V
- Output current : $I_O = 100$ mA (@ $V_{CC} = 5$ V)
- All the logical input has hysteresis voltage for the slow transition.
- Input with pull-up resistance. (Enable, Latch terminal)
- Input with pull-down resistance. (CLK, S-in terminal)
- Ordering Information

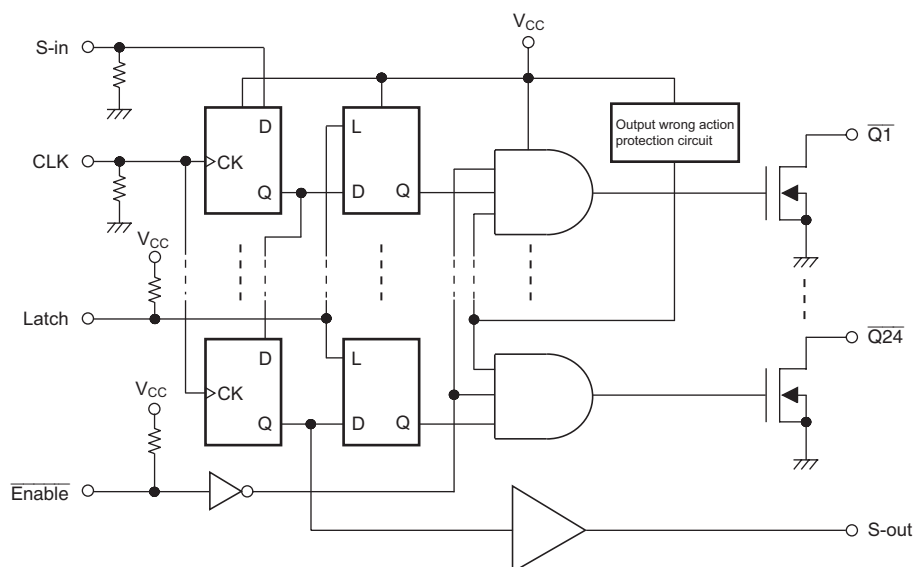
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RD30LDT3595FPH0	SSOP-36 pin	PRSP0036GA-A (36P2R-A)	FP	H (1,000 pcs/reel)	0 (Sn-Cu)

Pin Arrangement



(Top view)

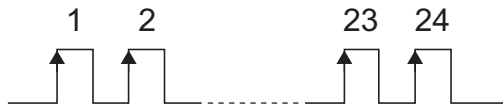
Logic Diagram



Function Table

Inputs				Outputs	
S-in	CLK ^{*1}	Latch	Enable	$\overline{Q1}$ to $\overline{Q24}$	S-out
L	IN	L	L	t - 1	L
L	IN	H	L	Z	L
H	IN	L	L	t - 1	H
H	IN	H	L	L	H
H	IN	H	H	Z	H

^{*1} IN : Input the following signal in CLK



H : High level

L : Low level

Z : High impedance

t - 1 : Output level before the indicated steady state input conditions were established.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	-0.5 to 7	V	
Input voltage range	V_I	-0.5 to $V_{CC} + 0.5$	V	
Output voltage range ^{*1} ,	V_O	-0.5 to 30	V	Output : Z (OFF)
		-0.5 to $V_{CC} + 0.5$	V	S-out
Continuous output current	I_O	100	mA	$V_O = 0$ to V_{CC}
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*2}	P_d	1.9	W	
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. This value is limited to 30 V maximum.

2. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	4.5	5.5	V	
Output voltage range	V_O	—	30	V	$\overline{Q1}$ to $\overline{Q24}$: Z (OFF)
Output current (per pin)	I_O	—	100	mA	$\overline{Q1}$ to $\overline{Q24}$: ON (duty cycle $\leq 50\%$)
Operating free-air temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristic

Item	Symbol	V _{CC} (V) *	Ta = 25°C			Ta = -40 to 85°C			Unit	Test condition
			Min	Typ	Max	Min	Typ	Max		
Input voltage	V _{IH}	4.5 to 5.5	2.0	—	V _{CC}	2.0	—	V _{CC}	V	
	V _{IL}	4.5 to 5.5	0	—	0.8	0	—	0.8	V	
Input current	I _{IH}	5.5	—	—	25	—	—	30	μA	V _{IH} = 5.5 V
	I _{IL}	5.5	—	—	-25	—	—	-30	μA	V _{IL} = 0 V
Output voltage (S-out)	V _{OH}	5.0	4.9	—	—	4.9	—	—	V	I _{OH} = -1 μA
	V _{OL}	5.0	—	—	0.1	—	—	0.1	V	I _{OL} = 1 μA
Output voltage (Q1 to Q24)	V _{OL}	5.0	—	—	0.55	—	—	0.77	V	I _{OL} = 100 mA
Output leakage current	I _{OLK}	5.5	—	—	50	—	—	100	μA	V _O = 30 V (Output : Z (OFF))
Quiescent supply current	I _{CC1}	5.5	—	—	300	—	—	500	μA	Input : Open All driver output : OFF
	I _{CC2}	5.5	—	—	300	—	—	500	μA	Driver output one circuit : ON
Driver output wrong action protection voltage	V _{T+}	—	2.9	3.4	3.9	2.9	3.4	3.9	V	
	V _{T-}	—	2.6	3.1	3.6	2.6	3.1	3.6	V	

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Timing Characteristics

(V_{CC} = 5 V, C_L = 15 pF, R_L (S-out) = ∞, R_L ($\overline{Qn}$) = 100 Ω, t_r = t_f = 20 ns)

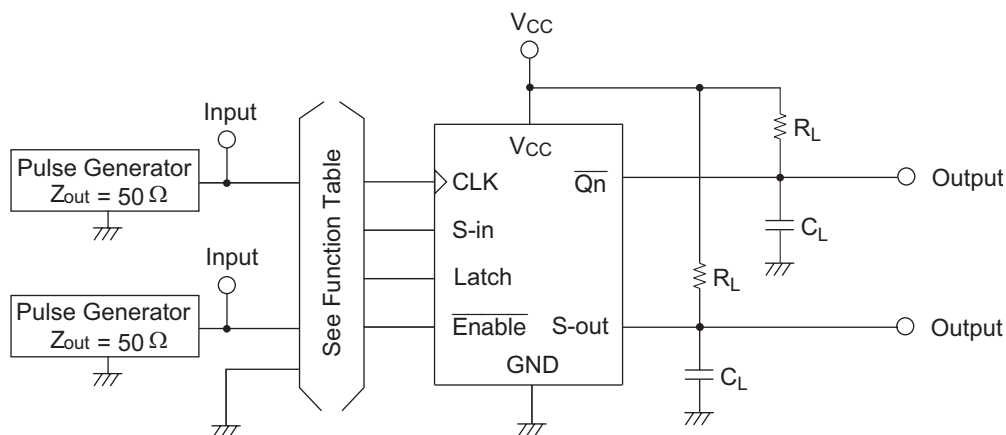
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C			Unit	Test condition
		Min	Typ	Max	Min	Typ	Max		
Maximum clock frequency	f _{max}	—	—	12.5	—	—	12.5	MHz	Duty cycle = 45 % to 55 %
Pulse width	t _W	30	—	—	30	—	—	ns	CLK
Pulse width	t _W	30	—	—	30	—	—	ns	Latch
Setup time	t _{su}	30	—	—	30	—	—	ns	S-in to CLK
Hold time	t _h	20	—	—	20	—	—	ns	S-in to CLK
Setup time	t _{su}	60	—	—	60	—	—	ns	Latch to CLK
Clock pulse rise time	t _r	—	—	500	—	—	500	ns	
Clock pulse fall time	t _f	—	—	500	—	—	500	ns	

Switching Characteristics

(V_{CC} = 5 V, C_L = 15 pF, R_L (S-out) = ∞, R_L ($\overline{Qn}$) = 100 Ω, t_r = t_f = 20 ns)

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Typ	Max			
Propagation delay time	t _{PLH}	—	—	60	—	—	60	ns	CLK	S-out
	t _{PHL}	—	—	60	—	—	60			
	t _{PLH}	—	—	70	—	—	70	ns	CLK	$\overline{Qn}$
	t _{PHL}	—	—	70	—	—	70			
	t _{PLH}	—	—	70	—	—	70	ns	Enable	$\overline{Qn}$
	t _{PHL}	—	—	70	—	—	70			

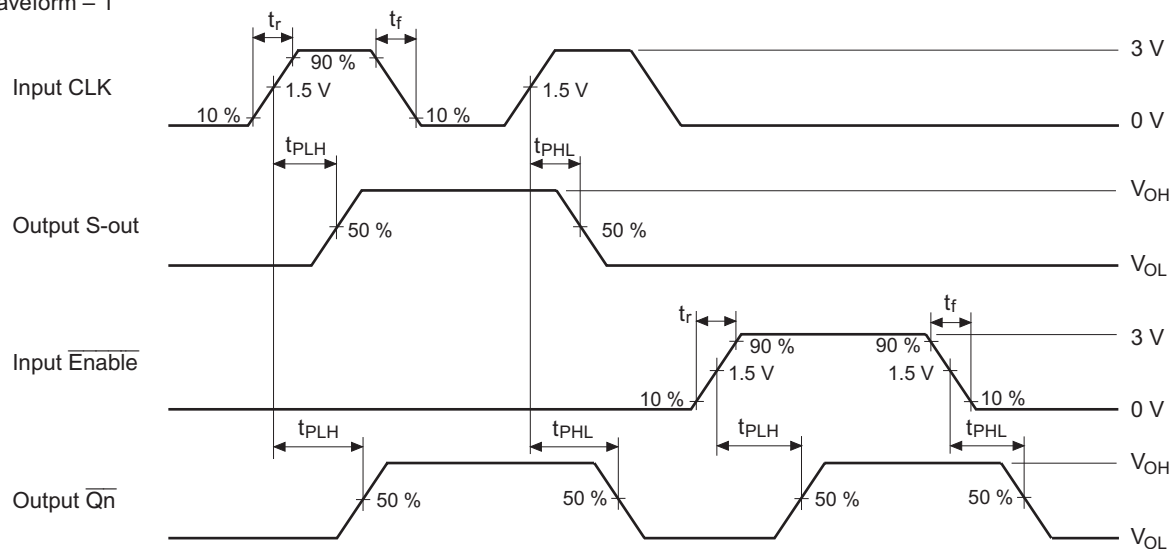
Test Circuit



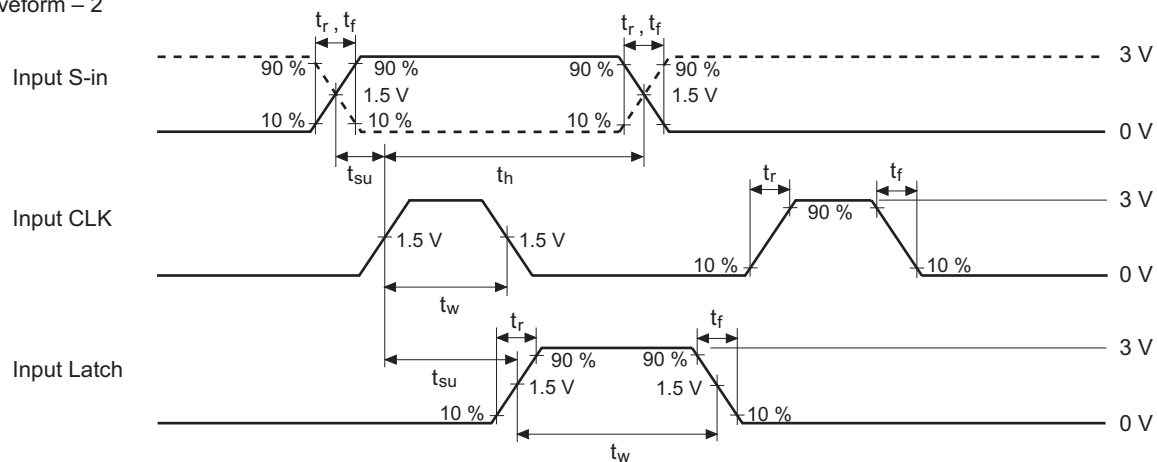
Notes: 1. Input waveform : $PRR \leq 1\text{MHz}$, Duty Cycle = 50%, $t_r \leq 20\text{ns}$, $t_f \leq 20\text{ns}$
 2. C_L includes probe and jig capacitance.

Waveforms

• Waveform – 1

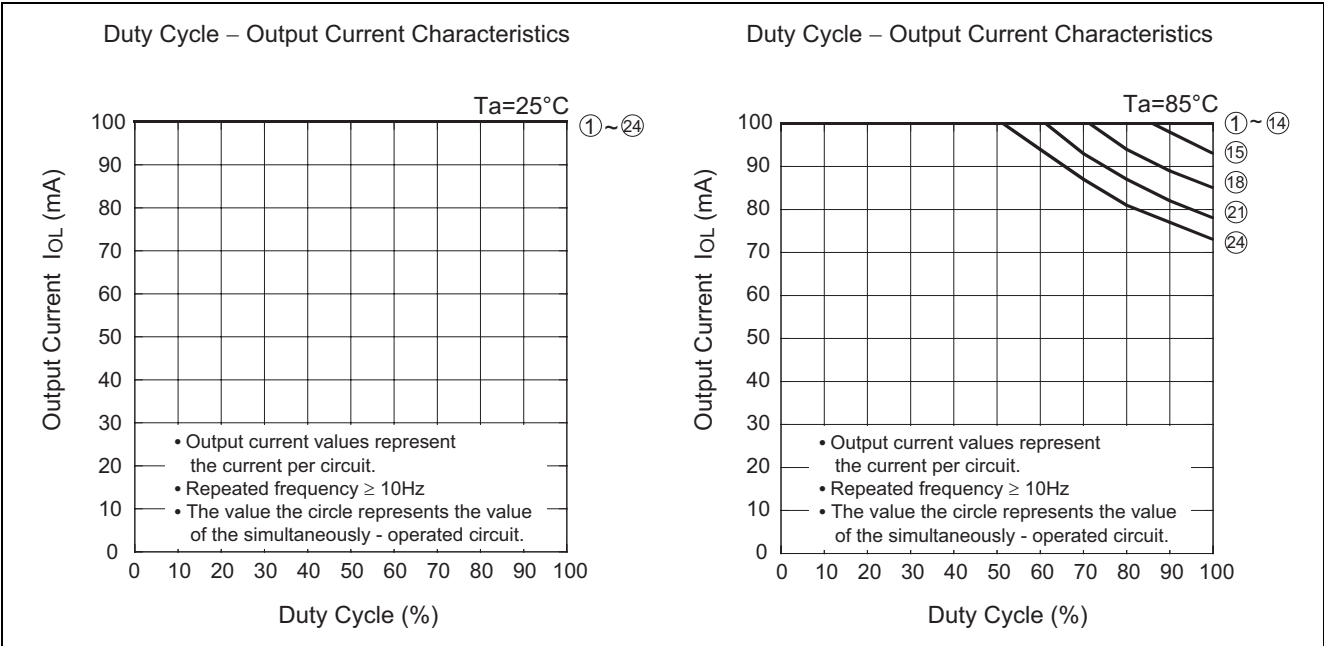


• Waveform – 2



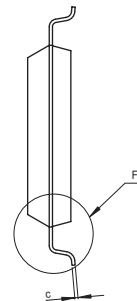
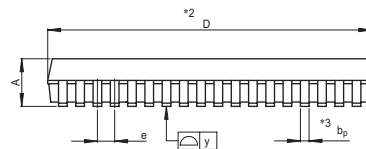
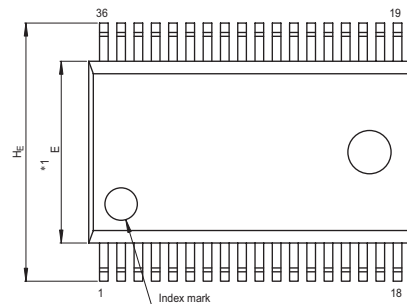
Notes: 1. Input waveform : $PRR \leq 1\text{MHz}$, $Z_o = 50\ \Omega$, $t_r \leq 20\text{ns}$, $t_f \leq 20\text{ns}$
 2. The output are measured one at a time with one transition per measurement.

Application Data

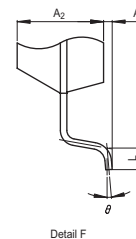


Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-A	36P2R-A	0.5g



NOTE)
1. DIMENSIONS "**1" AND "**2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "**3" DOES NOT
INCLUDE TRIM OFFSET.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A ₂	—	2.0	—
A	—	—	2.4
A ₁	0.05	—	—
b _p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H _E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

Notes:

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450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510