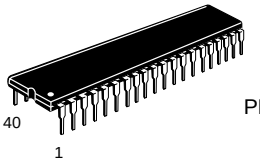
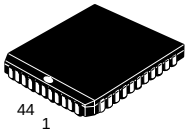
MC14469

Addressable Asynchronous Receiver/Transmitter

CMOS



P SUFFIX
PLASTIC DIP
CASE 711



FN SUFFIX
PLCC PACKAGE
CASE 777

ORDERING INFORMATION

MC14469P	Plastic DIP
MC14469FN	PLCC Package

The MC14469 receives one or two 11–bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 then transmits information in two 11–bit word data streams. Each of the transmitted words contains eight data bits, an even parity bit, and start and stop bits.

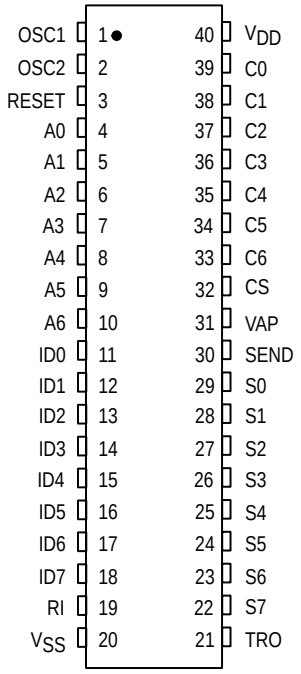
The received word contains seven address bits with the address of the MC14469 set on seven pins. Therefore, 2^7 or 128 units can be interconnected in simplex or full–duplex data transmission. In addition to the address received, seven command bits may be received for general–purpose data or control use.

The MC14469 finds application in transmitting data from remote analog–to–digital converters, remote MPUs, or remote digital transducers to the master computer or MPU.

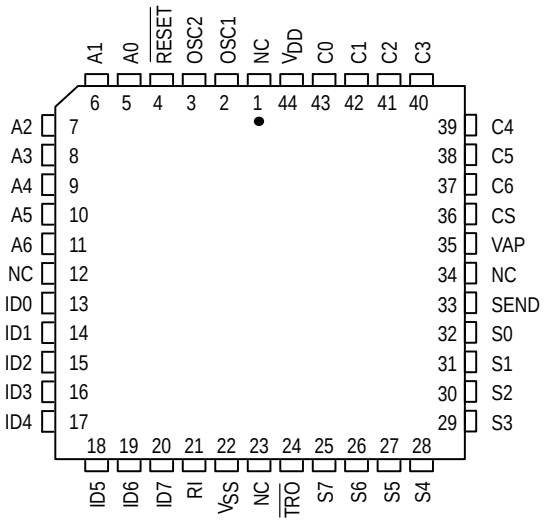
- Supply Voltage Range: 4.5 V to 18 V
- Low Quiescent Current: 75 μA Maximum @ 5 V, 25°C
- Guaranteed Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
- Receive — Serial to Parallel
  Transmit — Parallel to Parallel
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On–Chip Oscillator
- See Application Note AN806A
- Chip Complexity: 1200 FETs or 300 Equivalent Gates

PIN ASSIGNMENTS

P SUFFIX



FN SUFFIX



NC = NO CONNECTION

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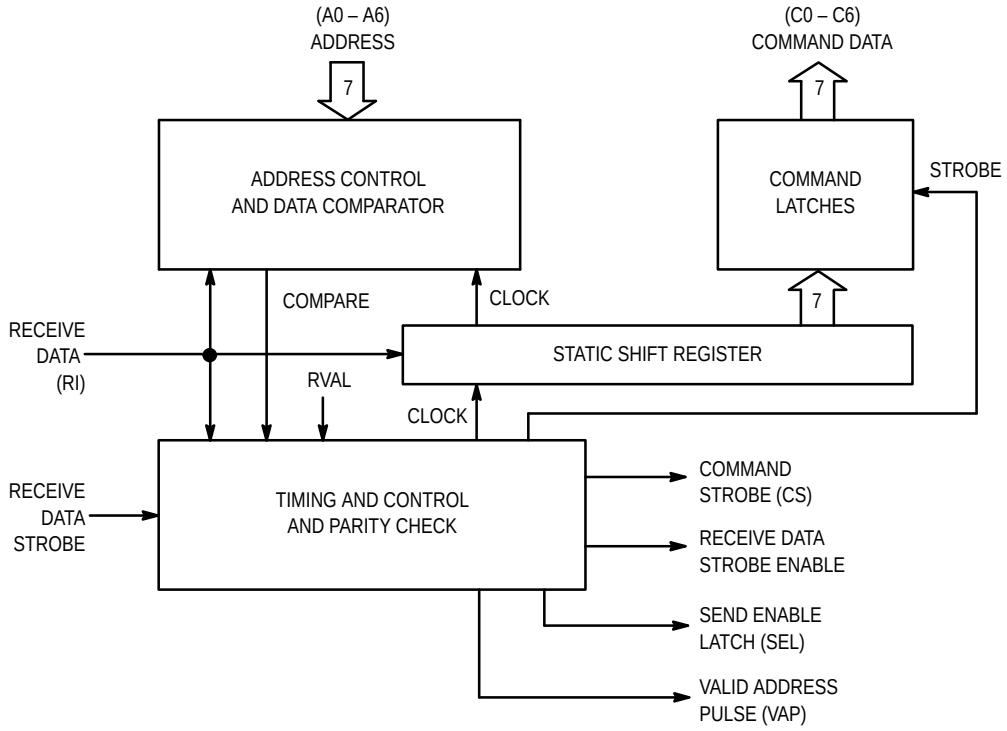
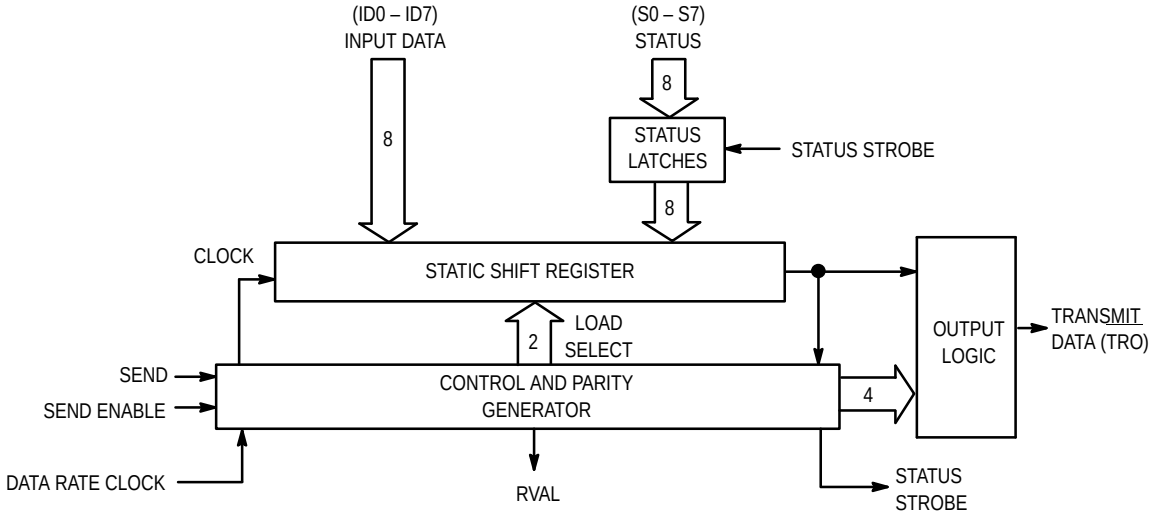
BLOCK DIAGRAM

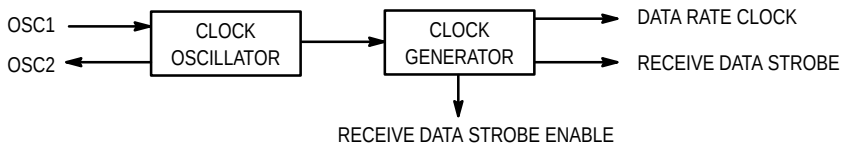
RECEIVE



TRANSMIT



CLOCKS



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD}	– 40°C Min	– 40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Output Voltage	V_{OL}								V
V_{in} = V_{DD} or 0 “0” Level		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{in} = 0 or V_{DD} “1” Level	V_{OH}	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
Input Voltage (Except OSC1)	V_{IL}								V
V_O = 4.5 or 0.5 V “0” Level		5.0	—	1.5	—	1.5	—	1.5	
V_O = 9.0 or 1.0 V		10	—	3.0	—	3.0	—	3.0	
V_O = 13.5 or 1.5 V		15	—	4.0	—	4.0	—	4.0	
V_O = 0.5 or 4.5 V “1” Level	V_{IH}	5.0	3.5	—	3.5	—	3.5	—	V
V_O = 1.0 or 9.0 V		10	7.0	—	7.0	—	7.0	—	
V_O = 1.5 or 13.5 V		15	11	—	11	—	11	—	
Output Drive Current (Except OSC2)	I_{OH}								mA
V_{OH} = 2.5 V Source		5.0	– 1.0	—	– 0.8	—	– 0.6	—	
V_{OH} = 4.6 V		5.0	– 0.2	—	– 0.16	—	– 0.12	—	
V_{OH} = 9.5 V		10	– 0.5	—	– 0.4	—	– 0.3	—	
V_{OH} = 13.5 V		15	– 1.4	—	– 1.2	—	– 1.0	—	
V_{OL} = 0.4 V Sink	I_{OL}	5.0	0.52	—	0.44	—	0.36	—	mA
V_{OL} = 0.5 V		10	1.3	—	1.1	—	0.9	—	
V_{OL} = 1.5 V		15	3.6	—	3.0	—	2.4	—	
Output Drive Current (OSC2 Only)	I_{OH}								mA
V_{OH} = 2.5 V Source		5.0	– 0.19	—	– 0.16	—	– 0.13	—	
V_{OH} = 4.6 V		5.0	– 0.04	—	– 0.035	—	– 0.03	—	
V_{OH} = 9.5 V		10	– 0.09	—	– 0.08	—	– 0.06	—	
V_{OH} = 13.5 V		15	– 0.29	—	– 0.27	—	– 0.2	—	
V_{OL} = 0.4 V Sink	I_{OL}	5.0	0.1	—	0.085	—	0.07	—	mA
V_{OL} = 0.5 V		10	0.17	—	0.14	—	0.1	—	
V_{OL} = 1.5 V		15	0.5	—	0.42	—	0.3	—	
OSC Frequency*	f_{OSC}	4.5	0	400	0	365	0	310	kHz
		12	0	800	0	730	0	620	
Input Current	I_{in}	15	—	± 0.3	—	± 0.3	—	± 1.0	µA
Pull–Up Current (A0 – A6, ID0 – ID7)	I_{UP}	15	12	120	10	100	8.0	85	µA
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	75	—	75	—	565	µA
		10	—	150	—	150	—	1125	
		15	—	300	—	300	—	2250	
Supply Voltage	V_{DD}	—	+ 4.5	+ 18	+ 4.5	+ 18	+ 4.5	+ 18	V

* 310 kHz at 85°C guarantees 4800 baud; 620 kHz at 85°C guarantees 9600 baud.

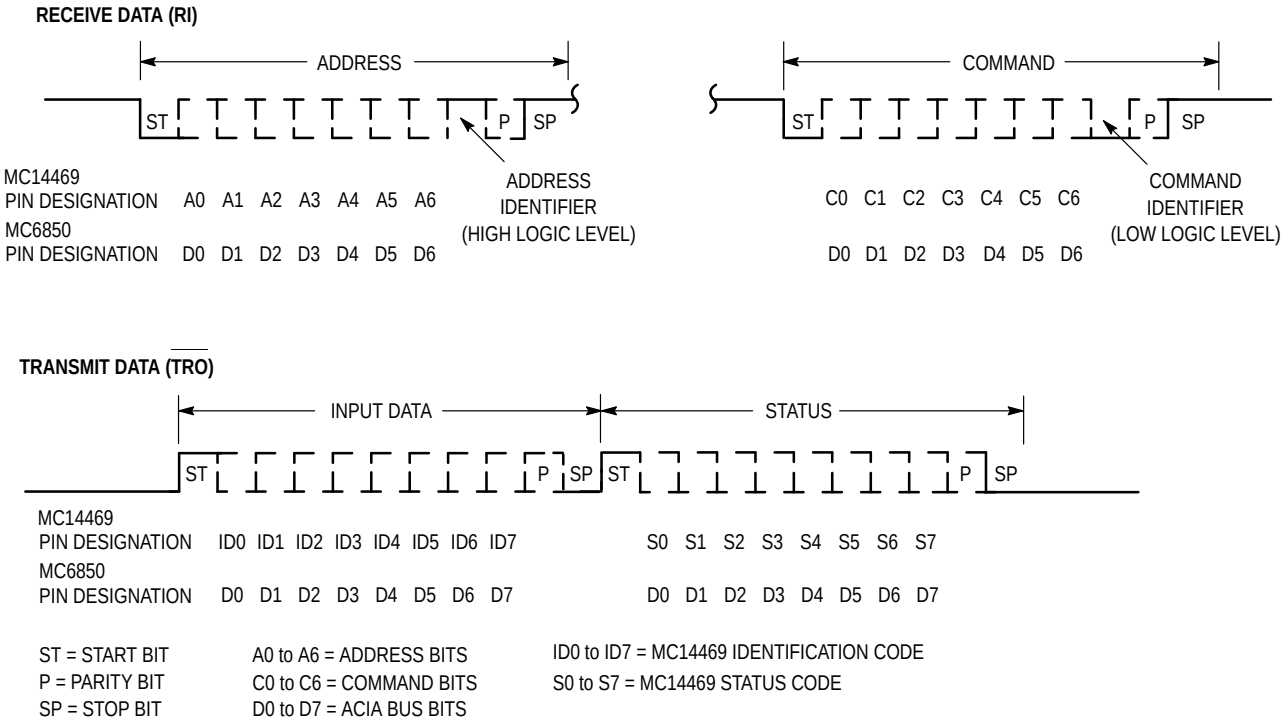


Figure 1. Data Format and Corresponding Data Position and Pins for MC14469 and MC6850

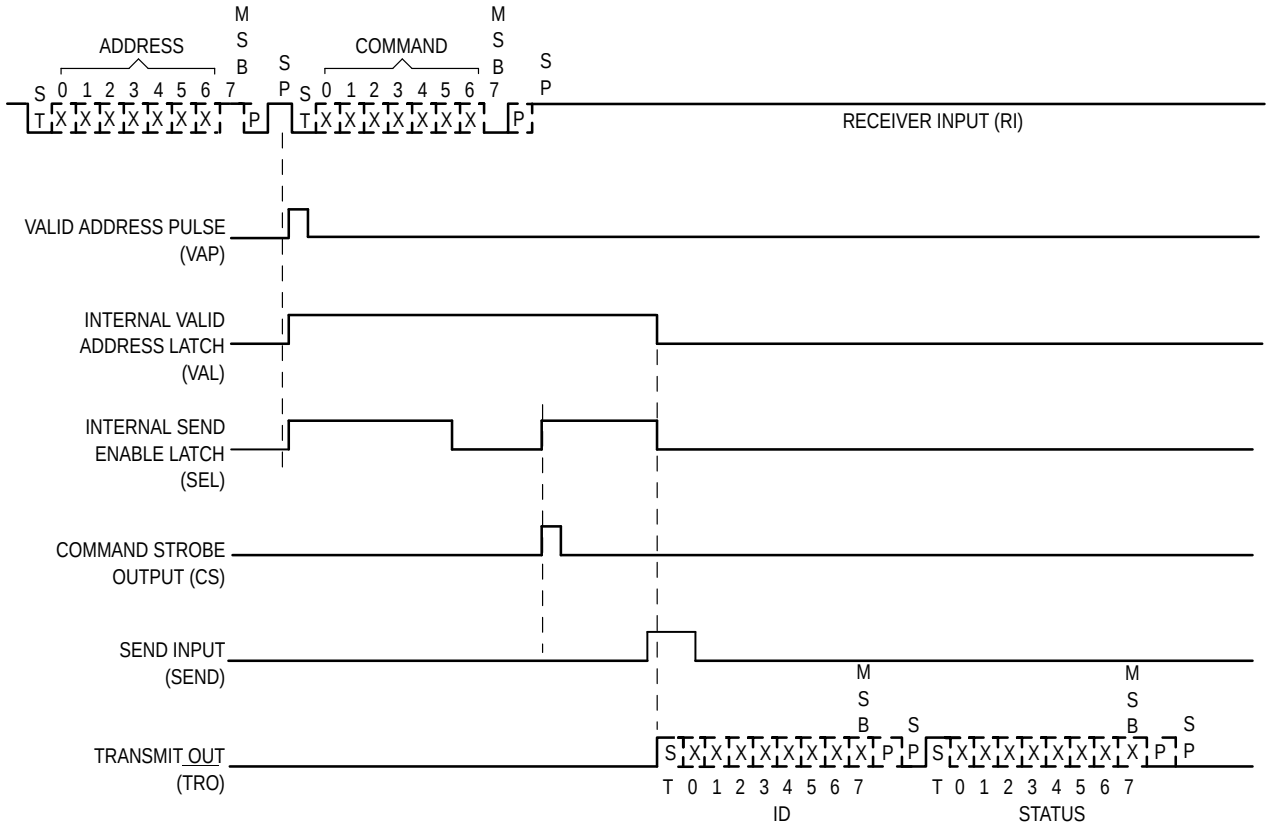


Figure 2. Typical Receive/Send Cycle

PIN DESCRIPTIONS

A0 – A6
Address Inputs

These inputs are the address setting pins which contain the address match for the received signal. Pins A0 – A6 have on–chip pull–up resistors.

C0 – C6
Command Word

These pins are the readout of the general–purpose command word which is the second word of the received signal.

CS
Command Strobe

This is the output for the command strobe signifying a valid set of command data (C0 – C6). The pulse width is one oscillator cycle. For example, when a 307.2 kHz ceramic resonator is used, the pulse width is approximately 3 μs.

ID0 – ID7
Input Data Pins

These pins contain the input data for the first eight bits of data to be transmitted. Pins ID0 – ID7 have on–chip pull–up resistors.

OSC1, OSC2
Oscillator Input and Oscillator Output

These pins are the oscillator input and output (see Figure 3).

$\overline{\text{RESET}}$
Reset

When this pin is pulled low for a minimum of 700 ns, the circuit is reset and ready for operation.

RI
Receive Input

This is the receive input pin.

S0 – S7
Second or Status Input Data

These pins contain the input data for the second eight bits of data to be transmitted.

SEND
Send

This pin accepts the send command after receipt of an address.

$\overline{\text{TRO}}$
Transmit Register Output Signal

This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

VAP
Valid Address Pulse

This is the output for the valid address pulse upon receipt of a matched incoming address.

V_{DD}
Positive Power Supply

This pin is the package positive power supply connection. This pin may range from + 4.5 V to + 18 V with respect to V_{SS}.

V_{SS}
Negative Power Supply

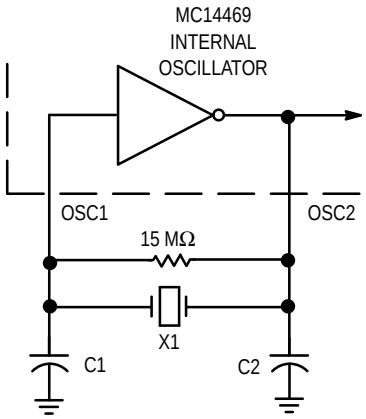
This pin is the negative power supply connection. Normally this pin is system ground.

OPERATING CHARACTERISTICS

The receipt of a start bit on the receive input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (A0 – A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word “1” or a command word “0”. Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address matches, a valid address pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit, and a stop bit. The eight data bits are composed of a seven–bit command, and a “0” which indicates a command word. At the end of the command word a command strobe pulse (CS) occurs.

A positive transition on the send input initiates the transmit sequence. Send must occur within seven bit times of CS. Again the transmitted data is made up of two eleven–bit words, i.e., address and command words. The data portion of the first word is made up from input data inputs (ID0 – ID7), and the data for the second word from second input data (S0 – S7) inputs. The data on inputs ID0 – ID7 is latched one clock before the falling edge of the start bit. The data on inputs S0 – S7 is latched on the rising edge of the start bit. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines. TRO begins either 1/2 or 1–1/2 bit times after send, depending where send occurs.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. OSC1 can be driven from an external oscillator (see Figure 3).



NOTE: For externally generated clock, drive OSC1, float OSC2.

X1 = Ceramic Resonator: 307.2 kHz ± 1 kHz for 4800 baud rate.
C1 and C2 are sized per the ceramic resonator supplier's recommendation.

Ceramic Resonator Suppliers:*
1. Morgan Matroc, Inc., Bedford, OH, 216/232–8600
2. Radio Materials Co., Attica, IN, 317/762–2491

* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 3. Oscillator Circuit

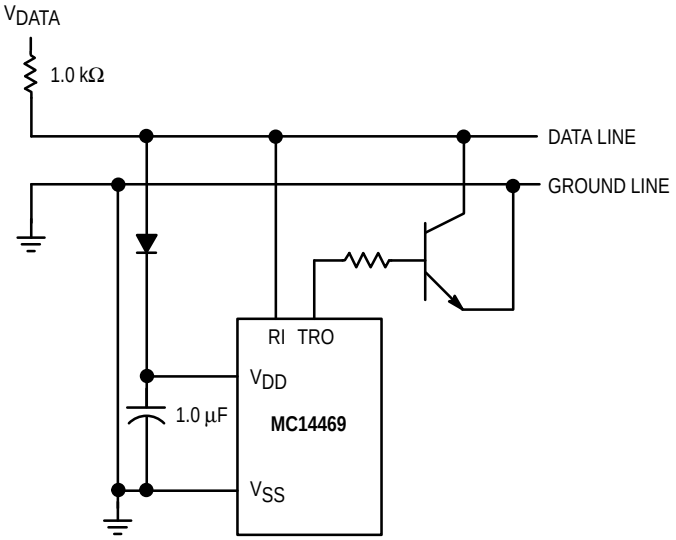


Figure 4. Rectified Power from Data Lines Circuit

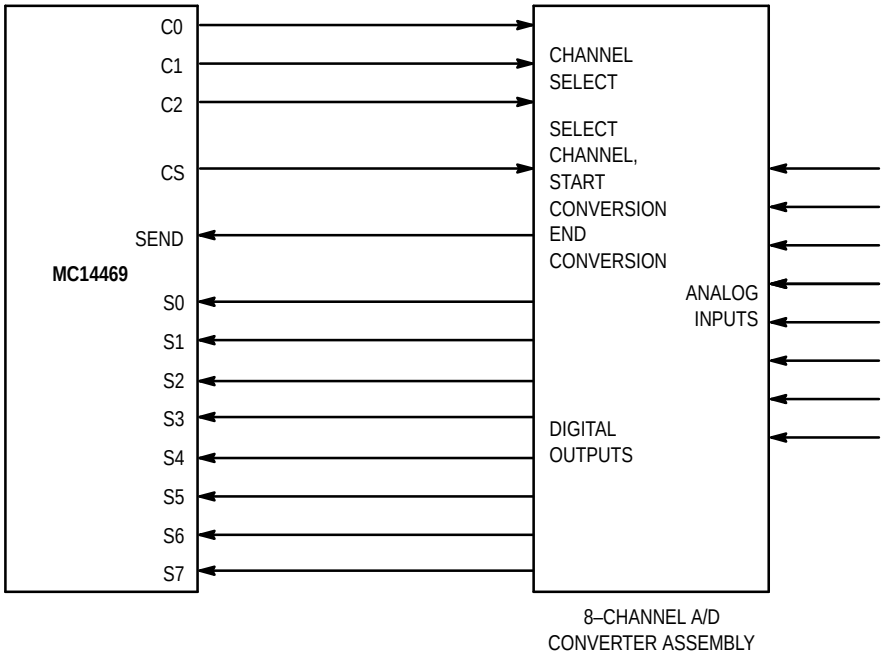
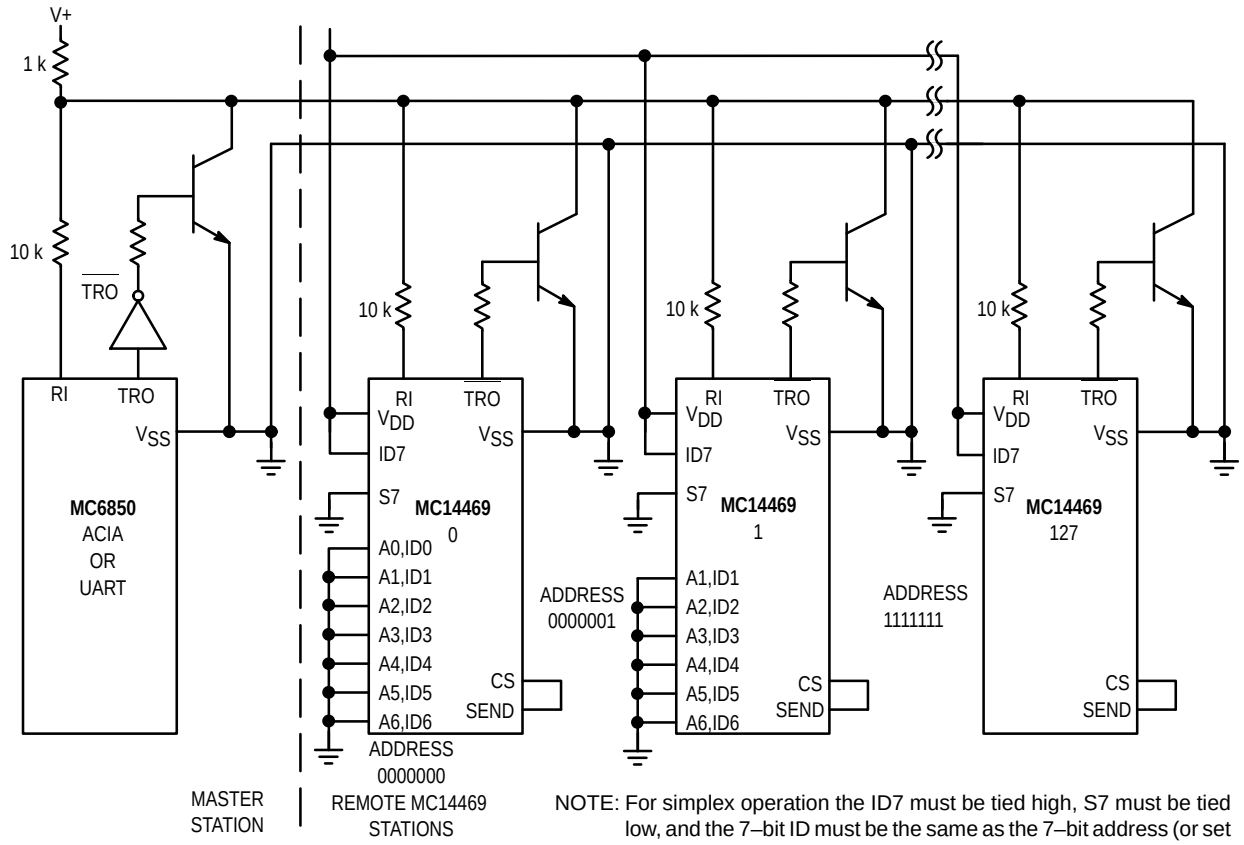


Figure 5. A–D Converter Interface



NOTE: For simplex operation the ID7 must be tied high, S7 must be tied low, and the 7–bit ID must be the same as the 7–bit address (or set to some unused address) to prevent erroneous responses.

Figure 6. Single Line, Simplex Data Transmission

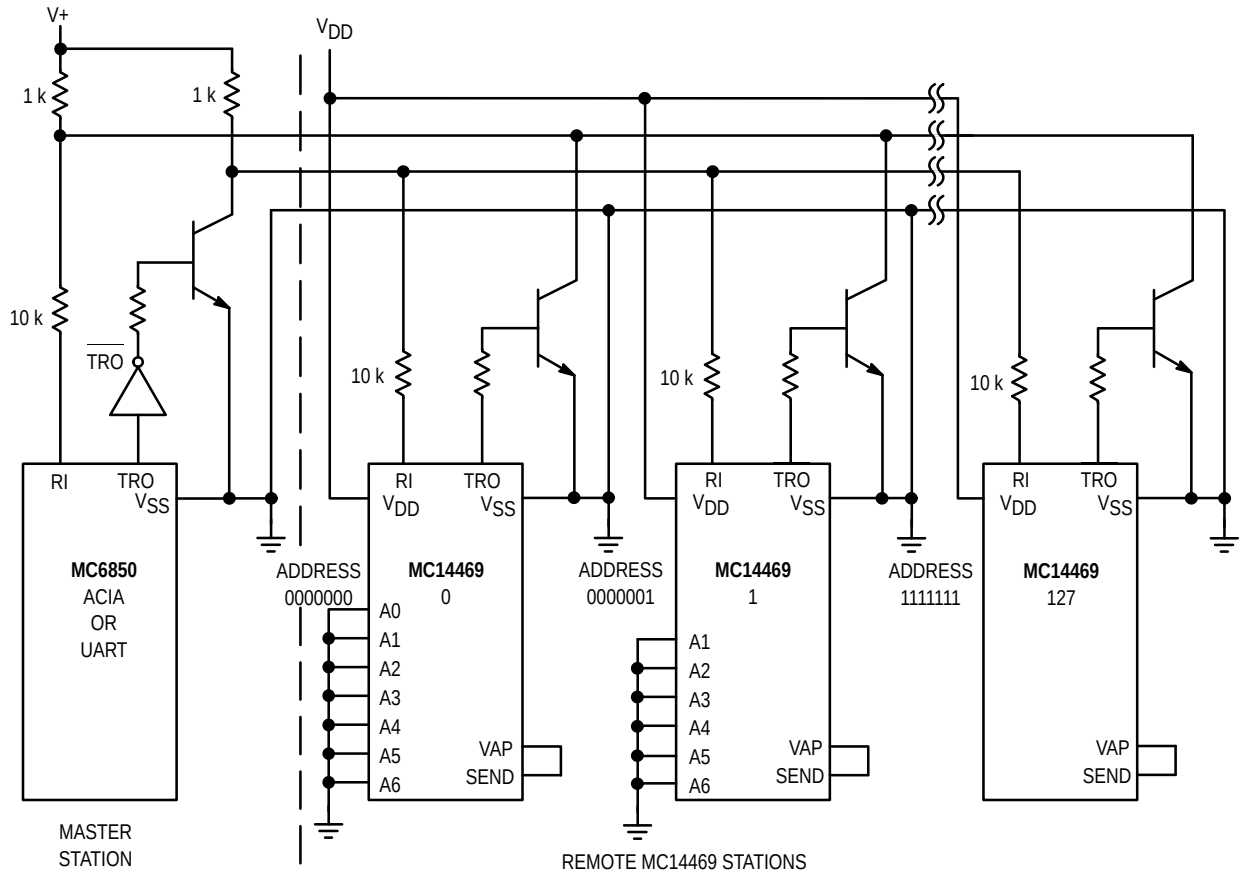


Figure 7. Double Line, Full Duplex Data Transmission

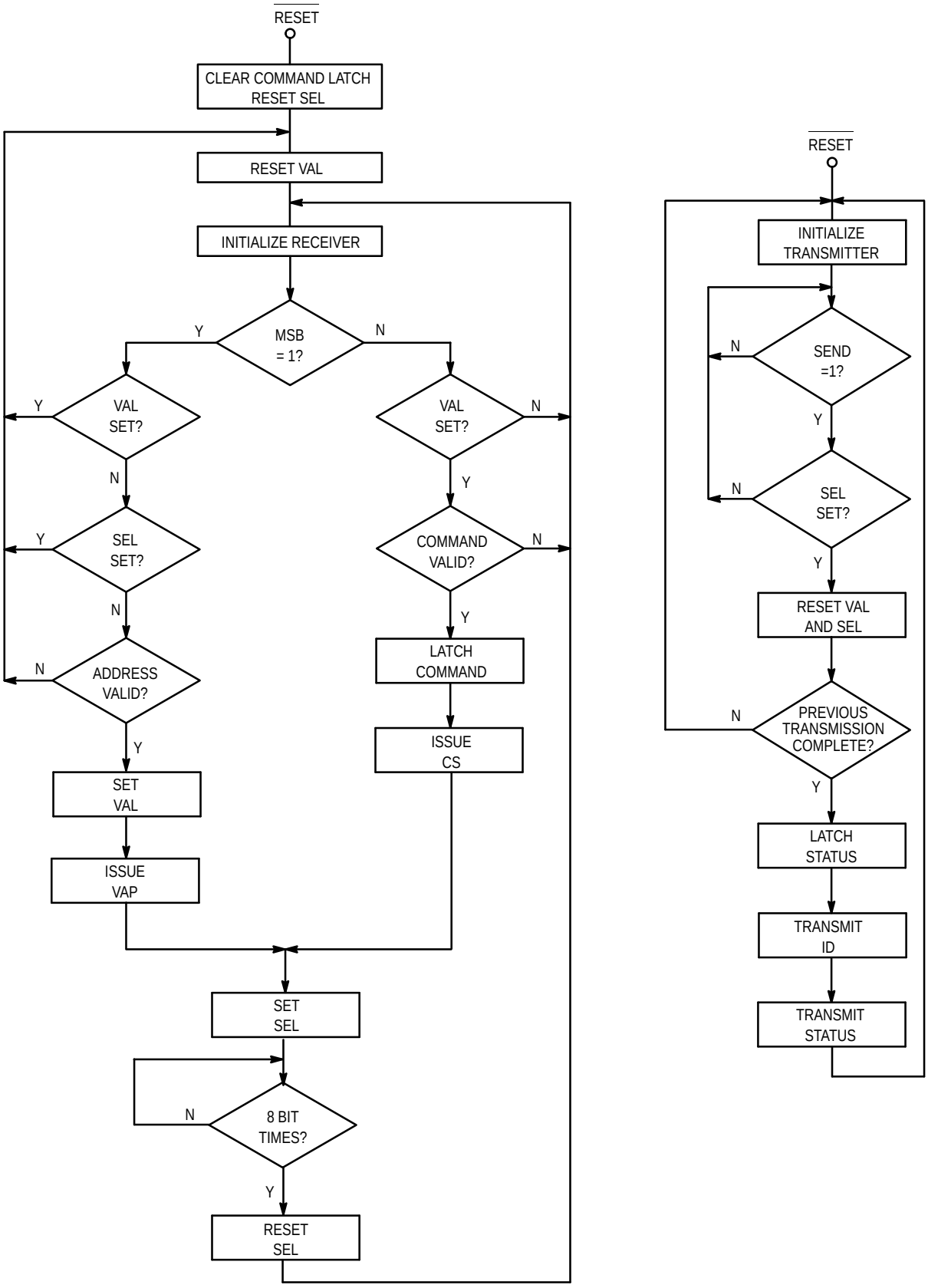
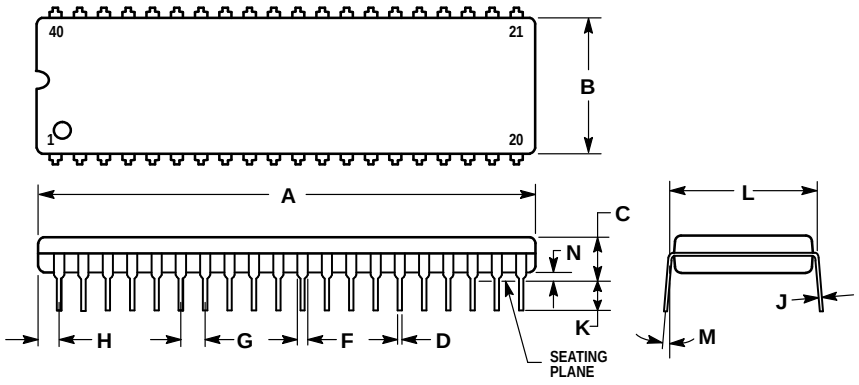


Figure 8. Flow Chart of MC14469 Operation

PACKAGE DIMENSIONS

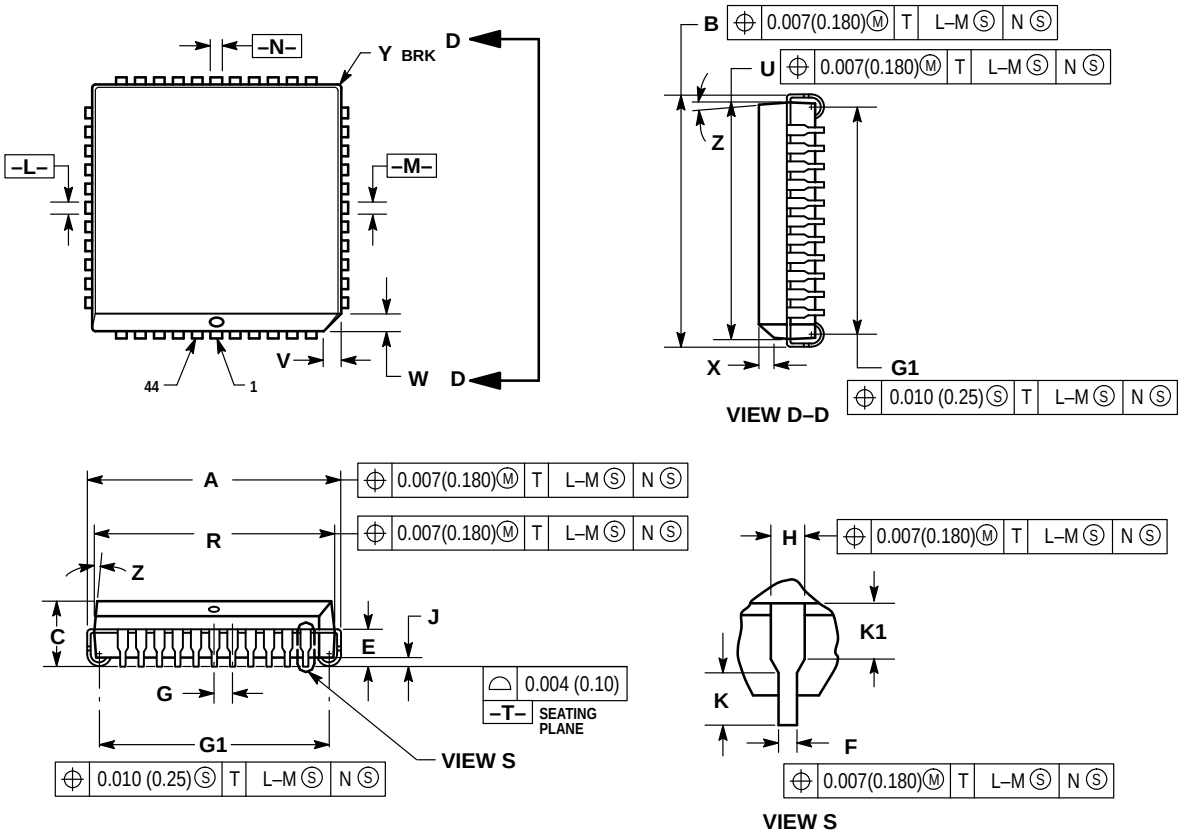
P SUFFIX
PLASTIC DIP
CASE 711–03



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

FN SUFFIX
PLCC PACKAGE
CASE 777–02



NOTES:
1. DATUMS –L–, –M–, AND –N– ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

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