

## TFT-LCD $I^2C$ Programmable VCOM Calibrator

The V<sub>COM</sub> voltage of an LCD panel needs to be adjusted to remove flicker. This part provides a digital interface to control the sink-current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external V<sub>COM</sub> buffer amplifier. The desired V<sub>COM</sub> setting is loaded from an external source via a standard 2-wire  $I^2C$  serial interface. At power up the part automatically comes up at the last programmed EEPROM setting.

An external resistor attaches to the SET pin, and sets the full-scale sink current that determines the lowest voltage of the external voltage divider.

The ISL45041 is available in an 8 Ld 3mmx3mm TDFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

An evaluation kit complete with software to control the DCP from a computer is available. Reference Application note AN1207 and Ordering Information.

## Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45041IRZ	041Z	0 to +85	8 Ld 3x3 TDFN	L8.3X3A
ISL45041IRZ-T*	041Z	0 to +85	8 Ld 3x3 TDFN Tape and Reel	L8.3X3A
ISL45041EVAL1Z	Evaluation Board			

\*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

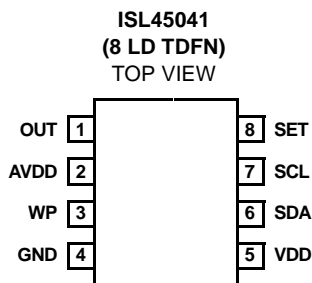
## Features

- 128-Step Adjustable Sink Current Output
- 2.25V to 3.3V Logic Supply Voltage Operating Range (2.25V Minimum Programming Voltage)
- Analog Supply Voltage Range 4.5V to 18V for VDD from 2.6V to 3.6V; 4.5V to 13V for VDD from 2.25V to 2.6V
- $I^2C$  Interface (Slave and Transmitter) - Address: 1001111
- On-Board 7-Bit EEPROM
- Output Adjustment SET Pin
- Output Guaranteed Monotonic Over-Temperature
- Thin 8 Ld 3mmx3mm DFN (0.8mm max)
- Pb-free available (RoHS compliant)

## Applications

- LCD Panels

## Pinout

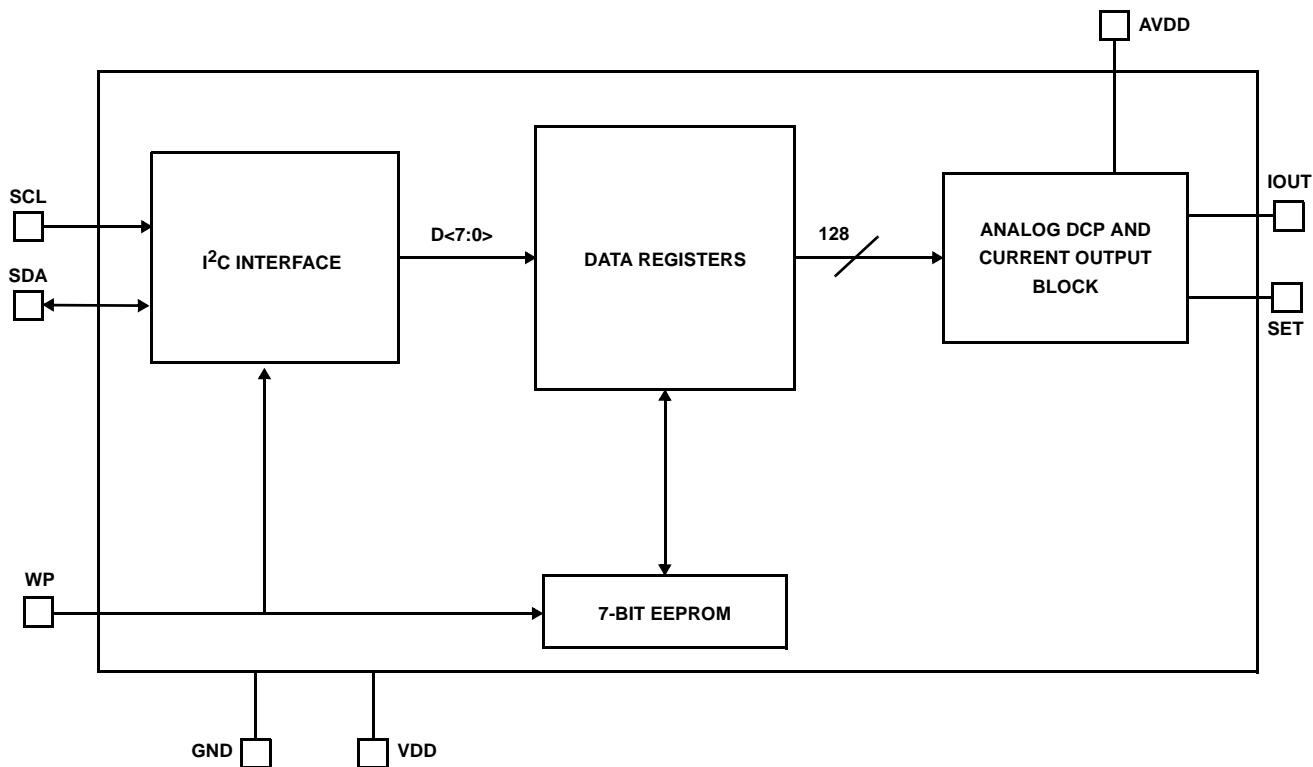


## Pin Descriptions

PIN	TYPE	PULL U/D	FUNCTION
OUT	Output		Adjustable Sink Current Output Pin. The current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maximum adjustable sink current setting.
AVDD	Supply		High-Voltage Analog Supply. Bypass to GND with 0.1μF capacitor.
WP	Input	Pull-Down	Write Protect. Active Low. To enable programming, connect to 0.7*VDD supply or greater.
GND	Supply		Ground connection.
VDD	Supply		System power supply input. Bypass to GND with 0.1μF capacitor.
SDA	In/Out		I <sup>2</sup> C Serial Data Input
SCL	Input		I <sup>2</sup> C Clock Input
SET	Analog		Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AVDD/20) divided by RSET.

## Block Diagram

ISL45041



**Absolute Maximum Ratings**

$V_{DD}$ to GND	.....+4V
Input Voltages to GND	
SET	..... -0.3V to +4V
AVDD	..... -0.3V to +20V
Output Voltages to GND	
OUT	..... -0.3V to +20V
ESD Rating	
HBM for Device	.....2kV
HBM for Input Pins (SCL, SDA)	.....4kV

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
8 Ld TDFN Package	170
Moisture Sensitivity (see Technical Brief TB363)	
All Packages	Level 2
Maximum Junction Temperature (Plastic Package)	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-free reflow profile	see link below
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

**Operating Conditions**

Temperature Range	
ISL45041IR	0°C to +85°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications** Test Conditions:  $V_{DD} = 3V$ ,  $AV_{DD} = 10V$ ,  $OUT = 5V$ ,  $R_{SET} = 24.9k\Omega$ ; Unless Otherwise Specified.  
 Typicals are at  $T_A = +25^\circ C$ 

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
<b>DC CHARACTERISTICS</b>							
$V_{DD}$ Supply Range - Operating	$V_{DD}$		Full	2.25	-	3.6	V
$V_{DD}$ Supply Range - EEPROM Programming	$V_{DD}$		Full	2.25	-	3.6	V
$V_{DD}$ Supply Current	$I_{DD}$	(Note 4)	Full	-	-	50	$\mu A$
AVDD Supply Range	AVDD	$V_{DD}$ Range 2.6V to 3.6V	Full	4.5	-	18	V
		$V_{DD}$ Range 2.25V to 2.6V	Full	4.5	-	13	V
AVDD Supply Current	$I_{AVDD}$	(Note 2)	Full	-	-	25	$\mu A$
SET Voltage Resolution	$SET_{VR}$		Full	7	7	7	Bits
SET Differential Nonlinearity	$SET_{DN}$	Monotonic Over-Temperature	Full	-	-	$\pm 1$	LSB
SET Zero-Scale Error	$SET_{ZSE}$		Full	-	-	$\pm 2$	LSB
SET Full-Scale Error	$SET_{FSE}$		Full	-	-	$\pm 8$	LSB
SET Current	$I_{SET}$	Through $R_{SET}$ (Note 5)	Full	-	20	-	$\mu A$
SET External Resistance	$SET_{ER}$	To GND, $AV_{DD} = 20V$	Full	10	-	200	$k\Omega$
		To GND, $AV_{DD} = 4.5V$	Full	2.25	-	45	$k\Omega$
AVDD to SET Voltage Attenuation	AVDD to SET	(Note 3)	Full	-	1:20	-	V/V
OUT Settling Time	$OUT_{ST}$	to $\pm 0.5$ LSB Error Band (Note 3)	Full	-	8	-	$\mu s$
OUT Voltage Range	$V_{OUT}$		Full	$V_{SET} + 0.5V$	-	13	V
SET Voltage Drift	$SET_{VD}$	(Note 3)	25 to 55	-	<10	-	mV
SDA, SCL, WP Input Logic High	$V_{IH}$		Full	$0.7 \cdot V_{DD}$	-	-	V
SDA, SCL, WP Input Logic Low	$V_{IL}$		Full	-	-	$0.3 \cdot V_{DD}$	V
SDA, SCL, WP Hysteresis		(Note 3)	Full	-	$0.22 \cdot V_{DD}$	-	V
WP IL	$IL_{WPN}$		Full	15	25	35	$\mu A$
SDA, SCL Output Logic High	$VOH_S$	@ 3mA	Full	0.4	-	-	V
SDA, SCL Output Logic Low	$VOL_S$	@ 3mA	Full	-	-	0.4	V

**Electrical Specifications** Test Conditions:  $V_{DD} = 3V$ ,  $AV_{DD} = 10V$ ,  $OUT = 5V$ ,  $R_{SET} = 24.9k\Omega$ ; Unless Otherwise Specified.  
Typicals are at  $T_A = +25^\circ C$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP ( $^\circ C$ )	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
<b>I<sup>2</sup>C</b>							
SCL Clock Frequency	$F_{SCL}$		Full	0	-	400	kHz
I <sup>2</sup> C Clock High Time	$t_{SCH}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Clock Low Time	$t_{SCL}$		Full	1.3	-	-	$\mu s$
I <sup>2</sup> C Spike Rejection Filter Pulse Width	$t_{DSP}$		Full	0	-	50	ns
I <sup>2</sup> C Data Set-up Time	$t_{SDS}$		Full	100	-	-	ns
I <sup>2</sup> C Data Hold Time	$t_{SDH}$		Full	0	-	900	ns
I <sup>2</sup> C SDA, SCL Input Rise Time	$t_{ICR}$	Dependent on Load (Note 6)	Full	-	$20 + 0.1 \cdot C_b$	1000	ns
I <sup>2</sup> C SDA, SCL Input Fall Time	$t_{ICF}$	(Note 6)	Full	-	$20 + 0.1 \cdot C_b$	300	ns
I <sup>2</sup> C Bus Free Time Between Stop and Start	$t_{BUF}$		Full	1.3	-	-	$\mu s$
I <sup>2</sup> C Repeated Start Condition Set-up	$t_{STS}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Repeated Start Condition Hold	$t_{STH}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Stop Condition Set-up	$t_{SPS}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Bus Capacitive Load	$C_b$		Full	-	-	400	pF
Capacitance on SDA	$C_{SDA}$		Full	-	-	10	pF
Capacitance on SCL	$C_S$	WP = 0	Full	-	-	10	pF
		WP = 1		-	-	22	pF
Write Cycle Time	$t_W$		Full	-	-	100	ms

NOTES:

2. Tested at  $AV_{DD} = 20V$ .
3. Simulated and Determined via Design and NOT Directly Tested.
4. Simulated Maximum Current Draw when Programming EEPROM is 23mA, should be considered when designing Power Supply.
5. A Typical Current of 20 $\mu A$  is Calculated using the  $AV_{DD} = 10V$  and  $R_{SET} = 24.9k\Omega$ . Reference "RSET Resistor" on page 5.
6. Simulated and Designed According to I<sup>2</sup>C Specifications.
7. Parts are 100% tested at  $+25^\circ C$ . Over-temperature limits established by characterization and are not production tested.



## I<sup>2</sup>C Timing Diagram

Figure 3 shows the I<sup>2</sup>C timing diagram and expected scope photos of SCL and SDA when writing all zeros or all ones.

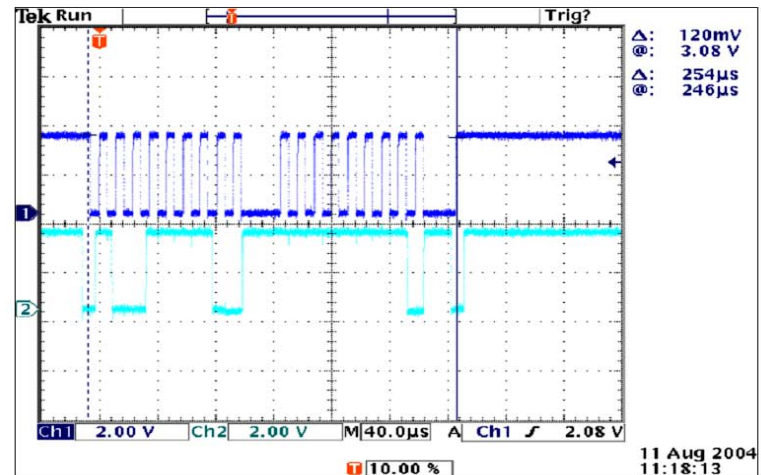
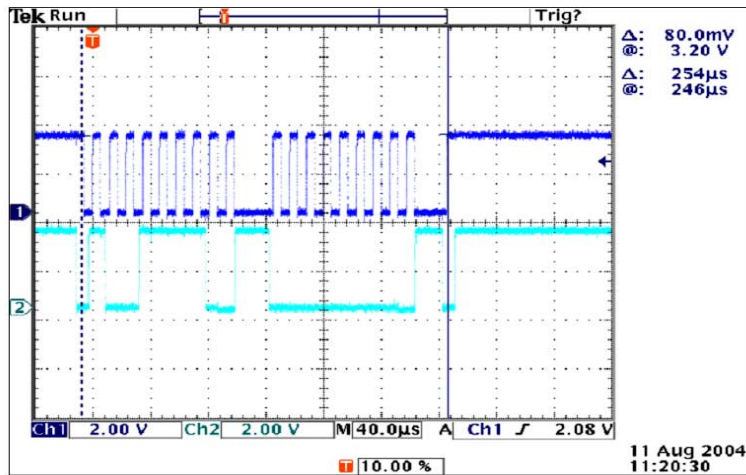
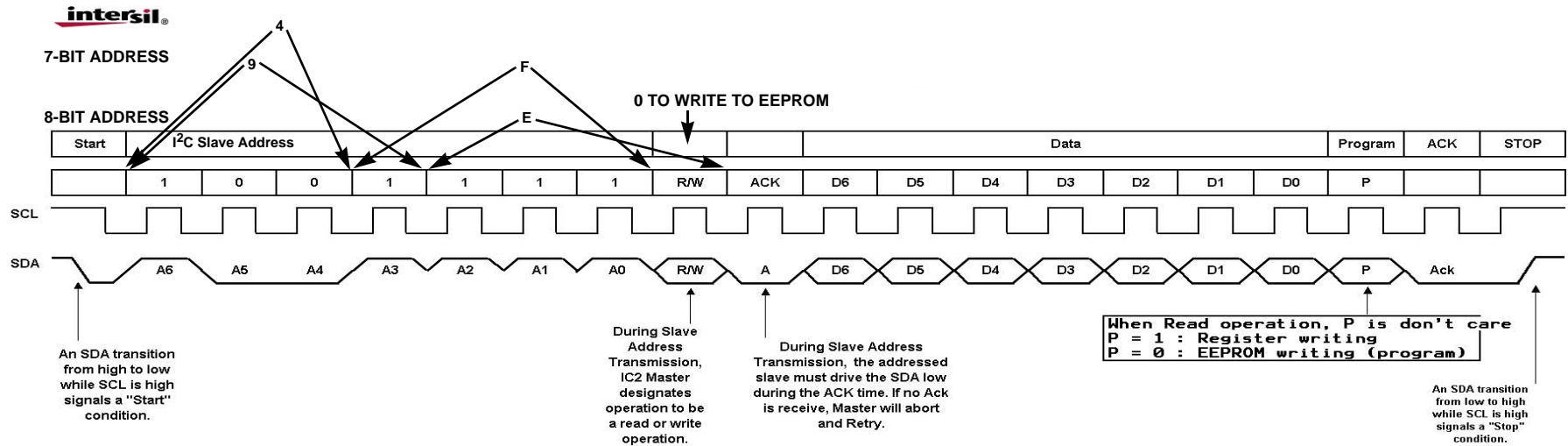
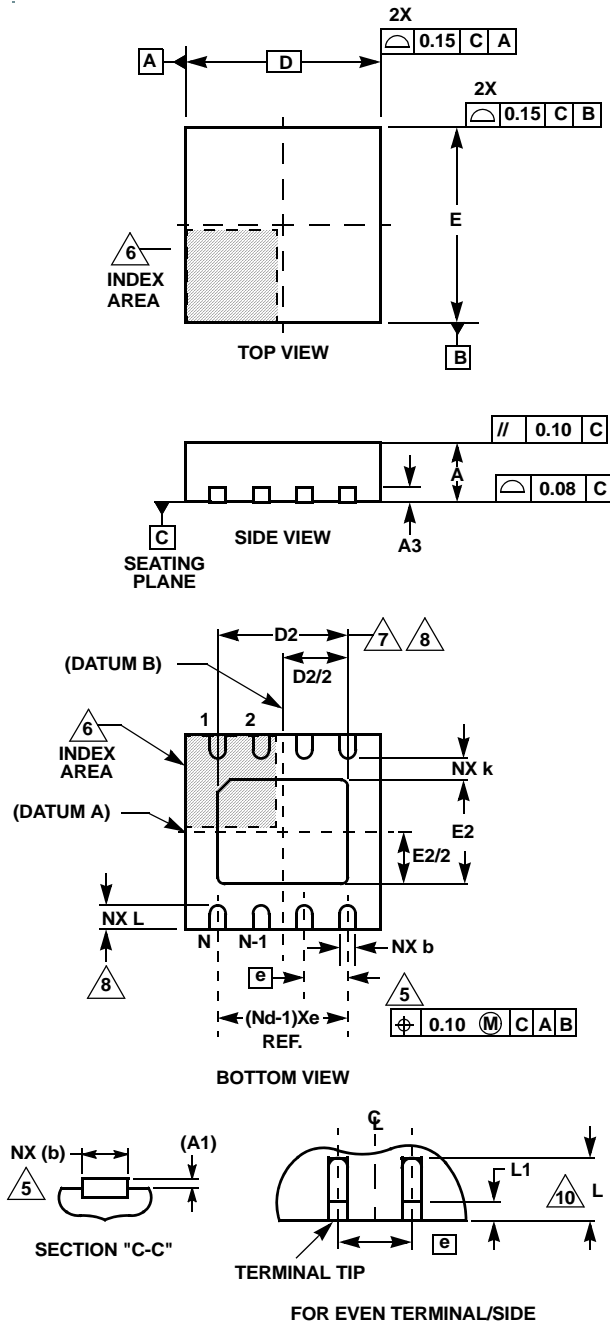


FIGURE 3. ISL45041 I<sup>2</sup>C TIMING DIAGRAM

## Thin Dual Flat No-Lead Plastic Package (TDFN)



## L8.3x3A

## 8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3	0.20 REF			-
b	0.25	0.30	0.35	5, 8
D	3.00 BSC			-
D2	2.20	2.30	2.40	7, 8, 9
E	3.00 BSC			-
E2	1.40	1.50	1.60	7, 8, 9
e	0.65 BSC			-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N	8			2
Nd	4			3

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## NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the "L" min dimension.

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