



Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

General Description

The MAX9178 quad low-voltage differential signaling (LVDS) line driver with high-ESD tolerance is ideal for applications requiring high data rates and low power with reduced noise. The MAX9178 is guaranteed to transmit data at speeds up to 400Mbps (200MHz) over controlled impedance of media of approximately 100Ω. The transmission media can be printed circuit (PC) board traces, backplanes, or cables.

The MAX9178 accepts four LVTTTL/LVCMOS inputs and translates them to LVDS output signals. All inputs tolerate overshoot of $V_{CC} + 1V$ and undershoot of $-1V$. The EN and $\overline{EN}$ inputs are ANDed together and control the high-impedance outputs. When the device is disabled, power drops to ultra-low 12.6mW (typ). Outputs conform to the ANSI TIA/EIA-644 LVDS standard.

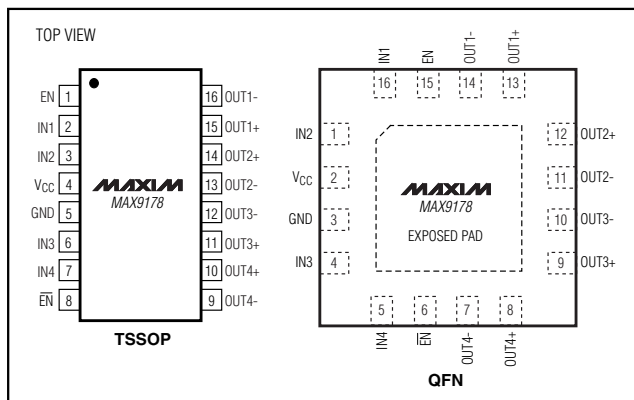
The MAX9178 operates from a single +3.3V supply, and is available in a 16-pin TSSOP and 16-pin thin QFN package with exposed pad. The MAX9178 is specified for operation from $-40^{\circ}C$ to $+85^{\circ}C$.

Applications

Digital Copiers	DSLAMs
Laser Printers	Network
Cell Phone Base Stations	Switches/Routers
Add/Drop Muxes	Backplane
Digital Cross-Connects	Interconnect
	Clock Distribution

Functional Diagram appears at end of data sheet.

Pin Configurations



Features

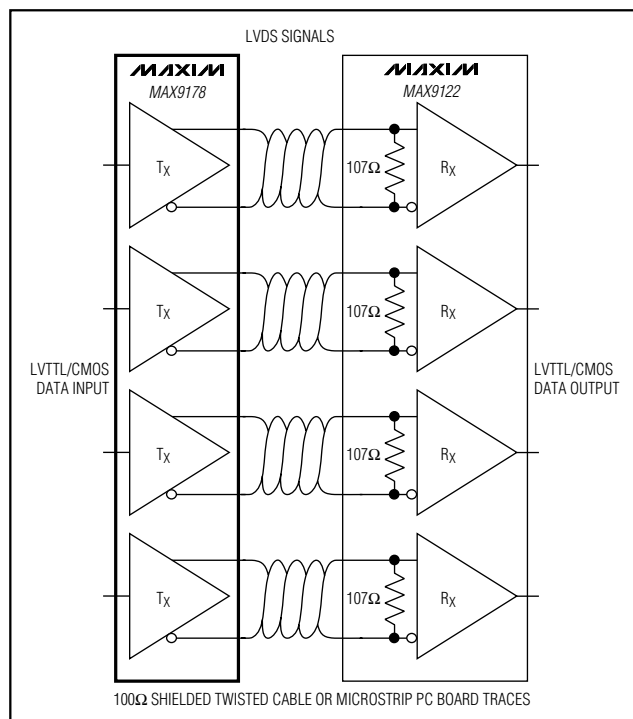
- ◆ Flow-Through Pinout
Simplifies PC Board Layout
Reduces Crosstalk
- ◆ Pin Compatible with DS90LV047A and MAX9123
- ◆ Guaranteed 400Mbps Data Rate
- ◆ Single-Ended Inputs Tolerate 1V Overshoot/Undershoot
- ◆ 250ps Maximum Pulse Skew
- ◆ IEC 61000-4-2 Level 4 ESD Tolerance on LVDS Outputs
- ◆ Conforms to ANSI TIA/EIA-644 LVDS Standard
- ◆ Single +3.3V Supply

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9178EUE	$-40^{\circ}C$ to $+85^{\circ}C$	16 TSSOP
MAX9178ETE	$-40^{\circ}C$ to $+85^{\circ}C$	16 Thin QFN-EP*

*EP = Exposed pad.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +4.0V
 IN₋, EN, $\overline{\text{EN}}$ to GND-1.4V to (V_{CC} + 1.4V)
 OUT₋ to GND-0.3V to +4.0V
 Short-Circuit Duration (OUT₋)Continuous
 Continuous Power Dissipation (T_A = +70°C)
 16-Pin TSSOP (derate 9.4mW/°C above +70°C)755mW
 16-Pin QFN (derate 16.9mW/°C above +70°C)1349mW
 Storage Temperature Range-65°C to +150°C
 Maximum Junction Temperature+150°C

ESD Protection
 Human Body Model
 All Pins to GND±2kV
 OUT₋±2kV
 IEC 61000-4-2 Level 4
 Contact Discharge (OUT₋)±8kV
 Air Discharge (OUT₋)±15kV
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, IN₋ = high or low, EN = high, $\overline{\text{EN}}$ = low, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS OUTPUTS (OUT₊, OUT₋)						
Differential Output Voltage	V _{OD}	Figure 1	250	368	450	mV
Change in Magnitude of V _{OD} Between Complementary Output States	ΔV _{OD}	Figure 1		0.3	25	mV
Offset Voltage	V _{OS}	Figure 1	1.125	1.28	1.375	V
Change in Magnitude of V _{OS} Between Complementary Output States	ΔV _{OS}	Figure 1		0.3	25	mV
Output High Voltage	V _{OH}	Figure 1			1.6	V
Output Low Voltage	V _{OL}	Figure 1	0.90			V
Unterminated Output High Voltage	V _{OHUT}	Output open, Figure 6	1.9			V
Unterminated Output Low Voltage	V _{OLUT}	Output open, Figure 6			0.1	V
Differential Output Short-Circuit Current Magnitude	I _{OSD}	V _{OD} = 0 (Note 3)			9	mA
Output Short-Circuit Current	I _{OS}	OUT ₊ = 0 at IN ₋ = high, or OUT ₋ = 0 at IN ₋ = low			-9	mA
Output High-Impedance Current	I _{OZ}	EN = low and $\overline{\text{EN}}$ = high, OUT ₋ = 0 or V _{CC} , no load	-0.5	±0.002	+0.5	μA
Power-Off Output Current	I _{OFF}	V _{CC} , IN ₋ , EN, $\overline{\text{EN}}$ = 0 or open, OUT ₋ = 0 or 3.6V, no load	-0.5	±0.001	+0.5	μA
INPUTS (IN₋, EN, $\overline{\text{EN}}$)						
High-Level Input Voltage	V _{IH}		2.0		V _{CC} + 1	V
Low-Level Input Voltage	V _{IL}		-1.0		+0.8	V

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, IN_- = high or low, EN = high, $\overline{EN}$ = low, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I _{IN}	0 ≤ IN ₋ , EN, $\overline{EN}$ ≤ V _{CC}	-20	5	+20	μA
		V _{CC} ≤ IN ₋ , EN, $\overline{EN}$ ≤ V _{CC} + 1		0.67	1.5	mA
		-1V ≤ IN ₋ , EN, $\overline{EN}$ ≤ 0	-1.5	-0.46		
SUPPLY CURRENT						
Supply Current	I _{CC}	IN ₋ = V _{CC} or 0, EN = V _{CC} , $\overline{EN}$ = 0, no load		3.8	6.0	mA
	I _{CC} L	IN ₋ = V _{CC} or 0, EN = V _{CC} , $\overline{EN}$ = 0, outputs loaded		18	25	
	I _{CC} Z	IN ₋ = V _{CC} or 0, EN = 0, $\overline{EN}$ = V _{CC}		3.8	6	

SWITCHING CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, $C_L = 15pF$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 4–7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	Figures 2, 3	0.9	1.4	2.0	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figures 2, 3	0.9	1.5	2.0	ns
Differential Pulse Skew	t_{SKD1}	Figures 2, 3 (Note 8)		0.1	0.25	ns
Differential Channel-to-Channel Skew	t_{SKD2}	Figures 2, 3 (Note 9)		0.15	0.35	ns
Differential Part-to-Part Skew	t_{SKD3}	Figures 2, 3 (Note 10)			0.9	ns
	t_{SKD4}	Figures 2, 3 (Note 11)			1.1	
Rise Time	t_R	Figures 2, 3	0.20	0.43	0.70	ns
Fall Time	t_F	Figures 2, 3	0.20	0.41	0.70	ns
Disable Time High to Z	t_{PHZ}	Figures 4, 5		3.9	5	ns
Disable Time Low to Z	t_{PLZ}	Figures 4, 5		3.9	5	ns
Enable Time Z to High	t_{PZH}	Figures 4, 5		5.0	7	ns
Enable Time Z to Low	t_{PZL}	Figures 4, 5		5.0	7	ns
Active to High Time	t_{AH}	$R_L = 80\Omega$ to $132\Omega \pm 1\%$; Figures 6, 7		50	100	ns
High to Active Time	t_{HA}	$R_L = 80\Omega$ to $132\Omega \pm 1\%$; Figures 6, 7 (Note 12)		1.0	1.5	μs
Maximum Operating Frequency	f_{MAX}	(Note 13)	200			MHz

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at $T_A = +85^\circ C$.

Note 2: Currents into the device are positive, and current out of the device is negative. All voltages are referenced to ground except V_{OD} , ΔV_{OD} , V_{OS} , and ΔV_{OS} .

Note 3: Guaranteed by design.

Note 4: AC parameters are guaranteed by design and characterization. Limits are set at ± 6 sigma.

Note 5: C_L includes probe and jig capacitance.

Note 6: Pulse generator output for AC tests: $t_R = t_F = 1ns$ ($0.2 \times V_{CC}$ to $0.8 \times V_{CC}$), 50% duty cycle, $R_O = 50\Omega$, $V_{OH} = V_{CC} + 1V$ settling to V_{CC} , $V_{OL} = -1V$ settling to zero, frequency = 200MHz.

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SWITCHING CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, $C_L = 15pF$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 4–7)

Note 7: Pulse generator output for t_{PHZ} , t_{PLZ} , t_{PZH} , t_{PZL} , t_{AH} , and t_{HA} tests: $t_R = t_F = 1ns$ ($0.2 \times V_{CC}$ to $0.8 \times V_{CC}$), 50% duty cycle, $R_O = 50\Omega$, $V_{OH} = V_{CC} + 1V$ settling to V_{CC} , $V_{OL} = -1V$ settling to zero, frequency = 100kHz.

Note 8: t_{SKD1} is the magnitude of the difference of differential propagation delay. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 9: t_{SKD2} is the magnitude difference of t_{PHLD} or t_{PLHD} of one channel to the t_{PHLD} or t_{PLHD} of another channel on the same device.

Note 10: t_{SKD3} is the magnitude of the difference of any differential propagation delays between devices at the same V_{CC} and within $5^\circ C$ of each other.

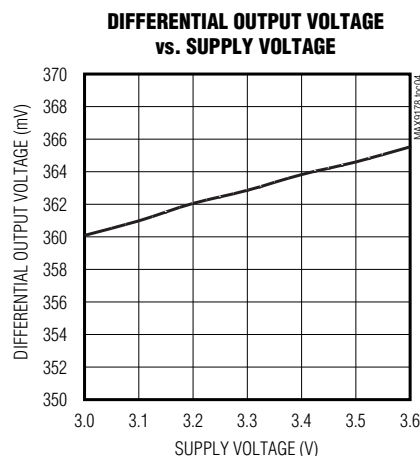
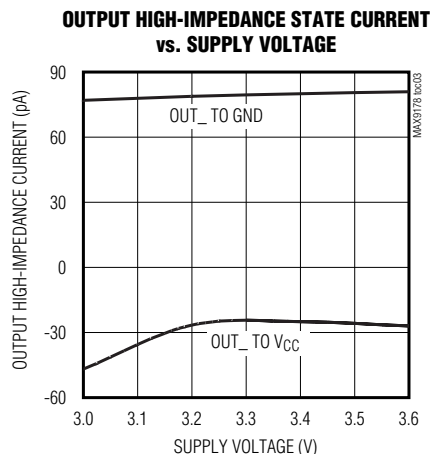
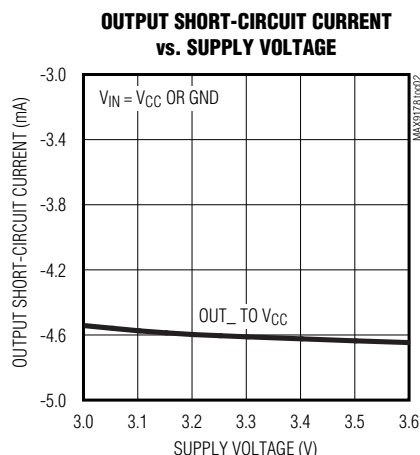
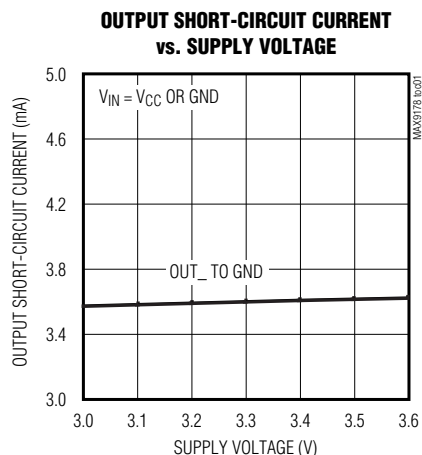
Note 11: t_{SKD4} is the magnitude of the difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

Note 12: After t_{HA} time, all switching characteristics specifications are met.

Note 13: Meets all AC parameters at $f_{MAX} = 200MHz$ with $I_{VOD} \geq 250mV$.

Typical Operating Characteristics

($V_{CC} = +3.3V$, $R_L = 100\Omega$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)

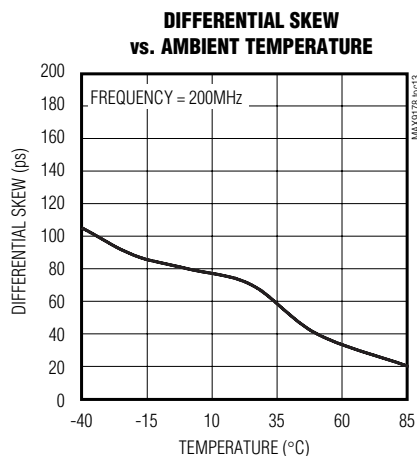
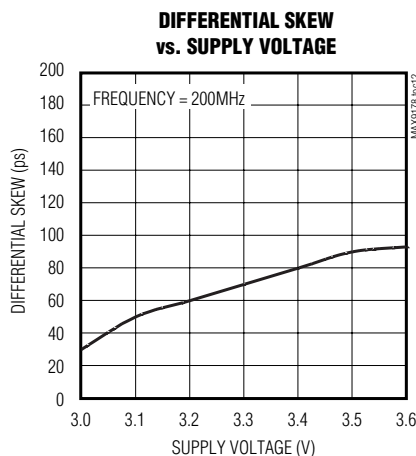
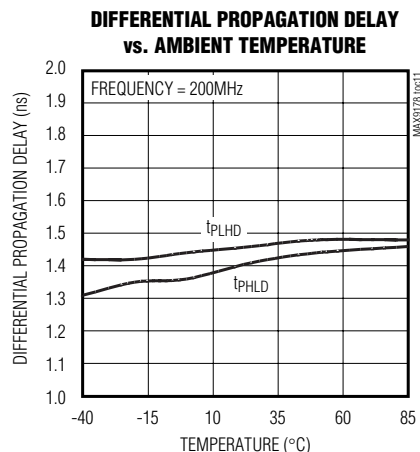
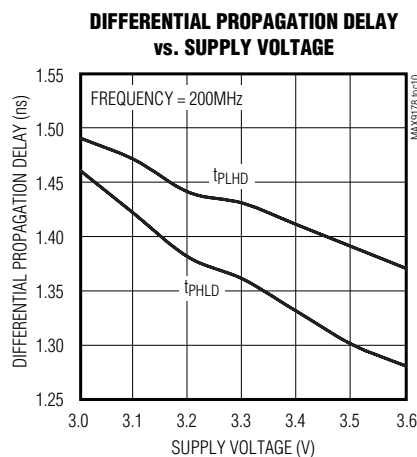
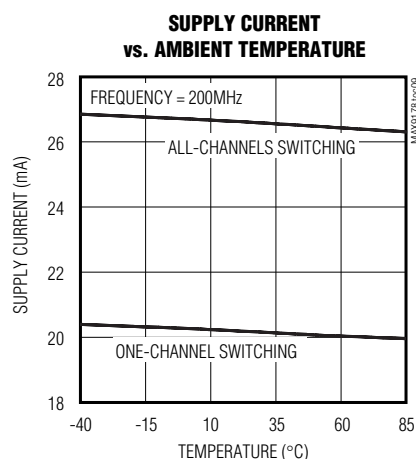
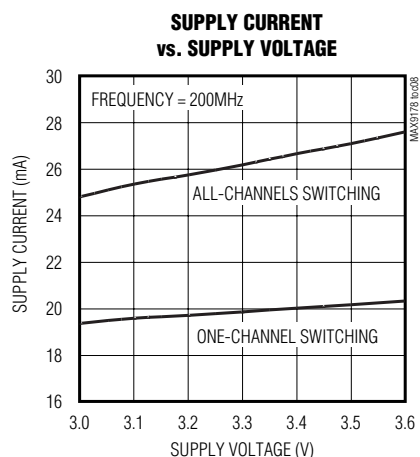
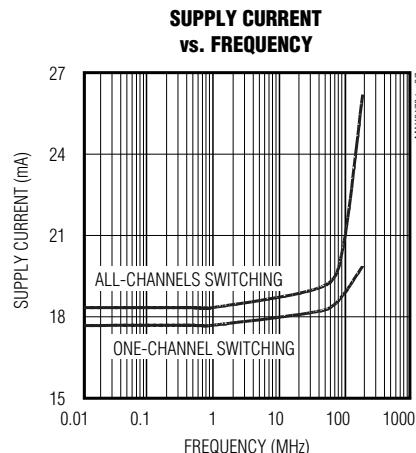
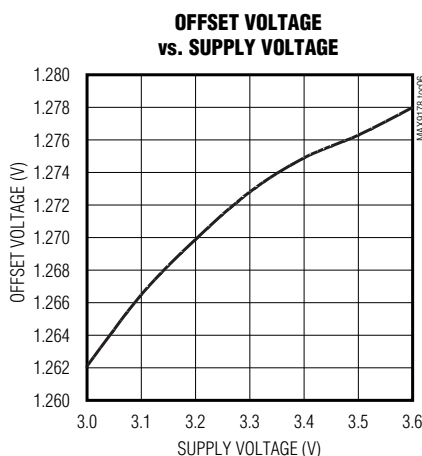
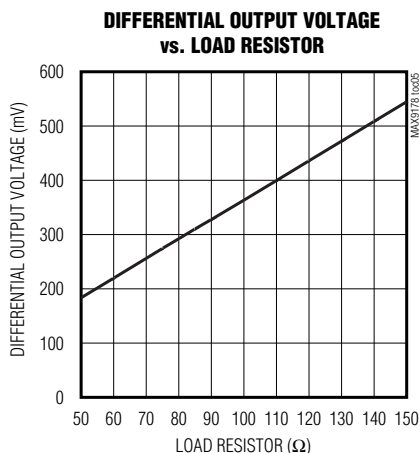


Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $R_L = 100\Omega$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)

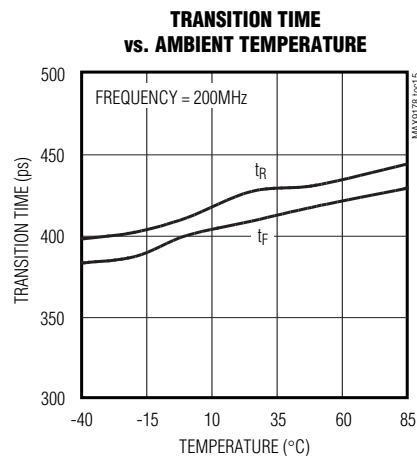
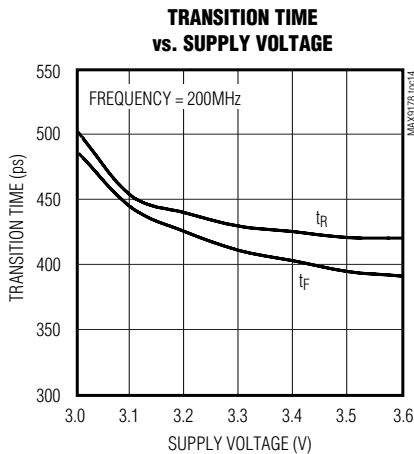
MAX9178



Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_L = 100Ω, C_L = 15pF, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1	15	EN	LVTTL/LVCMOS Enable Input. All outputs are disabled when EN is low. Internally pulled down.
2	16	IN1	LVTTL/LVCMOS Input 1. Input internally pulled down.
3	1	IN2	LVTTL/LVCMOS Input 2. Input internally pulled down.
4	2	V _{CC}	Power-Supply. Bypass V _{CC} to GND with 0.1μF and 0.001μF ceramic capacitors.
5	3	GND	Ground
6	4	IN3	LVTTL/LVCMOS Input 3. Input internally pulled down.
7	5	IN4	LVTTL/LVCMOS input 4. Input internally pulled down.
8	6	$\overline{\text{EN}}$	LVTTL/LVCMOS Inverting Enable Input. All outputs are disabled when $\overline{\text{EN}}$ is high. Internally pulled down.
9	7	OUT4-	Inverting LVDS Output 4
10	8	OUT4+	Noninverting LVDS Output 4
11	9	OUT3+	Noninverting LVDS Output 3
12	10	OUT3-	Inverting LVDS Output 3
13	11	OUT2-	Inverting LVDS Output 2
14	12	OUT2+	Noninverting LVDS Output 2
15	13	OUT1+	Noninverting LVDS Output 1
16	14	OUT1-	Inverting LVDS Output 1
—	EP	Exposed Pad	Exposed Pad. Solder to ground plane.

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Test Circuits/Timing Diagrams

MAX9178

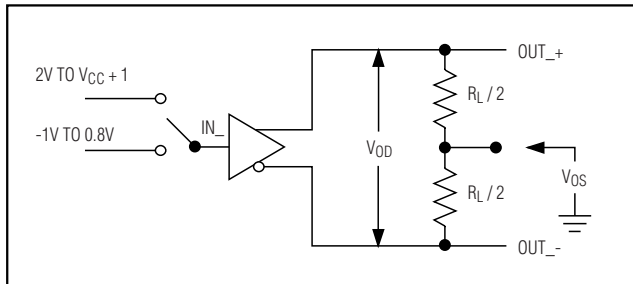


Figure 1. Driver V_{OD} and V_{OS} Test Circuit

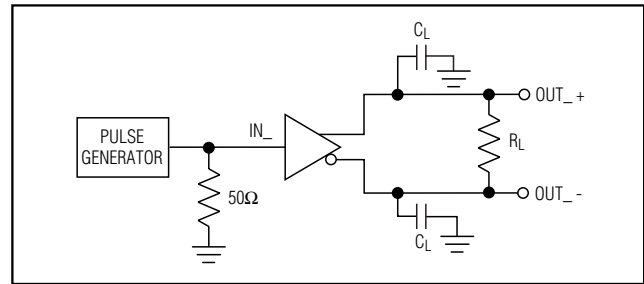


Figure 2. Transition Time and Propagation Delay Test Circuit

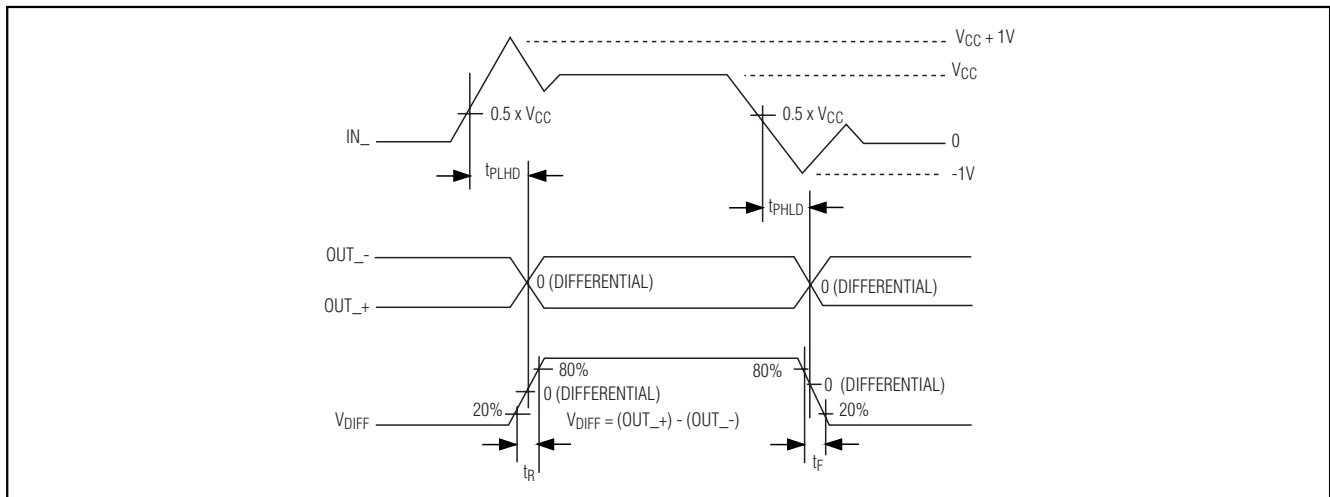


Figure 3. Transition Time and Propagation Delay Waveform Timing

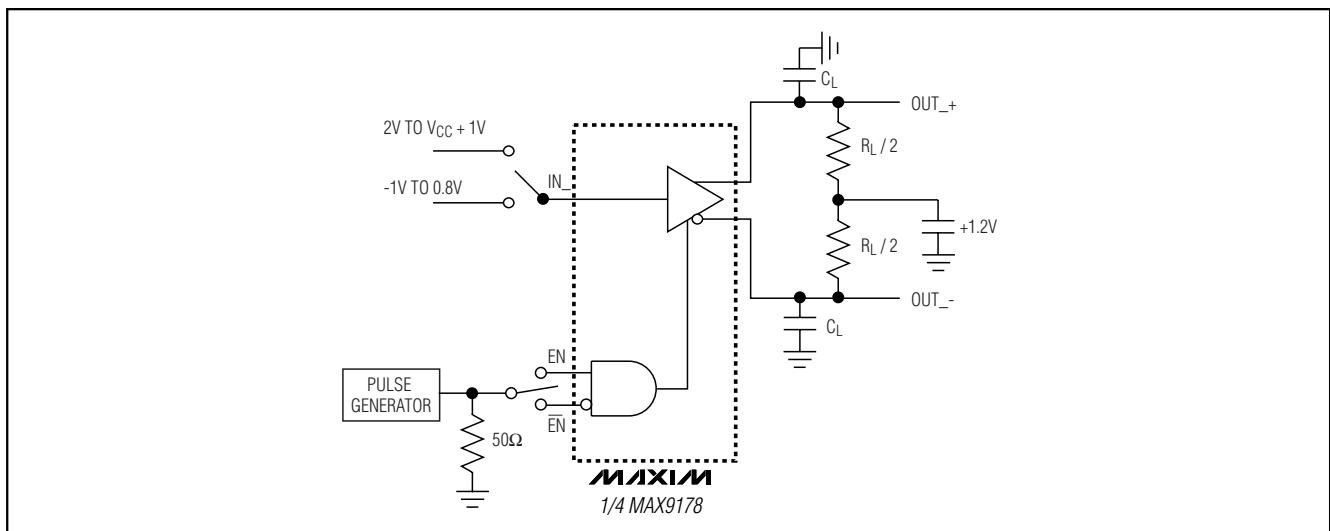


Figure 4. High-Impedance Delay Test Circuit

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Test Circuits/Timing Diagrams (continued)

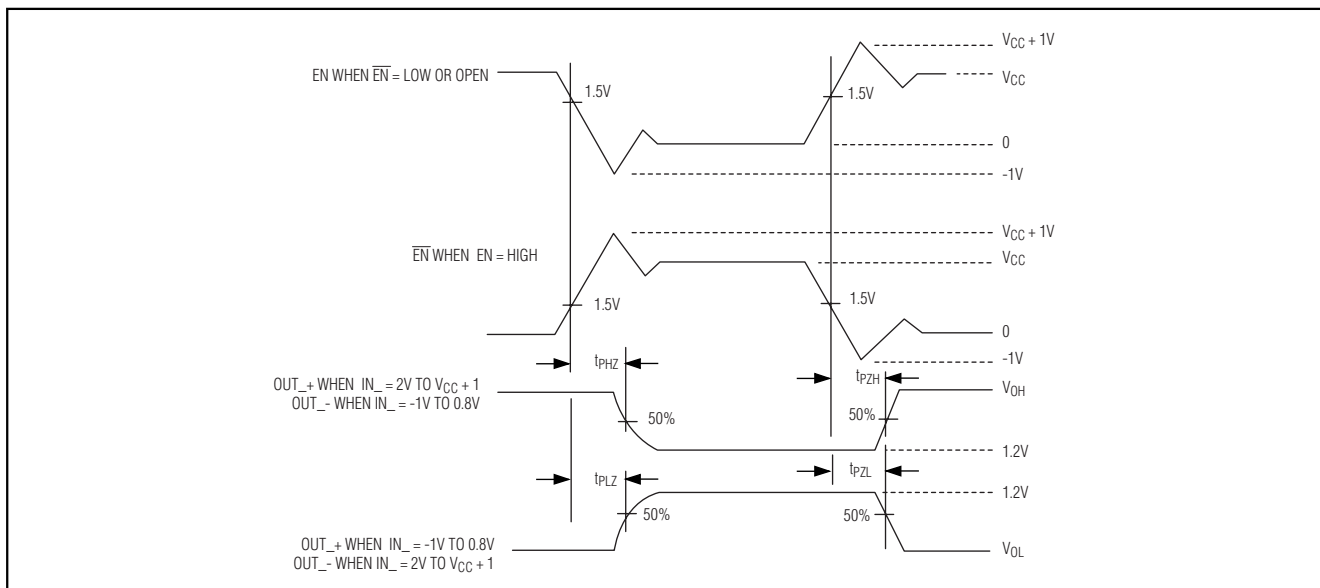


Figure 5. High-Impedance Delay Waveform Timing

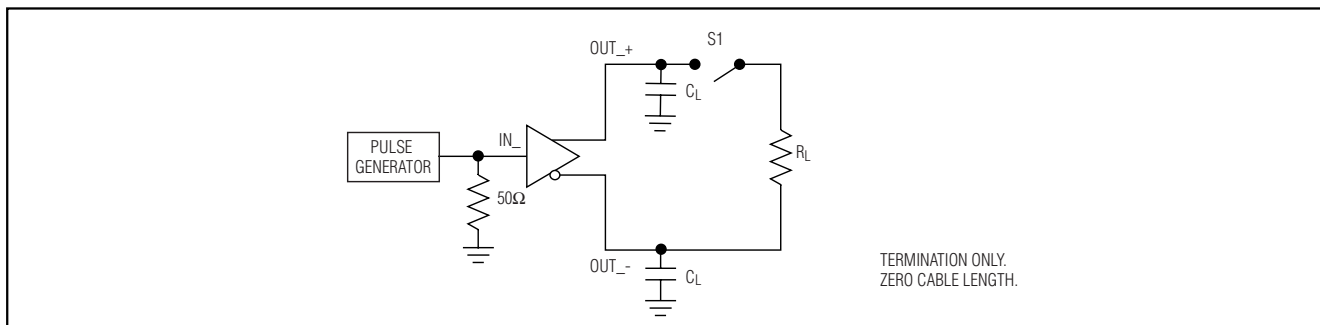


Figure 6. Active-to-High and High-to-Active Test Circuit

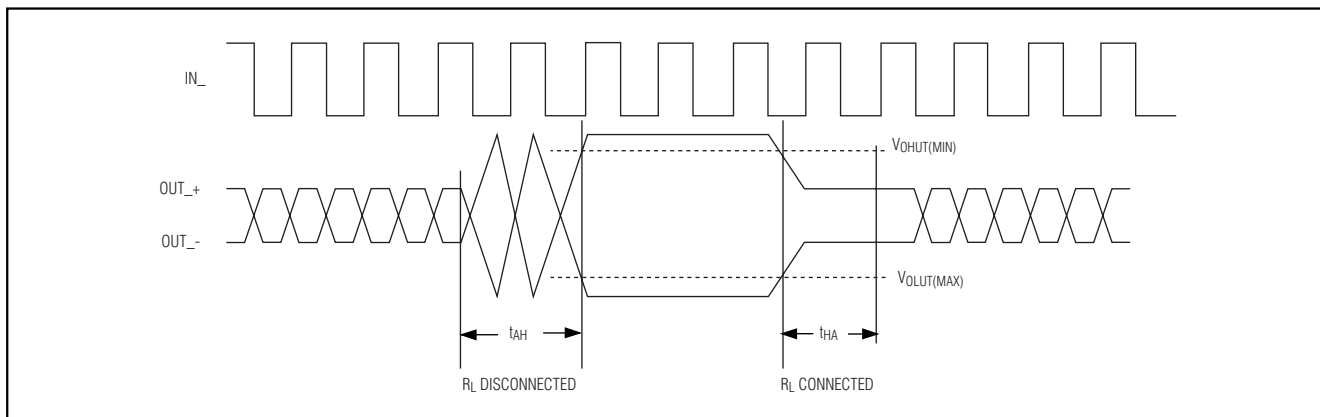


Figure 7. Active-to-High and High-to-Active Timing Diagram

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9178 is a 400Mbps quad differential LVDS driver that is designed for high-speed, point-to-point, and low-power applications. This device accepts LVTTTL/LVCMOS input levels and translates them to LVDS output signals.

The MAX9178 generates a 2.5mA to 4.5mA output current using a current-steering configuration. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited, and enter a high-impedance state when the device is not powered or is disabled.

The current-steering architecture of the MAX9178 requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver. Logic states are determined by the direction of current flow through the termination resistor. With a typical 3.7mA output current, the MAX9178 produces an output voltage of 370mV when driving a 100Ω load.

Termination

The termination resistors should match the differential impedance of the transmission line. Output voltage levels depend upon the value of the termination resistor. The MAX9178 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90Ω and 132Ω, depending on the characteristic impedance of the transmission medium. Table 1 lists the I/O functions.

Termination Detection

The MAX9178 has a limited-capability termination detection circuit at each output that drives the output high when the output termination is removed (or is not present at power-up), and starts the output switching when a termination is connected. These circuits prevent EMI and crosstalk that occur (due to reflections) if an unterminated line is driven.

Table 1. Input/Output Function Table

ENABLES		OUTPUT LOAD	INPUTS	OUTPUTS	
EN	$\overline{\text{EN}}$		IN ₋	OUT ₊	OUT ₋
H	L or open	Connected	L	L	H
			H	H	L
All other combinations of enable inputs		X	X	Z	Z

Z = High impedance.

X = Don't care.

Table 2. Cable Lengths and Frequencies

CONDITIONS	CABLE LENGTH (m)	TYPICAL SWITCHING FREQUENCY (MHz)
100Ω cable termination, 5pF load (each output to ground), 10% to 90% duty cycle	1	10.75
	2	8.5
	4	7.8

Bench testing with CAT-5E unshielded twisted-pair cable showed the termination detection working for the cable lengths and frequencies listed in Table 2. Other combinations of cable length and frequency are possible.

The termination detection worked with 30m of CAT-5 at 3MHz and with alternating 3MHz and 9MHz. The termination detection is prevented from working at various cable lengths, switching frequencies, and data patterns by reflections that discharge the detection circuit.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency, surface-mount ceramic 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Differential Traces

Output trace characteristics affect the performance of the MAX9178. Use controlled-impedance traces to match trace impedance to the transmission medium. Eliminate reflections and ensure that noise couples as common mode by running the differential trace pairs close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

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Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a nominal differential impedance of 100Ω . To minimize impedance discontinuities, use cables and connectors that have matched differential impedance.

Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Overshoot and Undershoot Voltage Protection

The MAX9178 is designed to protect the inputs (IN_{-} , EN , and $\overline{EN}$) against latchup due to transient overshoot and undershoot voltage. If the input voltage goes above V_{CC} or below GND by up to 1V, an internal circuit limits input current to 1.5mA.

IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard specifies ESD tolerance for electronic systems. The IEC 61000-4-2 model (Figure 8) specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9178 outputs are rated for IEC 61000-4-2 level 4 ($\pm 8kV$ Contact Discharge and $\pm 15kV$ Air Discharge). The Human Body Model (HBM, Figure 9) specifies a 100pF capacitor that is discharged into the device through a $1.5k\Omega$ resistor.

The IEC 61000-4-2 circuit discharges higher peak current and more energy than the HBM circuit due to the lower series resistance and larger capacitor.

Board Layout

A four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Separate the LVTTTL/LVCMOS and LVDS signals to prevent coupling.

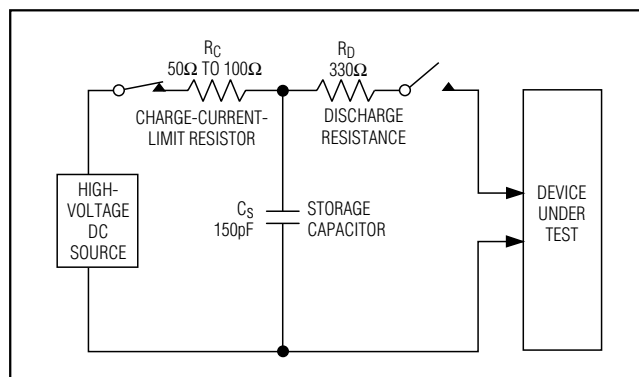


Figure 8. IEC 61000-4-2 Contact Discharge ESD Test Model

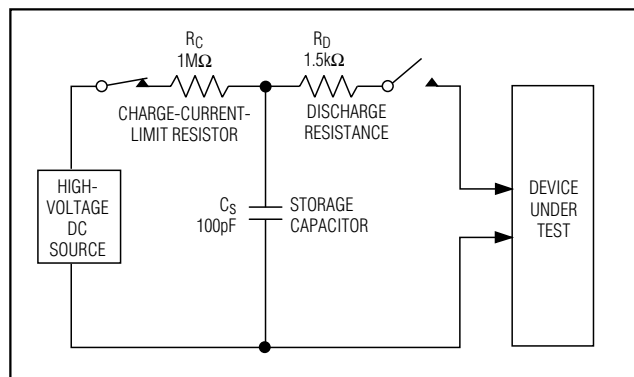
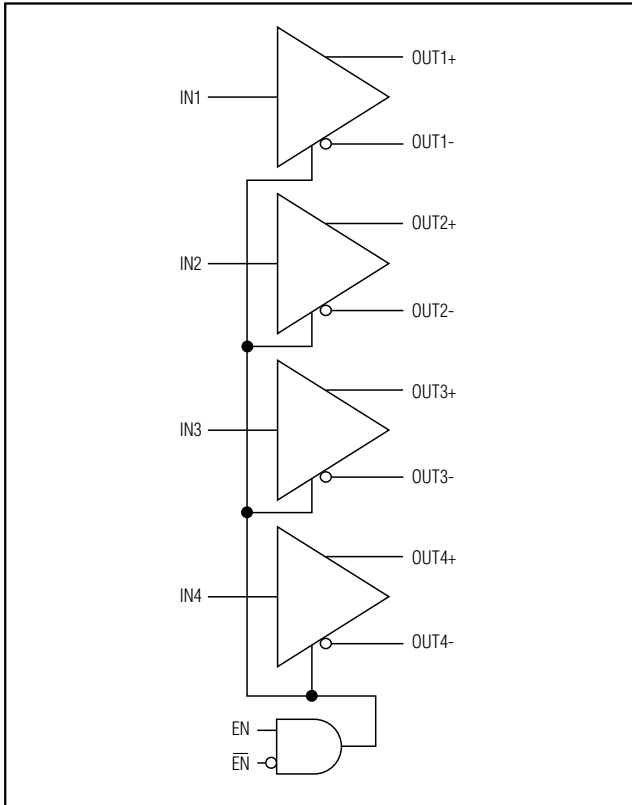


Figure 9. Human Body ESD Test Model

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Functional Diagram



Chip Information

TRANSISTOR COUNT: 1089

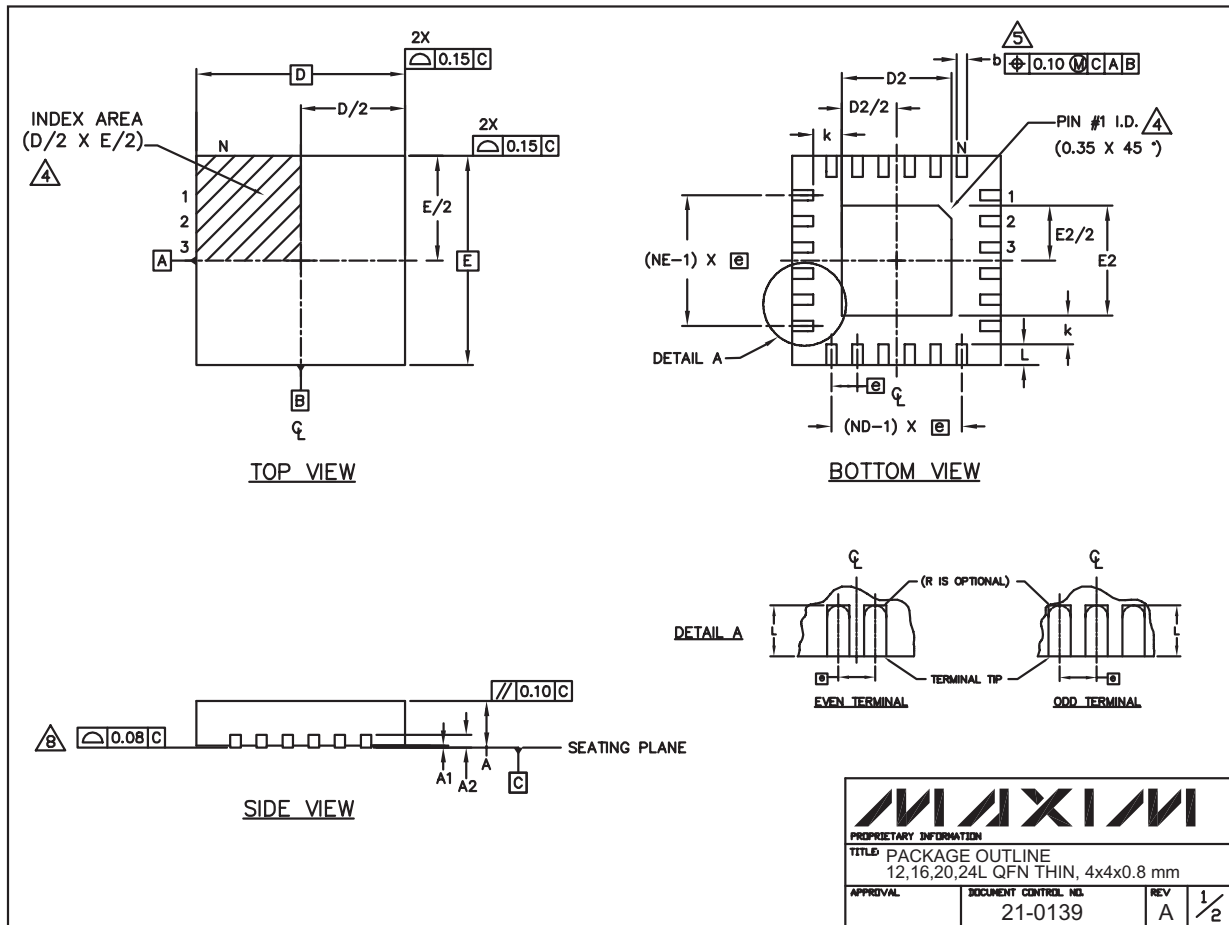
PROCESS: CMOS

MAX9178

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



24L QFN THIN.EPS

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Package Information (continued)

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MAX9178

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
JeDec	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

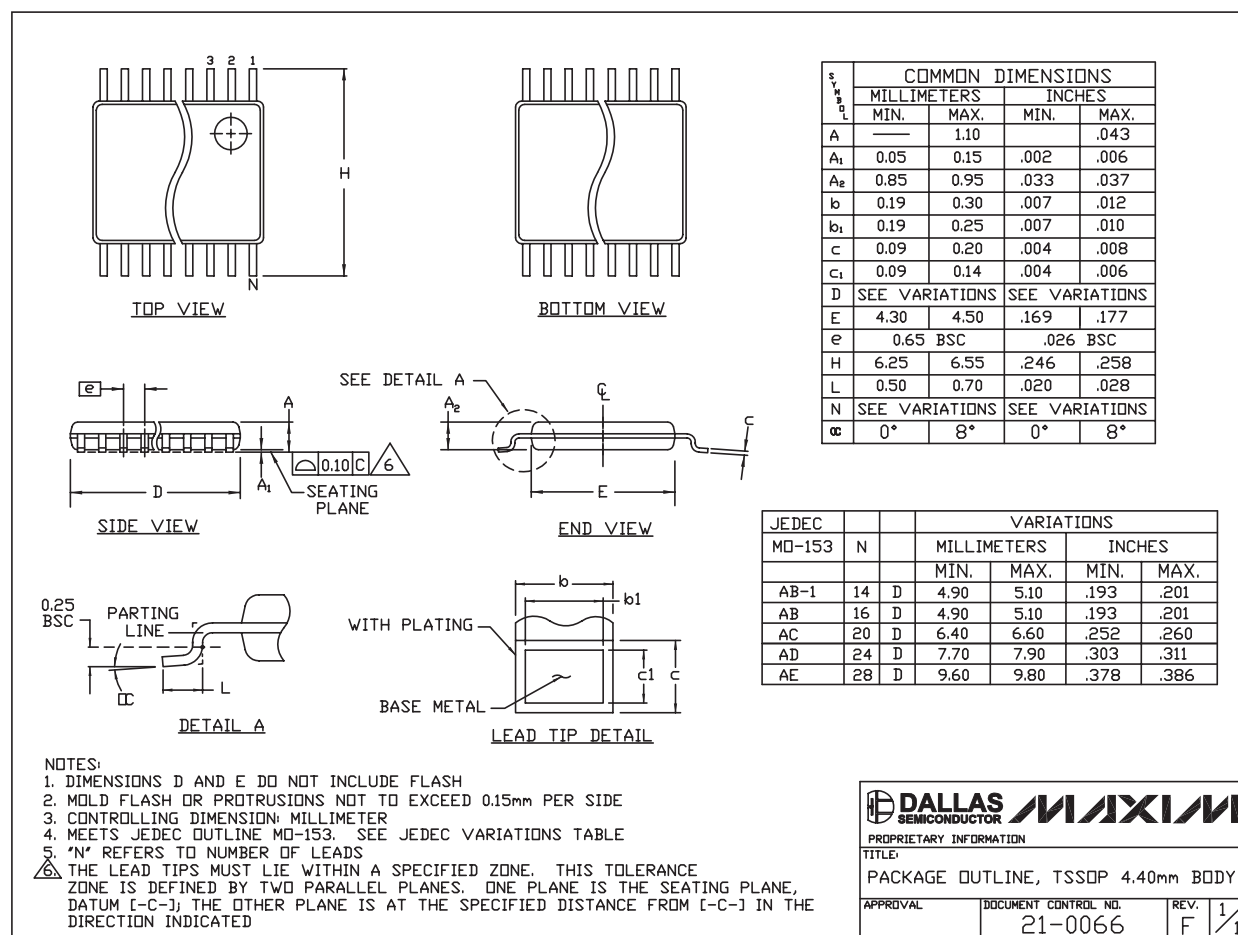
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220.

MAXIM			
PROPRIETARY INFORMATION			
TITLE PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV A	2/2

Quad LVDS Line Driver with High-ESD Tolerance and Flow-Through Pinout

Package Information (continued)

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TSSOP4, 4.0mm EP

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