



# HI-IF Single-Chip Broadband Tuners

## General Description

The MAX3570/MAX3571/MAX3573 low-cost, broadband, dual-conversion tuner ICs are designed for use in digital television receivers. Each IC integrates all necessary RF functions, including an integrated HI-IF filter, fully integrated VCOs, and an integrated IF VGA. The operating frequency range extends from 50MHz to 878MHz while providing over 60dB RF/IF gain-control range. The MAX3570/MAX3571 have an IF frequency centered at 44MHz, while the MAX3573 has an IF output centered at 36MHz.

These devices include a variable-gain front-end, achieving an overall 8dB noise figure. A dual synthesizer generates both local oscillator (LO) frequencies, providing superior phase noise performance of -86dBc/Hz at 10kHz. The integrated HI-IF filter achieves 55dBc (typ) of image rejection. Only an IF SAW filter, passive loop filters, and a crystal are needed to complete a single-chip tuner. Device programming and configuration are accomplished with a 3-wire serial interface for the MAX3570, and with a 2-wire serial interface for the MAX3571/MAX3573.

The MAX3570/MAX3571/MAX3573 are available in a 48-pin QFN-EP package and are specified for the commercial (0°C to +70°C) temperature range.

## Applications

DVB-C Digital Terrestrial Receivers  
ATSC Digital Terrestrial Receivers  
Cable Modems  
DOCSIS/EURO DOCSIS Cable Modems  
ITU J.83 Digital Set-Top Boxes

## Selector Guide

| PART    | SERIAL INTERFACE | IF CENTER FREQUENCY (MHz) |
|---------|------------------|---------------------------|
| MAX3570 | 3-Wire           | 44                        |
| MAX3571 | 2-Wire           | 44                        |
| MAX3573 | 2-Wire           | 36                        |

## Features

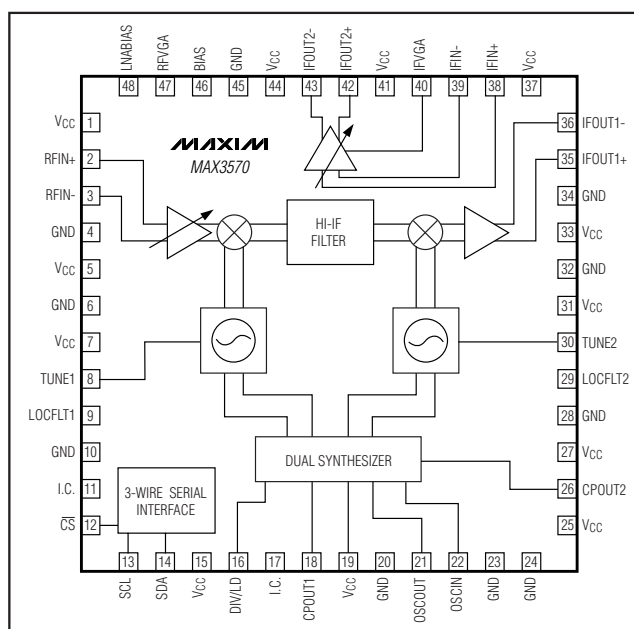
- ◆ Fully Integrated HI-IF Filter
- ◆ Fully Integrated VCOs, No External Components or Traces
- ◆ Low 8dB Noise Figure
- ◆ High Linearity—Greater Than 54dBc, CSO, CTB, X-MOD
- ◆ Industry's Smallest Footprint
- ◆ Superior Phase Noise for 256-QAM, 8-VSB, and COFDM

## Ordering Information

| PART       | TEMP RANGE   | PIN-PACKAGE |
|------------|--------------|-------------|
| MAX3570CGM | 0°C to +70°C | 48 QFN-EP*  |
| MAX3571CGM | 0°C to +70°C | 48 QFN-EP*  |
| MAX3573CGM | 0°C to +70°C | 48 QFN-EP*  |

\*EP = Exposed paddle.

## Pin Configurations/ Functional Diagrams



Pin Configurations/Functional Diagrams continued at end of data sheet.

# HI-IF Single-Chip Broadband Tuners

## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub> to GND .....-0.3V to +5.5V  
 IFIN<sub>-</sub>, IFOUT1<sub>-</sub>, IFOUT2<sub>-</sub>, RFIN<sub>-</sub>, TUNE<sub>-</sub>,  
 LOCFLT<sub>-</sub>, CPOUT<sub>-</sub>, OSCIN, OSCOUT,  
 IFVGA, RFVGA, BIAS, LNABIAS,  
 ADDR<sub>-</sub>, CS, SCL, SDA, DIV/LD.....-0.3V to (V<sub>CC</sub> + 0.3V)

Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 48-Pin QFN (derate 27mW/°C above +70°C) .....2162mW  
 Operating Temperature Range.....0°C to +70°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C



**CAUTION!** ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(MAX357\_ EV kit, V<sub>CC</sub> = +4.75V to +5.25V, R<sub>BIAS</sub> = 5.9kΩ ±1%, no AC signal applied, T<sub>A</sub> = 0°C to +70°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +5.0V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER                           | CONDITIONS                                                | MIN  | TYP | MAX  | UNITS |
|-------------------------------------|-----------------------------------------------------------|------|-----|------|-------|
| SUPPLY VOLTAGE AND SUPPLY CURRENT   |                                                           |      |     |      |       |
| Supply Voltage                      |                                                           | 4.75 |     | 5.25 | V     |
| Supply Current                      | At T <sub>A</sub> = +25°C, V <sub>RFVGA</sub> = +3.0V     | 320  |     |      | mA    |
|                                     | At T <sub>A</sub> = +70°C, V <sub>RFVGA</sub> = +0.5V     | 385  |     |      |       |
| RF and IF VGA Input Bias Current    | V <sub>RFVGA</sub> = V <sub>IFVGA</sub> = +0.5V and +3.0V | -50  |     | +50  | μA    |
| RF and IF VGA Control Voltage       | Maximum gain                                              | 3    |     |      | V     |
|                                     | Minimum gain                                              | 0.5  |     |      |       |
| LOGIC INTERFACE                     |                                                           |      |     |      |       |
| Input-Logic Low (V <sub>IL</sub> )  |                                                           |      |     | 0.9  | V     |
| Input-Logic High (V <sub>IH</sub> ) |                                                           | 2.3  |     |      | V     |
| Input Logic Current                 |                                                           | -10  |     | +10  | μA    |
| Output-Logic Low                    | Sink current = 3mA                                        |      |     | 0.4  | V     |
| Output-Logic High                   | Source current = 3mA                                      | 2.8  |     |      | V     |

# HI-IF Single-Chip Broadband Tuners

## AC ELECTRICAL CHARACTERISTICS

(MAX357\_ EV kit,  $V_{CC} = +4.75V$  to  $+5.25V$ ,  $R_{BIAS} = 5.9k\Omega \pm 1\%$ , **inputs terminated to  $75\Omega$** ,  $f_{RFIN} = 50MHz$  to  $878MHz$ ,  $f_{IF} = 45.75MHz$  (MAX3570/MAX3571),  $f_{IF} = 38.9MHz$  (MAX3573),  $f_{COMP1} = 1MHz$ ,  $f_{COMP2} = 62.5kHz$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                               | CONDITIONS                                                                                                     | MIN  | TYP  | MAX  | UNITS  |
|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------|------|------|--------|
| <b>OVERALL REQUIREMENTS (RF INPUT TO 1st IF OUTPUT)</b> |                                                                                                                |      |      |      |        |
| Operating Frequency Range                               | Gain specification met across this frequency band                                                              | 50   |      | 878  | MHz    |
| Input Return Loss                                       | Worst case across band, $75\Omega$ , any RFXGA setting                                                         |      | 8    |      | dB     |
| Voltage Gain                                            | $Z_{SOURCE} = 75\Omega$ , $Z_{LOAD} = 200\Omega$ , $T_A = +25^\circ C$                                         | 31.5 | 38.5 | 45.0 | dB     |
|                                                         | $V_{RFXGA} = +3.0V$ , $T_A = +70^\circ C$                                                                      | 30.0 | 37   | 43.5 |        |
| Gain-Reduction Range                                    | Measured at 50MHz                                                                                              | 30   |      |      | dB     |
| Gain Flatness                                           | $V_{RFXGA} = +3.0V$ at $f_{RFIN} = 878MHz$ vs. 50MHz                                                           | -1.5 |      | +1.5 | dB     |
|                                                         | $V_{RFXGA} = 0.5V$ at $f_{RFIN} = 878MHz$ vs. 50MHz                                                            | -2   |      | +2   |        |
| Noise Figure                                            | $V_{RFXGA} = +3.0V$                                                                                            |      | 7.9  |      | dB     |
| IIP2                                                    | $V_{RFXGA} = +3.0V$ , $T_A = +25^\circ C$ to $+70^\circ C$ , $V_{CC} = 4.85V$ to $5.15V$ , $f_{RF} = 860MHz$   |      | 34   |      | dBm    |
|                                                         | At 12dB gain reduction, $T_A = +25^\circ C$ to $+70^\circ C$ , $V_{CC} = 4.85V$ to $5.15V$ , $f_{RF} = 860MHz$ |      | 52.5 |      |        |
| IIP3                                                    | $V_{RFXGA} = +3.0V$ , $T_A = +25^\circ C$ to $+70^\circ C$ , $V_{CC} = 4.85V$ to $5.15V$                       |      | +8   |      | dBm    |
|                                                         | At 12dB gain reduction, $T_A = +25^\circ C$ to $+70^\circ C$ , $V_{CC} = 4.85V$ to $5.15V$                     |      | +18  |      |        |
| Beats within Output                                     | 0dBmV PIX carrier level (Note 2)                                                                               |      | -48  |      | dBc    |
| Channel Flatness                                        | From PIX to (PIX + 4) MHz                                                                                      | -0.5 | +0.3 | +1.0 | dB     |
| Isolation                                               | 5MHz to 150MHz, RF input to IF output (Note 3)                                                                 | -63  | -68  |      | dBc    |
| Image Rejection                                         | Measured at 91MHz above desired PIX (MAX3570/MAX3571)                                                          | 50   | 55   |      | dBc    |
|                                                         | Measured at 77.75MHz above desired PIX (MAX3573)                                                               | 50   | 55   |      |        |
| Spurious at RF Input (Note 3)                           | 50MHz to 878MHz                                                                                                |      | -54  | -48  | dBmV   |
|                                                         | Above 878MHz (LO and LO harmonics)                                                                             |      |      | +3   |        |
| Single Sideband Phase Noise                             | $f_{OFFSET} = 1kHz$                                                                                            |      | -62  |      | dBc/Hz |
|                                                         | $f_{OFFSET} = 10kHz$ , $BW_{LOOP} = 2.5kHz$                                                                    |      | -86  |      |        |
|                                                         | $f_{OFFSET} = 100kHz$ , $BW_{LOOP} = 2.5kHz$                                                                   |      | -105 |      |        |
| Output Return Loss                                      | Balanced, $50\Omega$                                                                                           |      | 9    |      | dB     |

MAX3570/MAX3571/MAX3573

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## AC ELECTRICAL CHARACTERISTICS

(MAX357\_ EV kit,  $V_{CC} = +4.75V$  to  $+5.25V$ ,  $R_{BIAS} = 5.9k\Omega \pm 1\%$ , **inputs terminated to  $1k\Omega$** ,  $Z_{LOAD} = 300\Omega$ ,  $f_{IF} = 40MHz$  to  $48MHz$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

| PARAMETER                    | CONDITIONS                                                               | MIN | TYP   | MAX | UNITS     |
|------------------------------|--------------------------------------------------------------------------|-----|-------|-----|-----------|
| <b>SECOND IF STAGE</b>       |                                                                          |     |       |     |           |
| Input Impedance              | Balanced                                                                 |     | 1.7   |     | $k\Omega$ |
| Output Impedance             | Balanced (Note 3)                                                        |     |       | 100 | $\Omega$  |
| Passband Voltage Gain        | $Z_{SOURCE} = 1.1k\Omega$ , $Z_{LOAD} = 300\Omega$ , $V_{IFVGA} = +3.0V$ | 50  | 53    | 57  | dB        |
|                              | $V_{IFVGA} = +0.5V$                                                      |     | 14.5  | 23  |           |
| Passband Flatness            | From PIX to (PIX - 4) MHz for 45.75MHz PIX frequency (Note 3)            |     |       | 0.2 | dB        |
| Maximum Output Voltage       |                                                                          |     | 3.2   |     | $V_{P-P}$ |
| VGA Gain Slope               | $V_{IFVGA} = +3.0V$ to $+0.5V$                                           | 10  |       | 20  | dB/V      |
| -3dB Bandwidth               | (Note 3)                                                                 |     |       | 180 | MHz       |
| Noise Figure                 | $f_{IF} = 44MHz$ , $V_{IFVGA} = +3.0V$                                   |     | 5.1   |     | dB        |
| Noise Figure vs. Attenuation | First 10dB back-off                                                      |     | 0.3   |     | dB/dB     |
| IIP3                         | Gain = 45dB, $V_{OUT} = 1.5V_{P-P}$                                      |     | -27.5 |     | dBm       |
|                              | Gain = 27dB, $V_{OUT} = 1.5V_{P-P}$                                      |     | -11.3 |     |           |
| OIP3                         | $V_{OUT} = 1.5V_{P-P}$ , $V_{IFVGA} = +3.0V$ to $+0.5V$ (Note 3)         |     | 25    |     | dBm       |
| PSRR                         | 50mV $_{P-P}$ at 200kHz                                                  |     | -57   |     | dB        |

# HI-IF Single-Chip Broadband Tuners

MAX3570/MAX3571/MAX3573

## SYNTHESIZER ELECTRICAL CHARACTERISTICS

(MAX357\_ EV kit,  $V_{CC} = +4.75V$  to  $+5.25V$ ,  $R_{BIAS} = 5.9k\Omega \pm 1\%$ ,  $f_{COMP1} = 1MHz$ ,  $f_{COMP2} = 62.5kHz$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                                        | CONDITIONS                    | MIN  | TYP | MAX    | UNITS |
|------------------------------------------------------------------|-------------------------------|------|-----|--------|-------|
| <b>1st LOCAL OSCILLATOR (LO1)</b>                                |                               |      |     |        |       |
| Tuning Range                                                     |                               | 1274 |     | 2111   | MHz   |
| VCO Tuning Gain                                                  |                               | 40   |     | 120    | MHz/V |
| <b>1st LOCAL OSCILLATOR (LO1) DIVIDER</b>                        |                               |      |     |        |       |
| RF1 N-Divider Ratio                                              |                               | 256  |     | 8191   |       |
| RF1 R-Divider Ratio                                              |                               | 1    |     | 31     |       |
| <b>1st LOCAL OSCILLATOR (LO1) PHASE DETECTOR AND CHARGE PUMP</b> |                               |      |     |        |       |
| Phase-Detector Phase Noise                                       | $f_{OFFSET} = 2kHz$ (Note 3)  |      |     | -142   | dBc   |
| Charge-Pump Source/Sink Matching                                 | Correlate locked vs. unlocked |      |     | 6      | %     |
| Charge-Pump Tri-State Current                                    | RF1                           | -7   |     | +7     | nA    |
| <b>2nd LOCAL OSCILLATOR (LO2)</b>                                |                               |      |     |        |       |
| Tuning Range                                                     |                               | 1175 |     | 1193   | MHz   |
| VCO Tuning Gain                                                  |                               | 25   |     | 70     | MHz/V |
| <b>2nd LOCAL OSCILLATOR (LO2) DIVIDER</b>                        |                               |      |     |        |       |
| RF2 N-Divider Ratio                                              |                               | 512  |     | 65,535 |       |
| RF2 R-Divider Ratio                                              |                               | 2    |     | 127    |       |
| <b>2nd LOCAL OSCILLATOR (LO2) PHASE DETECTOR AND CHARGE PUMP</b> |                               |      |     |        |       |
| Phase-Detector Phase Noise                                       | $f_{OFFSET} = 2kHz$ (Note 3)  |      |     | -142   | dBc   |
| Charge-Pump Source/Sink Matching                                 | Correlate locked vs. unlocked |      |     | 6      | %     |
| Charge-Pump Tri-State Current                                    | RF2                           | -7   |     | +7     | nA    |

## LOGIC INTERFACE

(MAX357\_ EV kit,  $V_{CC} = +4.75V$  to  $+5.25V$ ,  $R_{BIAS} = 5.9k\Omega \pm 1\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted.) (Note 1)

| PARAMETER               | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|------------|-----|-----|-----|-------|
| Maximum Clock Frequency |            | 400 |     |     | kHz   |

**Note 1:** These parameters are production tested from  $T_A = +25^\circ C$  to  $+70^\circ C$ , and are guaranteed by design and characterization at  $T_A = 0^\circ C$ .

**Note 2:** When using the tuning table provided in the EV kit documentation.

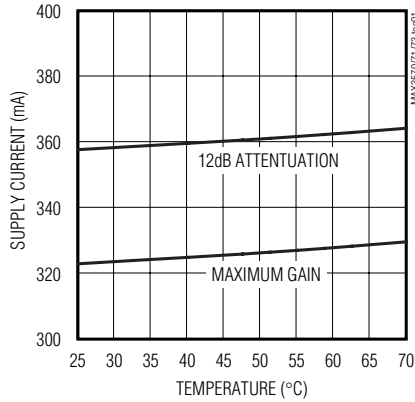
**Note 3:** These parameters are guaranteed by design and characterization, and are not production tested.

# HI-IF Single-Chip Broadband Tuners

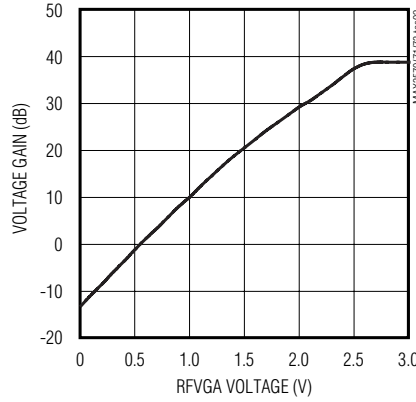
## Typical Operating Characteristics

(MAX357\_ EV kit,  $V_{CC} = +5.0V$ ,  $R_{BIAS} = 5.9k\Omega$ ,  $f_{RF} = 860MHz$ ,  $f_{IF} = 44MHz$  (MAX3570/MAX3571), 36MHz (MAX3573),  $T_A = +25^\circ C$ , unless otherwise noted.)

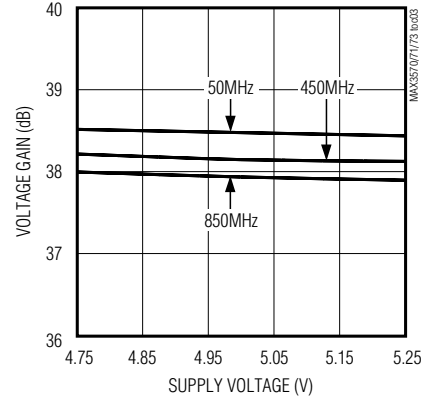
**SUPPLY CURRENT vs. TEMPERATURE**



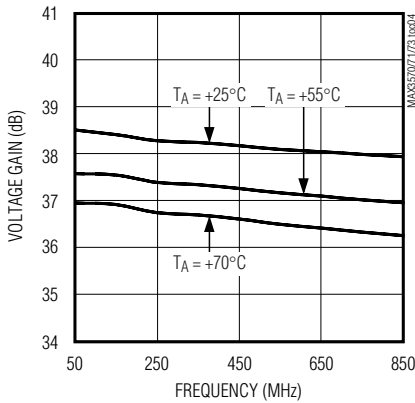
**VOLTAGE GAIN vs. RFVGA VOLTAGE**



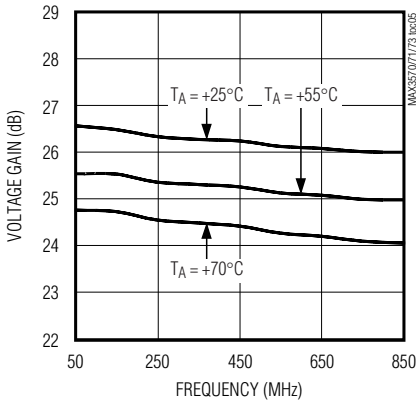
**VOLTAGE GAIN vs. SUPPLY VOLTAGE**



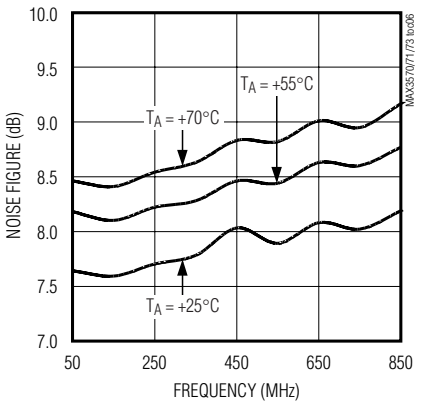
**VOLTAGE GAIN vs. FREQUENCY (MAX GAIN)**



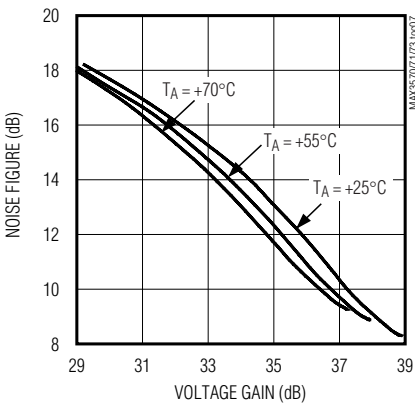
**VOLTAGE GAIN vs. FREQUENCY (MAX -12dB)**



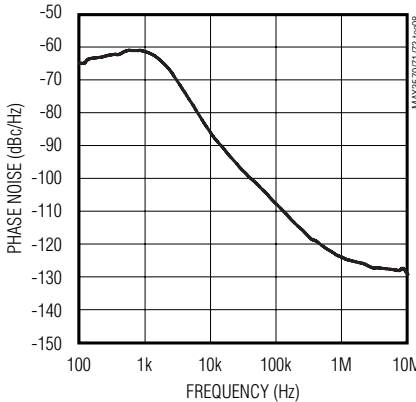
**NOISE FIGURE vs. FREQUENCY**



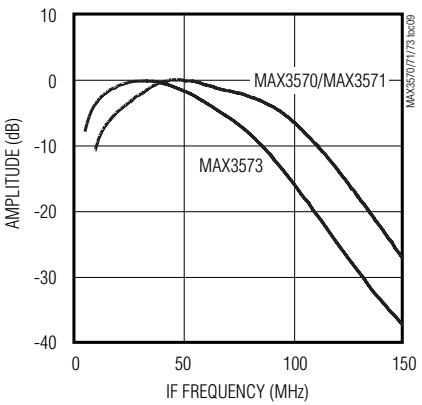
**NOISE FIGURE vs. VOLTAGE GAIN**



**PHASE NOISE vs. OFFSET FREQUENCY**



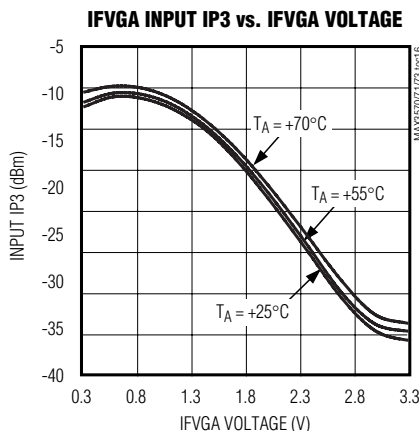
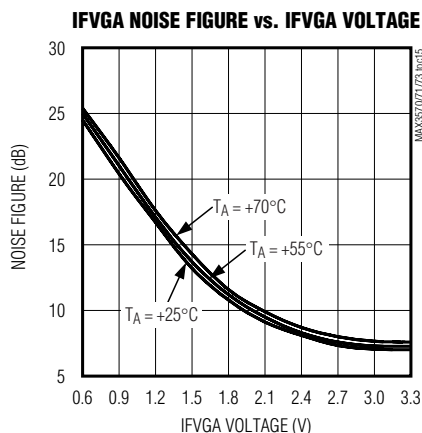
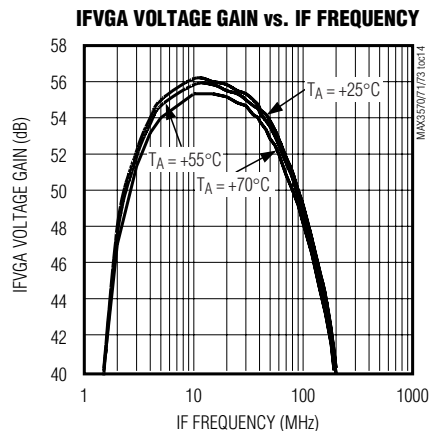
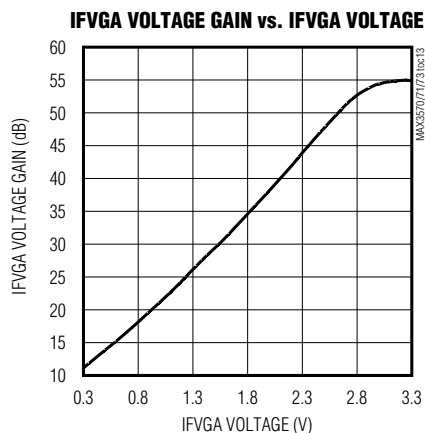
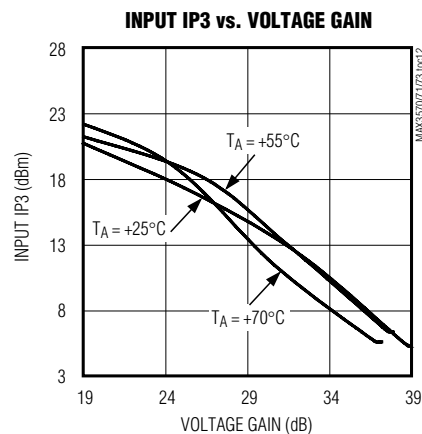
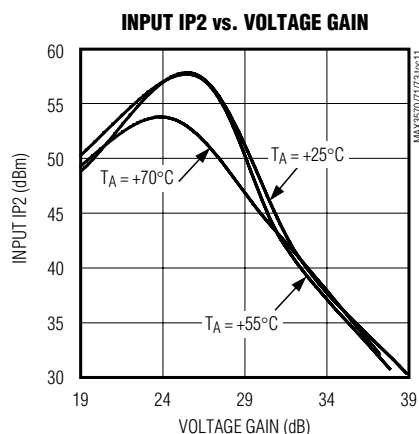
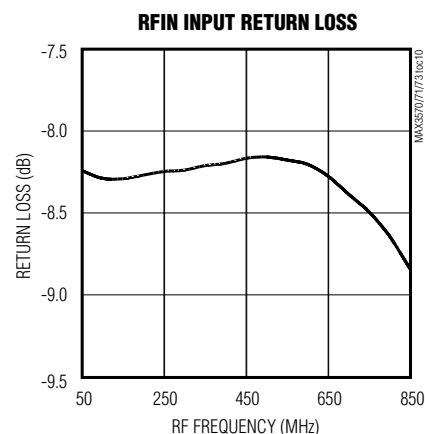
**IFOUT1 FREQUENCY RESPONSE**



# HI-IF Single-Chip Broadband Tuners

## Typical Operating Characteristics (continued)

(MAX357\_ EV kit,  $V_{CC} = +5.0V$ ,  $R_{BIAS} = 5.9k\Omega$ ,  $f_{RF} = 860MHz$ ,  $f_{IF} = 44MHz$  (MAX3570/MAX3571),  $36MHz$  (MAX3573),  $T_A = +25^\circ C$ , unless otherwise noted.)



MAX3570/MAX3571/MAX3573

# HI-IF Single-Chip Broadband Tuners

## Pin Description

| PIN                                           | NAME            | FUNCTION                                                                                                                                                                         |
|-----------------------------------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                             | V <sub>CC</sub> | RF Variable-Gain Amplifier (VGA) Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches. |
| 2, 3                                          | RFIN+,<br>RFIN- | Differential LNA Inputs. Requires AC coupling and can be driven balanced or single-ended. Recommend driving pin 3 and AC ground pin 2 for optimum input IP2 performance.         |
| 4, 6, 10,<br>20, 23,<br>24, 28,<br>32, 34, 45 | GND             | Ground. Connect to PC board ground plane.                                                                                                                                        |
| 5                                             | V <sub>CC</sub> | 1st Mixer Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                        |
| 7                                             | V <sub>CC</sub> | 1st VCO Circuitry Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                |
| 8                                             | TUNE1           | 1st VCO Tuning Input. Connect this analog voltage input to a third-order loop-filter output.                                                                                     |
| 9                                             | LOCFLT1         | 1st LO Noise-Filtering Capacitor Connection. Connect a capacitor to GND. (Refer to the EV kit.)                                                                                  |
| 11                                            | I.C.            | Internal Connection. Leave this pin unconnected (MAX3570).                                                                                                                       |
|                                               | ADDR2           | 2-Wire Serial Interface 2nd Address Pin (MAX3571/MAX3573)                                                                                                                        |
| 12                                            | CS              | 3-Wire Serial Interface Enable Input Pin (SPI™/QSPI™/MICROWIRE™ Compatible) (MAX3570)                                                                                            |
|                                               | ADDR1           | 2-Wire Serial Interface 1st Address Pin (MAX3571/MAX3573)                                                                                                                        |
| 13                                            | SCL             | 3-Wire Serial Interface Clock Input Pin (SPI/QSPI/MICROWIRE Compatible) (MAX3570)                                                                                                |
|                                               |                 | 2-Wire Serial Interface Clock Input Pin (MAX3571/MAX3573)                                                                                                                        |
| 14                                            | SDA             | 3-Wire Serial Interface Data Input Pin (SPI/QSPI/MICROWIRE Compatible) (MAX3570)                                                                                                 |
|                                               |                 | 2-Wire Serial Interface Data Input Pin (MAX3571/MAX3573)                                                                                                                         |
| 15                                            | V <sub>CC</sub> | Digital Circuitry Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                |
| 16                                            | DIV/LD          | Divider or Lock-Detect Logic Output                                                                                                                                              |
| 17                                            | I.C.            | Internal Connection. Leave this pin unconnected.                                                                                                                                 |
| 18                                            | CPOUT1          | 1st PLL Charge-Pump Output. Connect this high-impedance current output to a third-order loop-filter input.                                                                       |
| 19                                            | V <sub>CC</sub> | 1st Synthesizer Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                  |
| 21                                            | OSCOU           | Reference Oscillator Buffered Output                                                                                                                                             |
| 22                                            | OSCIN           | Reference Oscillator Input. Connect an external reference oscillator or crystal to this analog input through a coupling capacitor.                                               |
| 25                                            | V <sub>CC</sub> | 2nd Synthesizer Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                  |
| 26                                            | CPOUT2          | 2nd PLL Charge-Pump Output. Connect this high-impedance current output to a third-order loop-filter input.                                                                       |

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MICROWIRE is a trademark of National Semiconductor Corp.

# HI-IF Single-Chip Broadband Tuners

## Pin Description (continued)

| PIN    | NAME                | FUNCTION                                                                                                                                                                                                                                                                                     |
|--------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27     | V <sub>CC</sub>     | 2nd Charge-Pump Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                                                                                                                              |
| 29     | LOCFLT2             | 2nd LO Noise-Filtering Capacitor Connector. Connect a capacitor to GND. (Refer to the EV kit.)                                                                                                                                                                                               |
| 30     | TUNE2               | 2nd VCO Tuning Input. Connect this analog voltage input to a third-order loop-filter output.                                                                                                                                                                                                 |
| 31     | V <sub>CC</sub>     | 2nd VCO Circuitry Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                                                                                                                            |
| 33     | V <sub>CC</sub>     | 2nd LO Generation Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                                                                                                                            |
| 35, 36 | IFOUT1+,<br>IFOUT1- | 1st Differential IF Outputs. These outputs are AC-coupled to the SAW filter inputs.                                                                                                                                                                                                          |
| 37     | V <sub>CC</sub>     | 2nd Mixer and 1st IF Amplifier Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                                                                                                       |
| 38, 39 | IFIN+,<br>IFIN-     | Differential IF Inputs. Connected to the SAW filter outputs.                                                                                                                                                                                                                                 |
| 40     | IFVGA               | IF VGA Control. See the <i>Typical Operating Characteristics</i> .                                                                                                                                                                                                                           |
| 41     | V <sub>CC</sub>     | IF VGA Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                                                                                                                                       |
| 42, 43 | IFOUT2+,<br>IFOUT2- | IF VGA Outputs                                                                                                                                                                                                                                                                               |
| 44     | V <sub>CC</sub>     | HI-IF Filter Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with any other branches.                                                                                                                         |
| 46     | BIAS                | Bias Resistor Connection. Connect a 5.9k $\Omega$ precision $\pm 1\%$ resistor to GND. Resistor value can be increased to decrease the nominal current at the expense of linearity. Refer to Application Note: <i>MAX3570/MAX3571/MAX3573 Bias Resistor Setting</i> for further information. |
| 47     | RFVGA               | RF VGA Control. See the <i>Typical Operating Characteristics</i> .                                                                                                                                                                                                                           |
| 48     | LNABIAS             | LNA Bias Input. Connect through an inductor to GND. (Refer to the EV kit.)                                                                                                                                                                                                                   |
| EP     | GND                 | Exposed Ground Paddle. DC and AC GND return for the IC. Connect to PC board ground plane using multiple vias.                                                                                                                                                                                |

MAX3570/MAX3571/MAX3573

# HI-IF Single-Chip Broadband Tuners

## Detailed Description

### Programmable Registers

The MAX3570/MAX3571/MAX3573 include nine programmable registers (registers 1–9) consisting of six divider registers (registers 1–6), one VCO control register (register 7), and one test register (register 8). The final register (register 9) controls the HI-IF filter frequency offset, as well as the DIV/LD output MUX status. Most registers contain some don't care (X) bits. These can be either a "0" or a "1" and do not affect the mode of operation (Table 1). Data is shifted in MSB first. Positive logic is used.

### 3-Wire Serial Interface

The MAX3570 uses a 3-wire SPI/QSPI/MICROWIRE-compatible serial interface. An active-low chip select ( $\overline{CS}$ ) enables the device to receive data from the serial input (SDA). Register address and data information are clocked in on the rising edge of the serial clock signal (SCL). While shifting in the serial data, the device remains in its original configuration. A rising edge on  $\overline{CS}$  latches the data into the MAX3570's internal register, initiating the device's change of state. Figure 1 shows the details of the 3-wire interface address and data configuration.

Figure 1. 3-Wire Serial Interface Address and Data Configuration

|                |    |    |    |             |    |    |    |    |    |    |    |     |
|----------------|----|----|----|-------------|----|----|----|----|----|----|----|-----|
| MSB            |    |    |    |             |    |    |    |    |    |    |    | LSB |
| 4 ADDRESS BITS |    |    |    | 8 DATA BITS |    |    |    |    |    |    |    |     |
| A3             | A2 | A1 | A0 | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |     |

Figure 2. 2-Wire Serial Interface Register Write Example

|       |                        |     |                  |     |       |     |       |     |      |
|-------|------------------------|-----|------------------|-----|-------|-----|-------|-----|------|
| START | DEVICE ADDRESS         | ACK | REGISTER ADDRESS | ACK | DATA  | ACK | DATA  | ACK | STOP |
|       | 8b11000<ADDR2><ADDR1>0 |     | 8b0000XXXX       |     | D7–D0 |     | D7–D0 |     |      |

Figure 3. 2-Wire Serial Interface Register Read Example

|       |                        |     |                    |      |      |
|-------|------------------------|-----|--------------------|------|------|
| START | DEVICE ADDRESS         | ACK | READ BYTE (8 Bits) | NACK | STOP |
|       | 8b11000<ADDR2><ADDR1>1 |     | 8bXXXXXXX          |      |      |

### 2-Wire Serial Interface

The MAX3571/MAX3573 use a 2-wire I<sup>2</sup>C\*-compatible serial interface. The serial bus is monitored continuously, waiting for a START condition followed by its address. The address has 5 MSB internally set, while the next two bits are set with external pins, ADDR2 and ADDR1. The LSB determines whether it is a read or write. When the device recognizes its address, it acknowledges by pulling the SDA line low for one clock period; it is then ready to accept the register address for the first byte of data. Another acknowledge (ACK) is sent once the register address is received. The device is then ready to accept the data byte. More data bytes can be sent for sequential registers, and ACK is sent after each byte. After the final ACK is sent, the master issues a STOP condition to free the bus. Figure 2 shows the details of the 2-wire interface structure.

There is only one read-back register in the MAX3571/MAX3573. To access it, send a START condition, and then the read address is set by the external ADDR2 and ADDR1 pins. An ACK is sent, and the master then begins to read from the slave. After the eight bits have been read, the master should issue a no-acknowledge (NACK), and then a STOP condition.

Table 1. 2-Wire Serial Interface Address Configuration (Set by ADDR2 and ADDR1)

| ADDRESS (WRITE/READ) | ADDR2 | ADDR1 |
|----------------------|-------|-------|
| C0/C1 <sub>hex</sub> | Low   | Low   |
| C2/C3 <sub>hex</sub> | Low   | High  |
| C4/C5 <sub>hex</sub> | High  | Low   |
| C6/C7 <sub>hex</sub> | High  | High  |

\*Purchase of I<sup>2</sup>C components of Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

# HI-IF Single-Chip Broadband Tuners

**Table 2. Register Configuration**

| REGISTER NUMBER | REGISTER NAME | REGISTER ADDRESS  | 8 DATA BITS |       |       |      |      |      |      |      | MSB | LSB |
|-----------------|---------------|-------------------|-------------|-------|-------|------|------|------|------|------|-----|-----|
|                 |               |                   | D7          | D6    | D5    | D4   | D3   | D2   | DB1  | D0   |     |     |
|                 |               |                   |             |       |       |      |      |      |      |      |     |     |
| 1               | VCO1_N1       | 00 <sub>hex</sub> | X           | X     | X     | 1N12 | 1N11 | 1N10 | 1N9  | 1N8  |     |     |
| 2               | VCO1_N2       | 01 <sub>hex</sub> | 1N7         | 1N6   | 1N5   | 1N4  | 1N3  | 1N2  | 1N1  | 1N0  |     |     |
| 3               | VCO1_R        | 02 <sub>hex</sub> | X           | X     | X     | 1R4  | 1R3  | 1R2  | 1R1  | 1R0  |     |     |
| 4               | VCO2_N1       | 03 <sub>hex</sub> | 2N15        | 2N14  | 2N13  | 2N12 | 2N11 | 2N10 | 2N9  | 2N8  |     |     |
| 5               | VCO2_N2       | 04 <sub>hex</sub> | 2N7         | 2N6   | 2N5   | 2N4  | 2N3  | 2N2  | 2N1  | 2N0  |     |     |
| 6               | VCO2_R        | 05 <sub>hex</sub> | X           | 2R6   | 2R5   | 2R4  | 2R3  | 2R2  | 2R1  | 2R0  |     |     |
| 7               | VCO_SET       | 06 <sub>hex</sub> | 1VCO2       | 1VCO1 | 1VCO0 | X    | 1CP1 | 1CP0 | 2CP1 | 2CP0 |     |     |
| 8               | TEST          | 07 <sub>hex</sub> | X           | 1T4   | 1T3   | 1T2  | 1T1  | 1T0  | ST1  | ST0  |     |     |
| 9               | HI-IF         | 08 <sub>hex</sub> | X           | X     | F1    | F0   | MUX3 | MUX2 | MUX1 | MUX0 |     |     |

X = Don't care.

**Table 3. Register Description**

| REGISTER NUMBER | REGISTER NAME | REGISTER ADDRESS  | FUNCTION                                                          |
|-----------------|---------------|-------------------|-------------------------------------------------------------------|
| 1               | VCO1_N1       | 00 <sub>hex</sub> | VCO1 N-divider high                                               |
| 2               | VCO1_N2       | 01 <sub>hex</sub> | VCO1 N-divider low                                                |
| 3               | VCO1_R        | 02 <sub>hex</sub> | VCO1 R-divider                                                    |
| 4               | VCO2_N1       | 03 <sub>hex</sub> | VCO2 N-divider high                                               |
| 5               | VCO2_N2       | 04 <sub>hex</sub> | VCO2 N-divider low                                                |
| 6               | VCO2_R        | 05 <sub>hex</sub> | VCO2 R-divider                                                    |
| 7               | VCO_SET       | 06 <sub>hex</sub> | VCO select and charge-pump settings                               |
| 8               | TEST          | 07 <sub>hex</sub> | Test mode. For test purposes only. Program to 20 <sub>hex</sub> . |
| 9               | HI-IF         | 08 <sub>hex</sub> | Mode select, MUX output select                                    |

**Table 4. 1st VCO N-Divider Higher Register (VCO1\_N1)**

| BIT ID | BIT NAME          | BIT LOCATION (0 = LSB) | FUNCTION                   |
|--------|-------------------|------------------------|----------------------------|
| X      | X                 | 7, 6, 5                | Reserved                   |
| 1N     | 1st VCO N-Divider | 4–0                    | 1st VCO N-divider MSB bits |

**Table 5. 1st VCO N-Divider Lower Register (VCO1\_N2)**

| BIT ID | BIT NAME          | BIT LOCATION (0 = LSB) | FUNCTION                   |
|--------|-------------------|------------------------|----------------------------|
| 1N     | 1st VCO N-Divider | 7–0                    | 1st VCO N-divider LSB bits |

# HI-IF Single-Chip Broadband Tuners

**Table 6. 1st VCO R-Divider Higher Register (VCO1\_R)**

| BIT ID | BIT NAME          | BIT LOCATION (0 = LSB) | FUNCTION          |
|--------|-------------------|------------------------|-------------------|
| X      | X                 | 7, 6, 5                | Reserved          |
| 1R     | 1st VCO R-Divider | 4–0                    | 1st VCO R-divider |

**Table 7. 2nd VCO N-Divider Higher Register (VCO2\_N1)**

| BIT ID | BIT NAME          | BIT LOCATION (0 = LSB) | FUNCTION                   |
|--------|-------------------|------------------------|----------------------------|
| 2N     | 2nd VCO N-Divider | 7–0                    | 2nd VCO N-divider MSB bits |

**Table 8. 2nd VCO N-Divider Lower Register (VCO2\_N2)**

| BIT ID | BIT NAME          | BIT LOCATION (0 = LSB) | FUNCTION                   |
|--------|-------------------|------------------------|----------------------------|
| 2N     | 2nd VCO N-Divider | 7–0                    | 2nd VCO N-divider LSB bits |

**Table 9. 2nd VCO R-Divider Higher Register (VCO2\_R)**

| BIT ID | BIT NAME          | BIT LOCATION (0 = LSB) | FUNCTION          |
|--------|-------------------|------------------------|-------------------|
| X      | X                 | 7                      | Reserved          |
| 2R     | 2nd VCO R-Divider | 6–0                    | 2nd VCO R-divider |

**Table 10. VCO Tank and Charge-Pump Select Register (VCO\_SET)**

| BIT ID | BIT NAME                    | BIT LOCATION (0 = LSB) | FUNCTION                                                                                                                                                                                                                                                                                                                                                                              |
|--------|-----------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1VCO   | 1st VCO Tank Select         | 7, 6, 5                | 1st VCO Tank Select:<br><ul style="list-style-type: none"> <li>• 000 = 1st VCO tank (the lowest frequency oscillator)</li> <li>• 001 = 2nd VCO tank</li> <li>• 010 = 3rd VCO tank</li> <li>• 011 = 4th VCO tank</li> <li>• 100 = 5th VCO tank</li> <li>• 101 = 6th VCO tank</li> <li>• 110 = 7th VCO tank</li> <li>• 111 = 8th VCO tank (the highest frequency oscillator)</li> </ul> |
| X      | X                           | 4                      | Reserved                                                                                                                                                                                                                                                                                                                                                                              |
| 1CP    | 1st VCO Charge-Pump Current | 3, 2                   | 1st VCO Charge-Pump Current:<br><ul style="list-style-type: none"> <li>• 00 = 0.2mA</li> <li>• 01 = 0.4mA</li> <li>• 10 = 0.6mA</li> <li>• 11 = 0.8mA</li> </ul>                                                                                                                                                                                                                      |
| 2CP    | 2nd VCO Charge-Pump Current | 1, 0                   | 2nd VCO Charge-Pump Current:<br><ul style="list-style-type: none"> <li>• 00 = 0.2mA</li> <li>• 01 = 0.4mA</li> <li>• 10 = 0.6mA</li> <li>• 11 = 0.8mA</li> </ul>                                                                                                                                                                                                                      |

# HI-IF Single-Chip Broadband Tuners

MAX3570/MAX3571/MAX3573

**Table 11. HI-IF Step Control and MUX Output Register (HI-IF)**

| BIT ID | BIT NAME                           | BIT LOCATION (0 = LSB) | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|------------------------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| X      | X                                  | 7, 6                   | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| F      | HI-IF Filter Control               | 5, 4                   | HI-IF Filter Control:<br>• 00 = Step down 5MHz<br>• 01 = Nominal<br>• 11 = Step up 5MHz                                                                                                                                                                                                                                                                                                                                                                                                             |
| MUX    | Lock-Detect and MUX Output Control | 3–0                    | Lock-Detect and MUX Output Control:<br>• 0000 = Normal, low-noise operation<br>• 0001 = Lock detect for the 1st VCO<br>• 0010 = Lock detect for the 2nd VCO<br>• 0011 = 1st VCO N-divider<br>• 0100 = 1st VCO R-divider<br>• 0101 = 2nd VCO N-divider<br>• 0110 = 2nd VCO R-divider<br>• 0111 = Reference oscillator<br>• 1000 = AND output of lock detector<br>• 1001 = NAND output of lock detector<br>• 1010 = 1st VCO VTUNE over/under indicator<br>• 1011 = 2nd VCO VTUNE over/under indicator |

**Table 12. Read Mode Register Configuration**

| REGISTER NUMBER | REGISTER NAME | MSB         |       |     |     |     |    |     |    | LSB |
|-----------------|---------------|-------------|-------|-----|-----|-----|----|-----|----|-----|
|                 |               | 8 DATA BITS |       |     |     |     |    |     |    |     |
|                 |               | D7          | D6    | D5  | D4  | D3  | D2 | DB1 | D0 |     |
| 1               | LD_POR        | LOCK1       | LOCK2 | POR | OU1 | OU2 | X  | X   | X  |     |

**Table 13. Read Mode Register Description**

| REGISTER NUMBER | REGISTER NAME | FUNCTION                       |
|-----------------|---------------|--------------------------------|
| 1               | LD_POR        | Lock detect and power-on reset |

**Table 14. Lock Detect and POR Register**

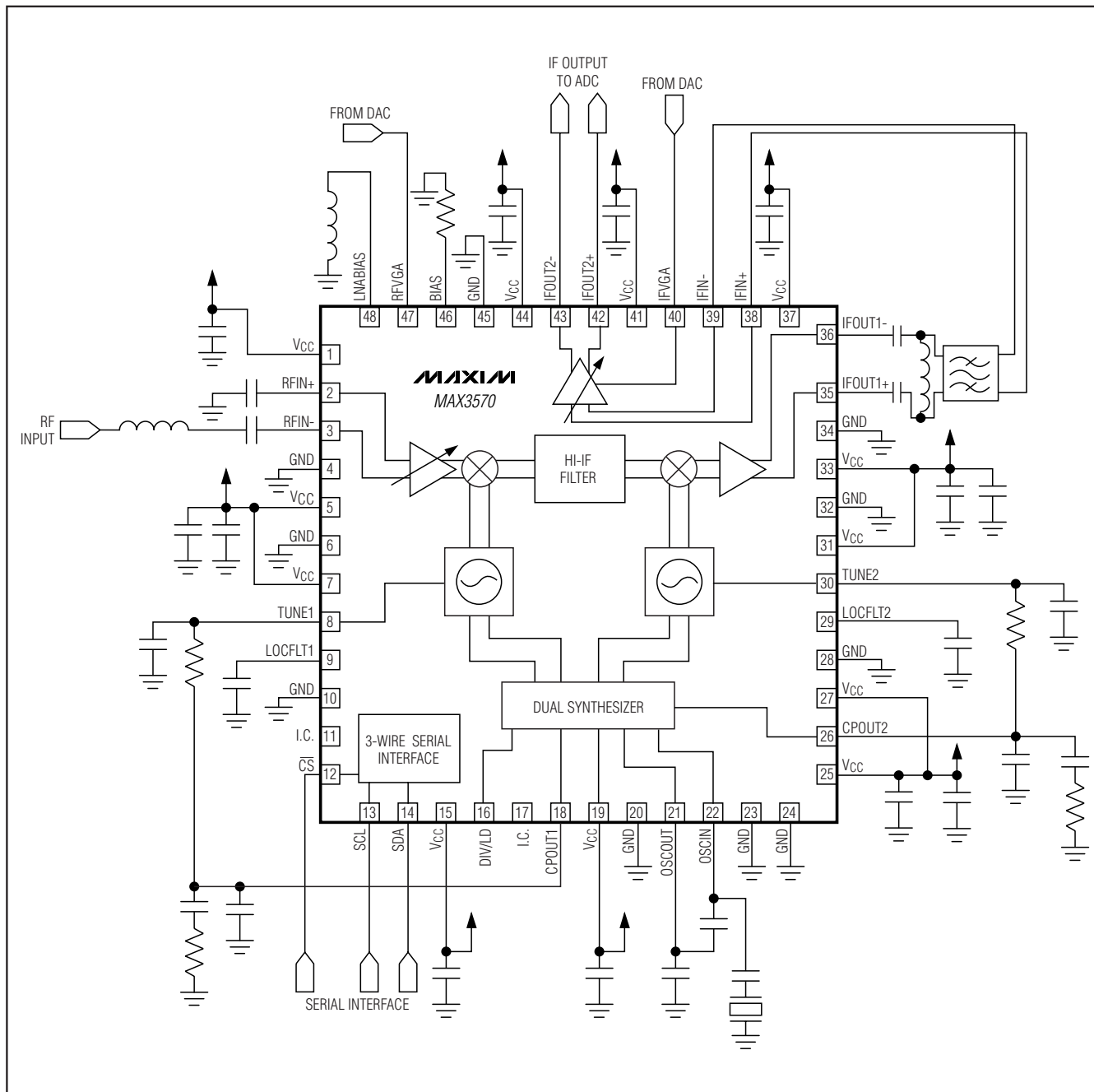
| BIT ID | BIT NAME | BIT LOCATION (0 = LSB) | FUNCTION                                                        |
|--------|----------|------------------------|-----------------------------------------------------------------|
| LOCK1  | LOCK1    | 7                      | Lock indicator for 1st VCO (see Table 15)                       |
| LOCK2  | LOCK2    | 6                      | Lock indicator for 2nd VCO                                      |
| POR    | POR      | 5                      | Power-on reset indicator; 1 indicates successful power-on reset |
| OU1    | OU1      | 4                      | Over or Under VTUNE indicator for 1st VCO (see Table 15)        |
| OU2    | OU2      | 3                      | Over or Under VTUNE indicator for 2nd VCO                       |
| X      | X        | 2, 1, 0                | Reserved                                                        |

**Table 15. 1st VCO Truth Table**

| LOCK1 | OU1 | DESCRIPTION                    |
|-------|-----|--------------------------------|
| 1     | x   | 1st VCO locked                 |
| 0     | 0   | (Under) Choose next lower tank |
| 0     | 1   | (Over) Choose next higher tank |

# HI-IF Single-Chip Broadband Tuners

## Typical Application Circuit



# HI-IF Single-Chip Broadband Tuners

MAX3570/MAX3571/MAX3573

## Applications Information

### RF Input

An LNA provides a single-ended broadband input matched to a  $75\Omega$  source. It provides a linear, continuous gain-control range of over 30dB before the signal is upconverted. A 16nH inductor in series with a 1000pF capacitor is required at the RF input (pin 3) to achieve optimal matching (see the *Typical Application Circuit*).

### HI-IF Frequency Agility

In a double conversion receiver, beat frequencies are generated from harmonics of the LOs associated with this system. In some instances these beat frequencies may coincide with the IF. If this occurs, it is possible to shift the HI-IF slightly by retuning the LOs. This shift moves the beat out of the IF band. The MAX3570/MAX3571/MAX3573 support this capability by allowing the user to shift the center frequency of the HI-IF filter slightly, tracking the shift in the LO frequencies, preserving the optimum image rejection and insertion loss. The HI-IF filter frequency shift is controlled with the HI-IF filter step control bits (F0 and F1, register address 8). (Patent pending.)

### IF Outputs

A first differential IF output (IFOUT1+, IFOUT1-), although intended to drive a standard IF SAW filter, is capable of driving loads as low as  $200\Omega$ . A second differential IF output (IFOUT2+, IFOUT2-) provides a balanced output capable of driving loads as low as  $300\Omega$  and can be AC-coupled to a standard QAM demodulator's ADC.

### Gain Control

The MAX3570/MAX3571/MAX3573 have two VGA circuits that are used to achieve the optimum SNR while minimizing distortion. At low input signal levels the RFVGA voltage should be 3.0V. This sets the LNA gain at its maximum. The IFVGA control voltage is used to set the required output signal level. As the RF input level increases, the IFVGA voltage drops. When the IFVGA voltage reaches a user-defined value (RFVGA attack point), the IFVGA voltage is frozen and the RFVGA voltage is adjusted to maintain the desired output level.

### VCO1 Selection

VCO1 generates the first local oscillator (LO1) frequency for the upconverting mixer. It consists of an array of eight VCOs; each tuned to a unique frequency band, to cover the required frequency range. The desired VCO is chosen through the serial data interface (SDI). Please refer to Application Note: MAX3550/MAX3551/MAX3553 *VCO Selection* for further information on VCO1 VCO selection.

## Synthesizer Comparison Frequency Selection

The two on-chip synthesizers of the MAX3570/MAX3571/MAX3573 are capable of supporting a wide range of comparison frequencies. The PLL for the first LO (LO1) provides a comparison frequency range from below 250kHz up to 4MHz, assuming a 4MHz reference (crystal) frequency. The second LO (LO2) PLL supports a comparison frequency range from below 50kHz up to 2MHz, again assuming a 4MHz reference.

Comparison frequencies of 1MHz for LO1 ( $R1 = 4$ ) and 250kHz for LO2 ( $R2 = 16$ ) are recommended for the MAX3570 and MAX3571. For the MAX3573, the recommended LO2 comparison frequency is 142.8571kHz ( $R2 = 28$ , 4MHz crystal frequency). These values ensure optimum resolution while working with the loop filters to suppress spurious energy and provide acceptable lock time.

### Synthesizer Loop Filters

A third-order lowpass loop filter is used for each local oscillator to achieve low spurious and low phase noise. The loop bandwidth is chosen so the spurious rejection is sufficient and a reasonable lock time is achieved. Refer to the EV kit for the recommended loop-filter component values.

### Crystal Oscillator Interface

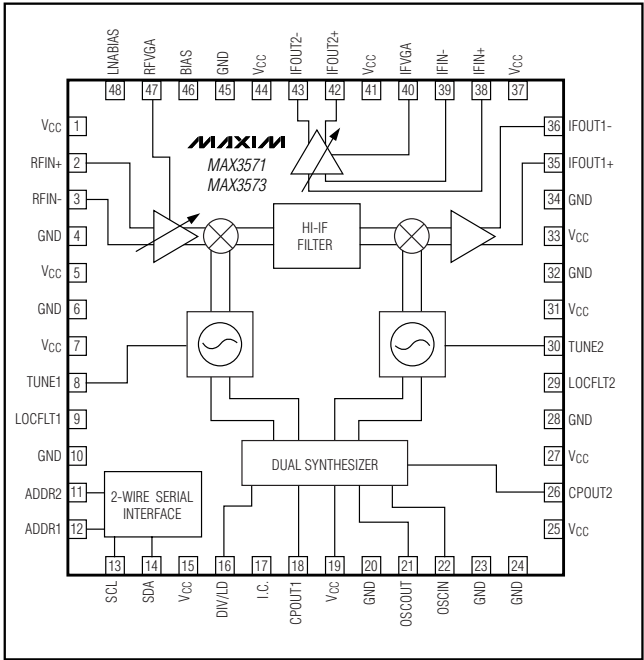
The crystal oscillator pins (OSCIN, OSCOUT) must be connected to a crystal or an external reference oscillator. When connecting directly to a crystal, refer to the EV kit for the recommended component values. When using an external reference oscillator, drive OSCIN with an amplitude of 1.5V<sub>P-P</sub>, and leave OSCOUT unconnected.

### Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at a central VCC node. The VCC traces branch out from this node, each going to a separate VCC node in the MAX3570/MAX3571/MAX3573 circuit. At the end of each trace is a bypass capacitor with a low impedance to ground at the frequency of interest. This arrangement provides local decoupling at each VCC pin. Use at least one via per bypass capacitor for a low-inductance ground connection.

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The layout of a matching network can be very sensitive to parasitic circuit elements. To minimize parasitic inductance, keep all traces short and place components as close to the IC as possible. To minimize parasitic capacitance, a cutout in the ground plane (and any other planes) below the matching network components can be used. Refer to the EV kit for the recommended input matching network.

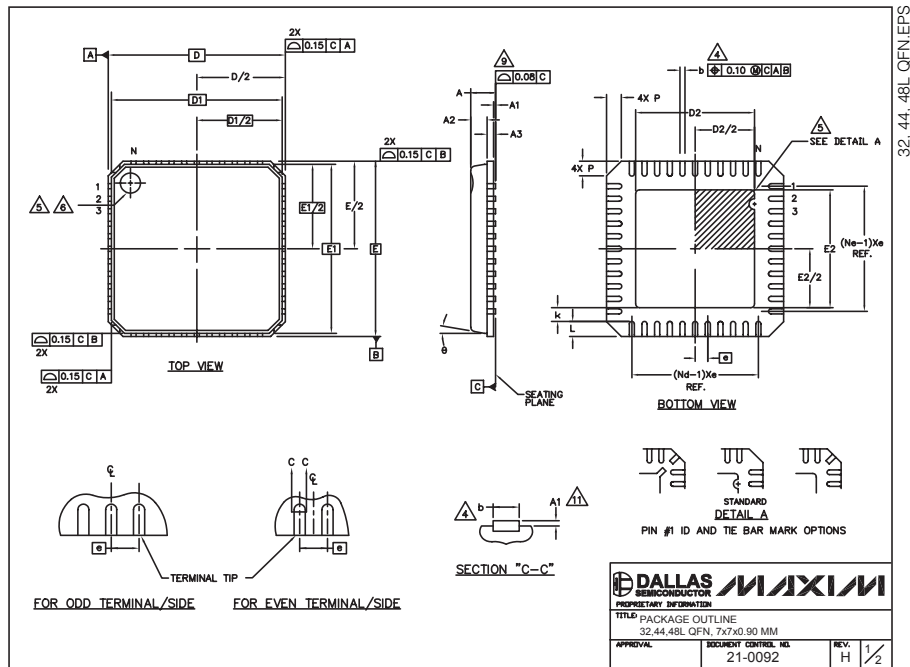
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TRANSISTOR COUNT: 18,970  
PROCESS: SiGe BiCMOS

# HI-IF Single-Chip Broadband Tuners

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).) Refer to G4877-1.



| COMMON DIMENSIONS |          |      |      |          |      |      |          |      |      |
|-------------------|----------|------|------|----------|------|------|----------|------|------|
| PKG               | 32L 7x7  |      |      | 44L 7x7  |      |      | 48L 7x7  |      |      |
| SYMBOL            | MIN.     | NDM. | MAX. | MIN.     | NDM. | MAX. | MIN.     | NDM. | MAX. |
| A                 | 0.80     | 0.90 | 1.00 | 0.80     | 0.90 | 1.00 | 0.80     | 0.90 | 1.00 |
| A1                | 0.00     | 0.01 | 0.05 | 0.00     | 0.01 | 0.05 | 0.00     | 0.01 | 0.05 |
| A2                | 0.00     | 0.65 | 1.00 | 0.00     | 0.65 | 1.00 | 0.00     | 0.65 | 1.00 |
| A3                | 0.20 REF |      |      | 0.20 REF |      |      | 0.20 REF |      |      |
| b                 | 0.23     | 0.28 | 0.35 | 0.18     | 0.23 | 0.30 | 0.18     | 0.23 | 0.30 |
| D                 | 6.90     | 7.00 | 7.10 | 6.90     | 7.00 | 7.10 | 6.90     | 7.00 | 7.10 |
| D1                | 6.75 BSC |      |      | 6.75 BSC |      |      | 6.75 BSC |      |      |
| E                 | 6.90     | 7.00 | 7.10 | 6.90     | 7.00 | 7.10 | 6.90     | 7.00 | 7.10 |
| E1                | 6.75 BSC |      |      | 6.75 BSC |      |      | 6.75 BSC |      |      |
| e                 | 0.65 BSC |      |      | 0.50 BSC |      |      | 0.50 BSC |      |      |
| k                 | 0.25     | -    | -    | 0.25     | -    | -    | 0.25     | -    | -    |
| L                 | 0.35     | 0.55 | 0.75 | 0.35     | 0.55 | 0.75 | 0.30     | 0.40 | 0.50 |
| N                 | 32       |      |      | 44       |      |      | 48       |      |      |
| Nd                | 8        |      |      | 11       |      |      | 12       |      |      |
| Ne                | 8        |      |      | 11       |      |      | 12       |      |      |
| P                 | 0.00     | 0.42 | 0.60 | 0.00     | 0.42 | 0.60 | 0.00     | 0.42 | 0.60 |
| U                 | 0"       |      |      | 12"      |      |      | 0"       |      |      |

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
4. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
5. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING IDENTIFICATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. PACKAGE WARPAGE MAX 0.08mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
11. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
12. MEETS JEDEC MO220 EXCEPT DIMENSION "b" MINIMUM.
13. APPLY ONLY FOR TERMINAL.
14. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION(STEPPED SIDES).

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