119-Bump BGA
Commercial Temp
Industrial Temp

1M x 18, 512K x 36
18Mb Register-Register Late Write SRAM

250 MHz–357 MHz
1.8 V V_{DD}
1.5 V or 1.8 V HSTL I/O

Features

- Register-Register Late Write mode, Pipelined Read mode
- 1.8 V +150/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- ZQ controlled programmable output drivers
- Dual Cycle Deselect
- Fully coherent read and write pipelines
- Byte write operation (9-bit bytes)
- Differential HSTL clock inputs, $\overline{K}$ and K
- Asynchronous output enable
- Sleep mode via ZZ
- IEEE 1149.1 JTAG-compliant Serial Boundary Scan
- JEDEC-standard 119-bump BGA package
- Pb-Free 119-bump BGA package available

Family Overview

GS8150V18/36A are 18,874,368-bit (18Mb) high performance SRAMs. This family of wide, very low voltage HSTL I/O SRAMs is designed to operate at the speeds needed to implement economical high performance cache systems.

Functional Description

Because GS8150V18/36A are synchronous devices, address data inputs and read/write control inputs are captured on the rising edge of the input clock. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

GS8150V18/36A support pipelined reads utilizing a rising-edge-triggered output register. They also utilize a Dual Cycle Deselect (DCD) output deselect protocol.

GS8150V18/36A are implemented with high performance HSTL technology and are packaged in a 119-bump BGA.

Mode Control

There are two mode control select pins (M1 and M2), which allow the user to set the correct read protocol for the design. The GS8150V18/36A support single clock Pipeline mode, which directly affects the two mode control select pins. In order for the part to fuction correctly, and as specified, M1 must be tied to VSS and M2 must be tied to V_{DD} or V_{DDQ}. This must be set at power-up and should not be changed during operation.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Parameter Synopsis

		-357	-333	-300	-250	Unit
Pipeline	Cycle	2.8	3.0	3.3	4.0	ns
	tKHQV	1.4	1.5	1.6	2.0	ns
	Curr (x18)	600	550	500	450	mA
	Curr (x36)	650	600	550	500	mA

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GS8150V36 Pinout—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	A	A	NC	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	DQ_C	V_{SS}	ZQ	V_{SS}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{SS}$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{G}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{B}_C$	NC	$\overline{B}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	NC	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{B}_D$	$\overline{CK}$	$\overline{B}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{SW}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQ_D	V_{SS}	A	V_{SS}	DQ_A	DQ_A
R	NC	A	M1	V_{DD}	M2	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

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GS8150V18 Pinout—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	A	A	NC	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_B	NC	V_{SS}	ZQ	V_{SS}	DQ_A	NC
E	NC	DQ_B	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{B}_B$	NC	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	NC	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	$\overline{CK}$	$\overline{B}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A	V_{SS}	DQ_A	NC
P	NC	DQ_B	V_{SS}	A	V_{SS}	NC	DQ_A
R	NC	A	M1	V_{DD}	M2	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

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GS8150V18/36 BGA Pin Description

Symbol	Type	Description
A	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low
NC	—	No Connect
CK	I	Clock Input Signal; active high
$\overline{CK}$	I	Clock Input Signal; active low
$\overline{SW}$	I	Write Enable; active low
$\overline{G}$	I	Output Enable; active low
ZZ	I	Sleep mode control; active high
M1	I	Read Operation Protocol Select—Selects Register-Register read operations; must be tied low in this device
M2	I	Read Operation Protocol Select—Selects Register-Register read operations; must be tied high in this device
ZQ	I	FLXDrive-II™ Output Impedance Control
$\overline{SS}$	I	Synchronous Select Input
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
V_{REF}	I	Input Reference Voltage
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply

Read Operations

Pipelined Read

A read cycle begins when the RAM captures logic 0 on $\overline{SS}$ and logic 1 on $\overline{SW}$ at the rising edge of K (and the falling edge of $\overline{K}$). Address inputs captured on that clock edge are propigated into the RAM, which delivers data to the input of the output registers. The second rising edge of K fires the output registers and releases read data to the output drivers. If $\overline{G}$ is held active low, the drivers drive the data onto the output pins. Read data is sustained on the output pins as long as $\overline{G}$ is held low or until the next rising edge of K, at which point the outputs may update to new data or deselect, depending on what control command was registered at the second rising edge of K.

Dual Cycle Deselect

Chip deselect ($\overline{SS}$ = logic 1) is pipelined to the same degree as read data. Therefore, a deselect command entered on the rising edge of K is acted upon in response to the next rising edge of K.

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Write Operations

Write operations are initiated when the write enable input signal ($\overline{SW}$) and chip select ($\overline{SS}$) are captured at logic 0 on a rising edge of the K clock (and falling edge of the $\overline{K}$ clock).

Late Write

In Late Write mode the RAM requires Data In one rising clock edge later than the edge used to load Address and Control. Late Write protocol has been employed on SRAMs designed for RISC processor L2 cache applications and in Flow Through mode NBT SRAMs.

Byte Write Control

The Byte Write Enable inputs ($\overline{Bx}$) determine which bytes will be written. Any combination of Byte Write Enable control pins, including all or none, may be activated. A Write Cycle with no Byte Write inputs active is a write abort cycle. Byte write control inputs are captured by the same clock edge used to capture $\overline{SW}$.

Example of x36 Byte Write Truth Table

Function	$\overline{SW}$	$\overline{Ba}$	$\overline{Bb}$	$\overline{Bc}$	$\overline{Bd}$
Read	H	X	X	X	X
Write Byte A	L	L	H	H	H
Write Byte B	L	H	L	H	H
Write Byte C	L	H	H	L	H
Write Byte D	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort	L	H	H	H	H

FLXDrive-II™ HSTL Output Driver Impedance Control

HSTL I/O SigmaRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired SRAM driver impedance. The allowable range of RQ to guarantee impedance matching with specified tolerance is between 150Ω and 300Ω. Periodic readjustment of the output driver impedance occurs automatically because driver impedance is affected by drifts in supply voltage and die temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. The SRAM requires 32K start-up clock cycles, selected or deselected, after V_{DD} reaches its operating range to reach its programmed output driver impedance.

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Register-Register Late Write, Pipelined Read Truth Table

CK	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{Bx}$	$\overline{G}$	Current Operation	DQ (t_n)	DQ (t_{n+1})
X	1	X	X	X	X	Sleep (Power Down) mode	Hi-Z	Hi-Z
↑	0	1	X	X	X	Deselect	***	Hi-Z
↑	0	0	1	X	1	Read	Hi-Z/	Hi-Z
↑	0	0	1	X	0	Read	***	$Q(t_n)$
↑	0	0	0	0	X	Write All Bytes	***	$D(t_n)$
↑	0	0	0	X	X	Write Bytes with $\overline{Bx}$ = 0	***	$D(t_n)$
↑	0	0	0	1	X	Write (Abort)	***	Hi-Z

Notes:

1. If one or more $\overline{Bx}$ = 0, then B = "T" else B = "F".
2. "1" = input "high"; "0" = input "low"; "X" = input "don't care".
3. "***" indicates that the DQ input requirement/output state and CQ output state are determined by the previous operation.
4. DQs are tristated in response to Bank Deselect, Deselect, and Write commands, one full cycle after the command is sampled.
5. CQs are tristated in response to Bank Deselect commands only, one full cycle after the command is sampled.
6. Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

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Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.5	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} + 0.5 (≤ 2.5 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} + 0.5 (≤ 2.5 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
1.5 V I/O Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	
1.8 V I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	1

Note:
The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

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HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	V_{REF} + 100	—	V_{DDQ} + 300	mV	
DC Input Logic Low	V_{IL} (dc)	–300	—	V_{REF} – 100	mV	
DC Clock Input Differential Voltage	V_{DIF} (dc)	100	—	V_{DDQ} + 300	mV	2
V_{REF} DC Voltage	V_{REF} (dc)	V_{DDQ}/2 – 0.1	—	V_{DDQ}/2 + 0.1	V	1
Clock Input Voltag	V_{CK} (dc)	–300	—	V_{DDQ} + 300	V	
Clock Input Commone Mode Voltage	V_{CM} (dc)	600	750	900	V	

Notes:

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{DIF}).
3. To guarantee AC characteristics, V_{IH},V_{IL},Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers.Compatible with both 1.8 V and 1.5 V I/O drivers.
5. See AC Input Definition drawing below.

HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 200	—	mV	3,4
AC Input Logic Low	V_{IL} (ac)	—	V_{REF} – 200	mV	3,4
AC Clock Input Differential Voltage	V_{DIF} (ac)	800	—	mV	2,3
V_{REF} Peak to Peak AC Voltage	V_{REF} (ac)	—	5% V_{REF} (DC)	mV	1

Notes:

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{DIF}). The RAM can be operated with a single ended clocking with either CK or $\overline{CK}$ tied to V_{REF}.
3. To guarantee AC characteristics, V_{IH},V_{IL},Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers.Compatible with both 1.8 V and 1.5 V I/O drivers.
5. See AC Input Definition drawing below.

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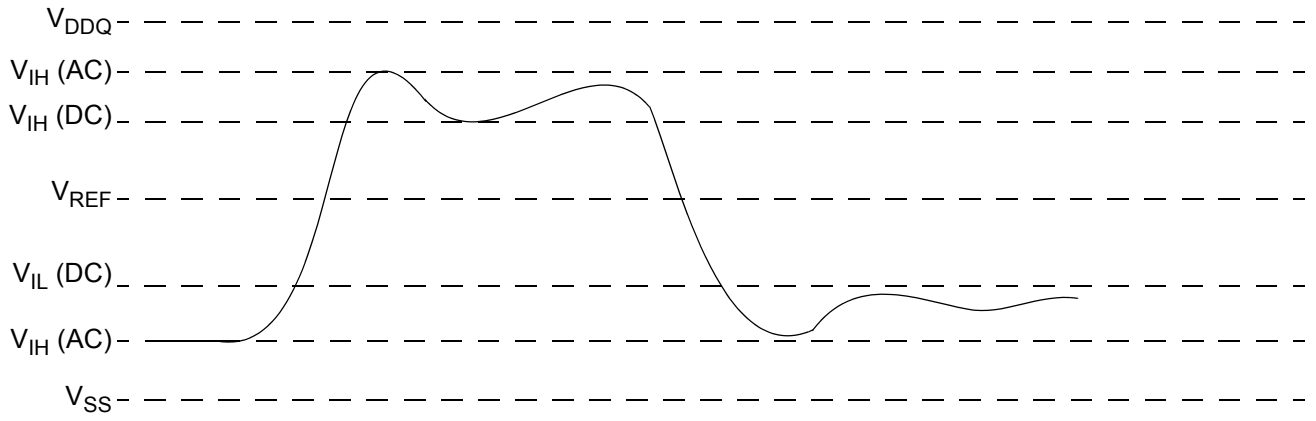
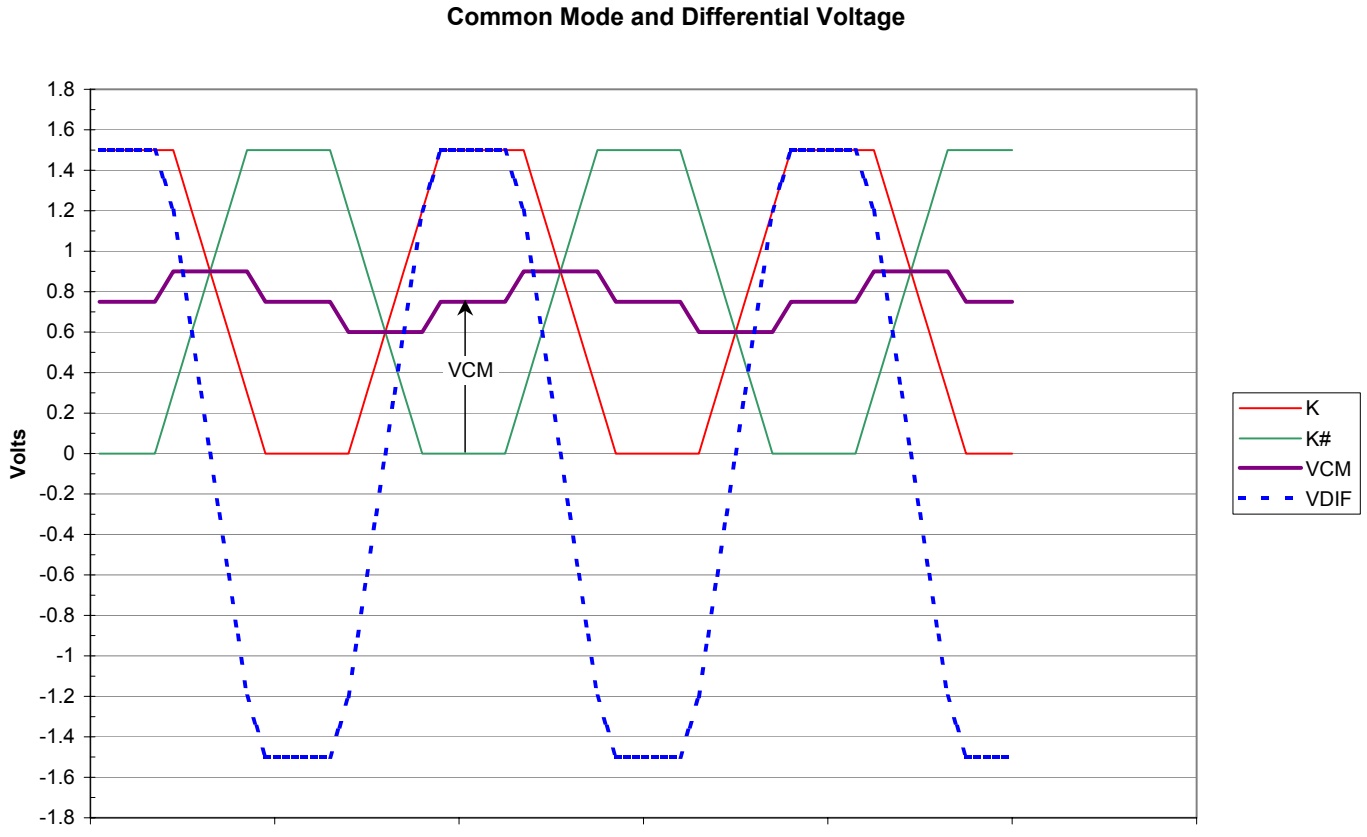
HSTL I/O AC Input Definitions



Differential Voltage and Common Mode Voltage



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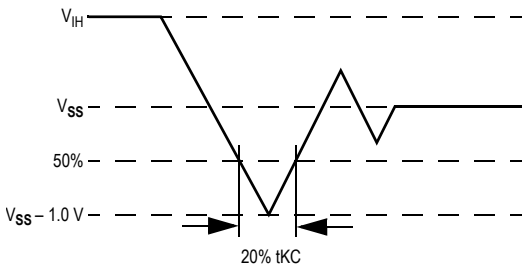
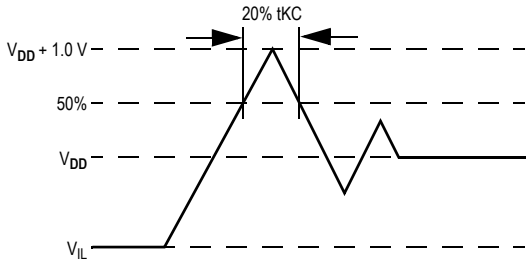
Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V)

Parameter	Symbol	Test conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	5	pF
Output Capacitance (Clock)	$C_{IN(CK)}$	V_{IN} = 0 V	5	pF

Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	1.25 V
Input low level	0.25 V
Input rise/fall time (10% to 90%)	0.5 ns/0.5 ns
Input reference level	$V_{DDQ}/2$
Clock input reference level	Differential cross point
Output reference level	$V_{DDQ}/2$
Clock (V_{DIF})	0.75 V
Clock (V_{CM})	0.75 V
V_{DDQ}	1.5 V
RQ	250Ω

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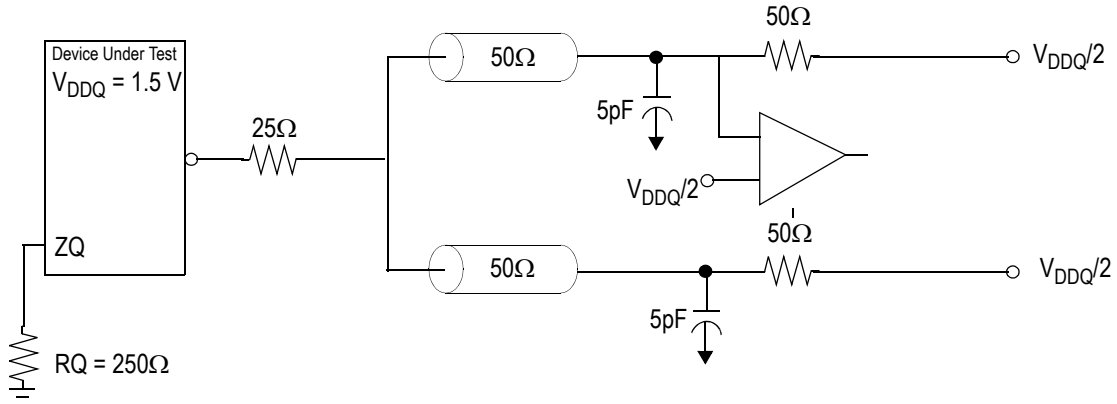
AC Test Load Diagram



Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DDQ}	–2 uA	2 uA	—
ZQ, MCH, MCL, EP2, EP3 Pin Input Current	I_{INM}	V_{IN} = 0 to V_{DDQ}	–50 uA	50 uA	—
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA	—

Operating Currents

Parameter		Symbol	-357		-333		-300		-250		Test Conditions
			0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	
Operating Current	x36	I_{DD}	650 mA	660 mA	600 mA	610 mA	550 mA	560 mA	500 mA	510 mA	SS ≤ V_{IL} Max. tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \geq V_{IN} \geq V_{IH}$
	x18	I_{DD}	600 mA	610 mA	550 mA	560 mA	500 mA	510 mA	450 mA	460 mA	
HSTL Deselect Current		I_{DD3}	150 mA	160 mA	150 mA	160 mA	150 mA	160 mA	150 mA	160 mA	Device Deselected All inputs V_{SS} + 0.10 V ≥ V_{IN} ≥ V_{DD} – 0.10 V

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AC Electrical Characteristics

Parameter	Symbol	-357		-333		-300		-250		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	2.8	—	3.0	—	3.3	—	4.0	—	ns	—
Clock High Time	tKHKL	1.1	—	1.2	—	1.3	—	1.5	—	ns	—
Clock Low Time	tKLKH	1.1	—	1.2	—	1.3	—	1.5	—	ns	—
Clock High to Output Low-Z	tKHQX1	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output Valid	tKHQV	—	1.4	—	1.5		1.6	—	2.0	ns	—
Clock High to Output Invalid	tKHQX	0.5	—	0.5	—	0.5	—	0.5	—	ns	—
Clock High to Output High-Z	tKHQZ	—	1.4	—	1.5		1.6	—	2.0	ns	1
Address Valid to Clock High	tAVKH	0.5	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Address Don't Care	tKHAX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Enable Valid to Clock High	tEVKH	0.5	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Enable Don't Care	tKHEX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Write Valid to Clock High	tWVKH	0.5	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Write Don't Care	tKHWX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Byte Write Valid to Clock High	tBVKH	0.5	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Byte Write Don't Care	tKHBX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Data In Valid to Clock High	tDVKH	0.5	—	0.5	—	0.5	—	0.5	—	ns	—
Clock High to Data In Don't Care	tKHDX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Output Enable Low to Output Data Valid	tGLQV	—	1.4	—	1.5		1.6	—	2.0	ns	—
Output Enable Low to Output Data Low-Z	tGLQX	0	—	0	—	0	—	0	—	ns	—
Output Enable High to Output Data High-Z	tGHQZ	—	1.4	—	1.5		1.6	—	2.0	ns	—
Sleep Mode Enable Time	tZZE	—	15	—	15	—	15	—	15	ns	—
Sleep Mode Recovery Time	tZZR	20	—	20	—	20	—	20	—	ns	—

Notes:

1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.

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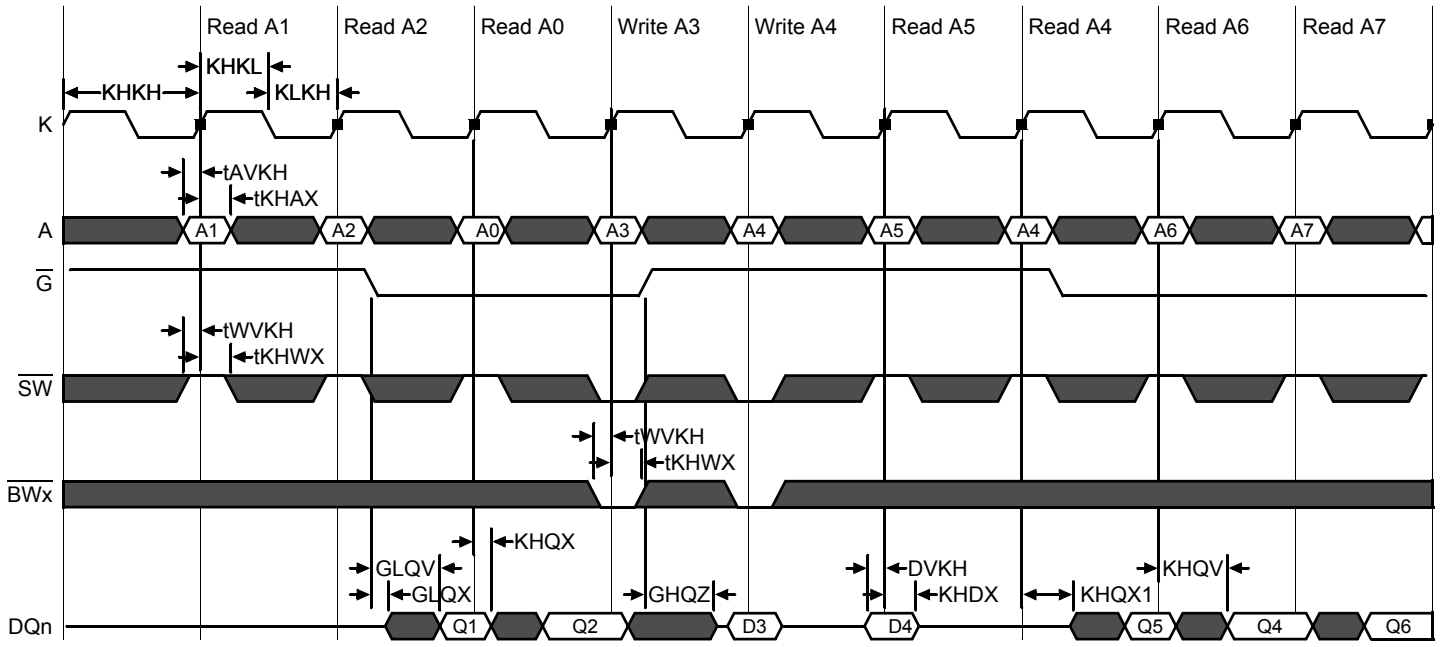
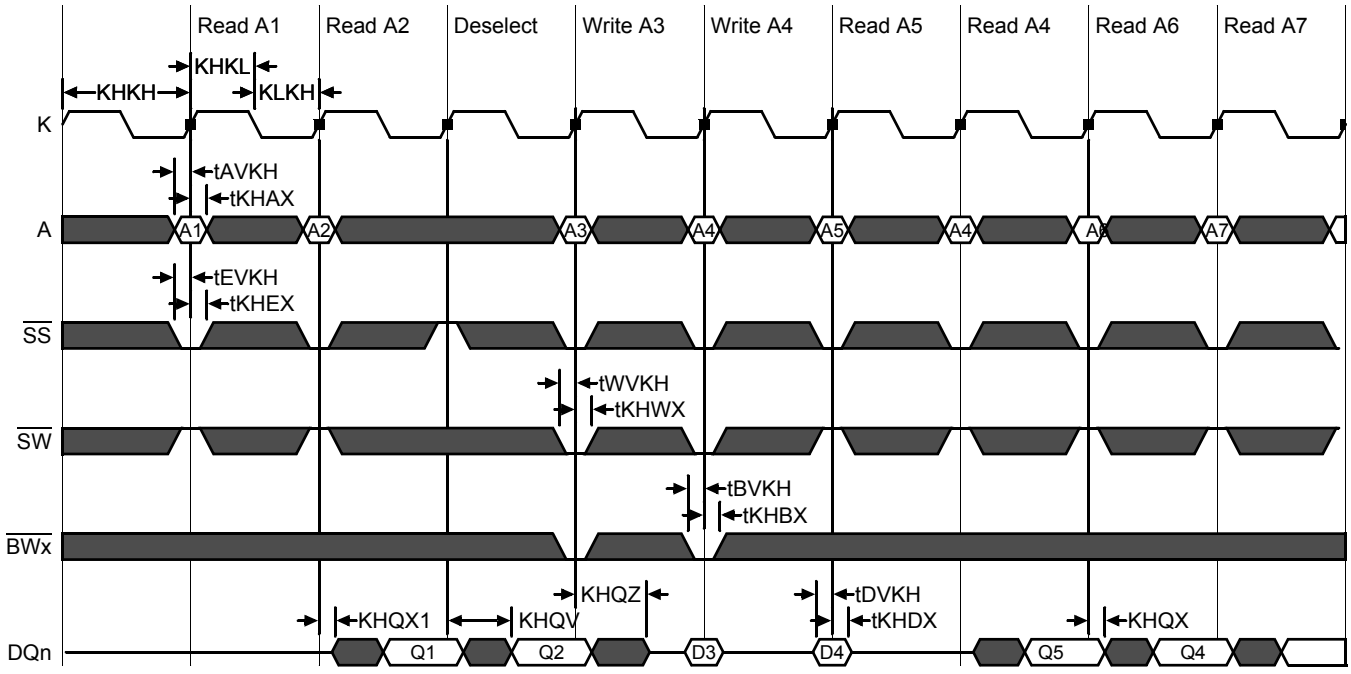
$\overline{G}$ Controlled Read-Write



Note:
$\overline{K}$ is not shown; assumes $\overline{K}$ tied to V_{REF} or out of phase with K

$\overline{SS}$ Controlled Read-Write



Note:
$\overline{K}$ is not shown; assumes $\overline{K}$ tied to V_{REF} or out of phase with K

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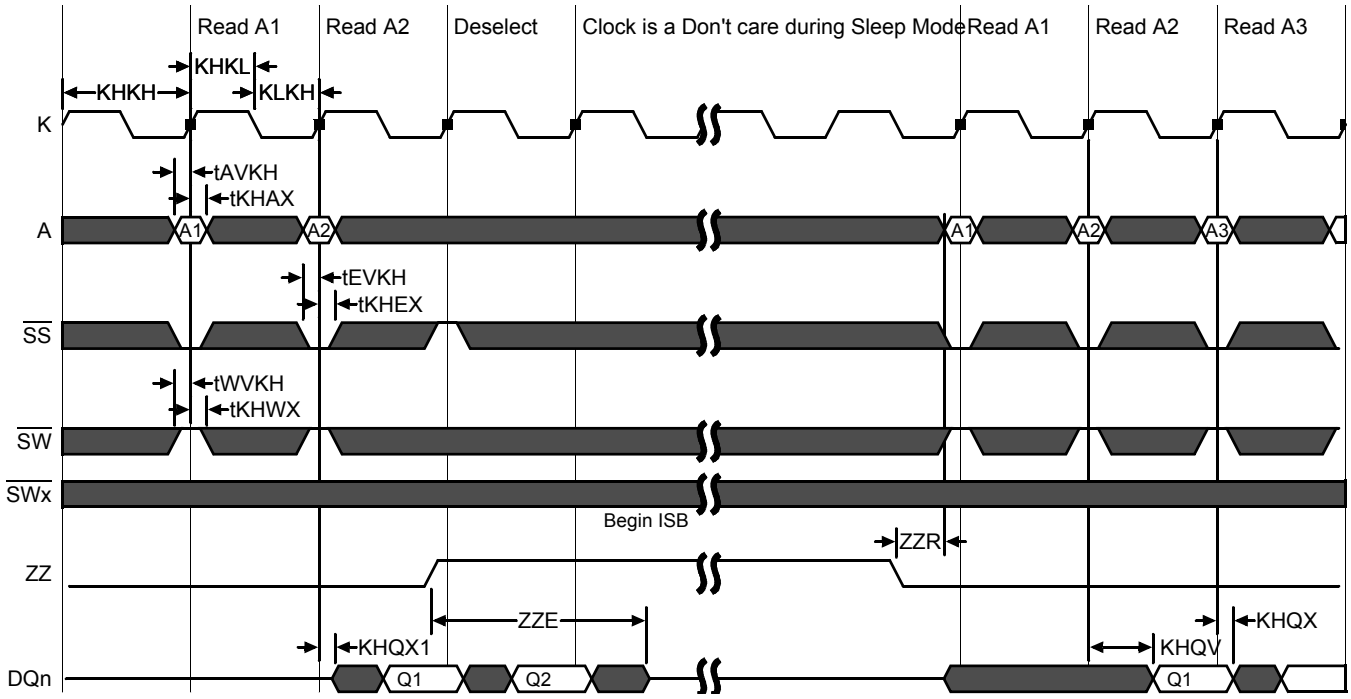
ZZ Timing



Note:
$\overline{K}$ is not shown; assumes $\overline{K}$ tied to V_{REF} or out of phase with K

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

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JTAG Port Registers

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

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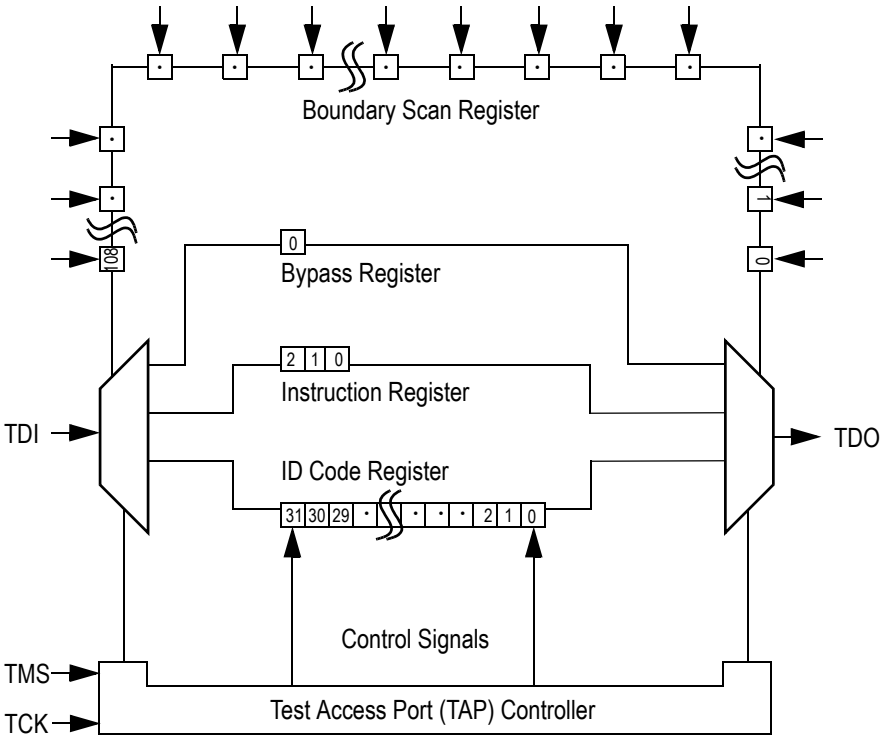
JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

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Tap Controller Instruction Set

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x36	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

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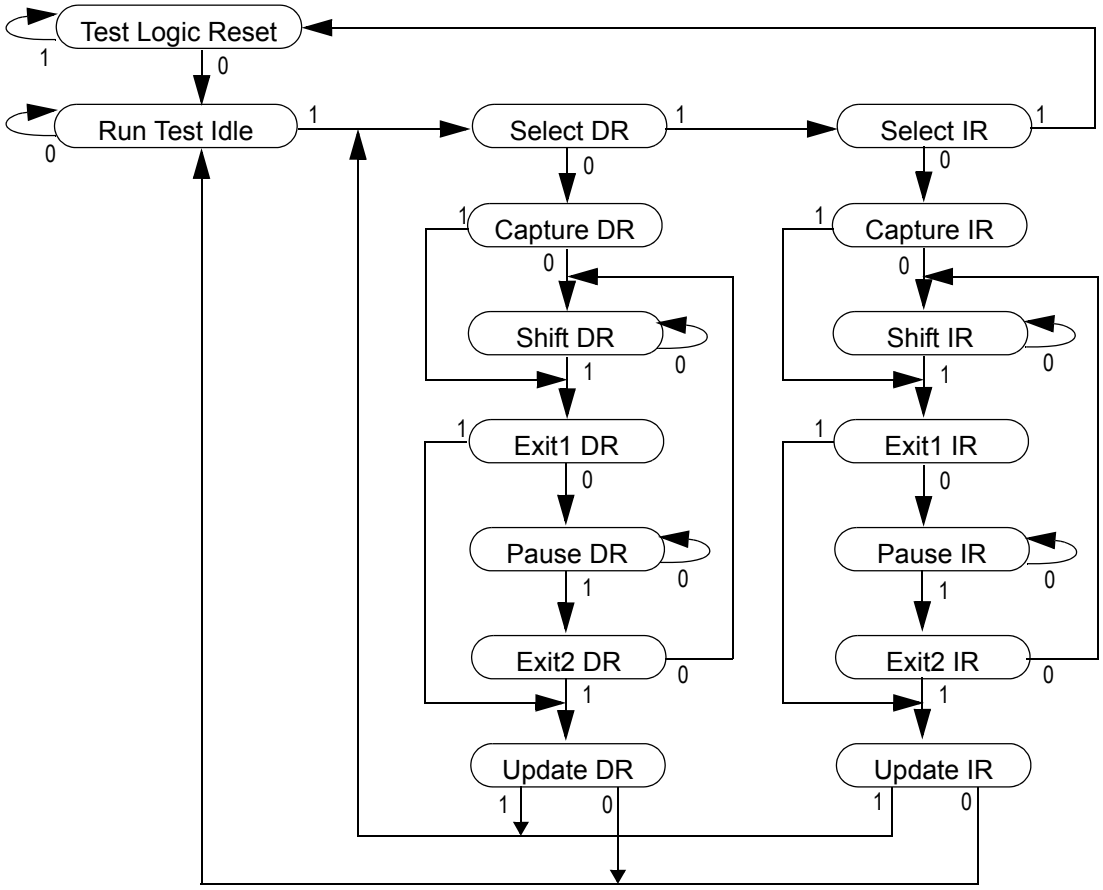
JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

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Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

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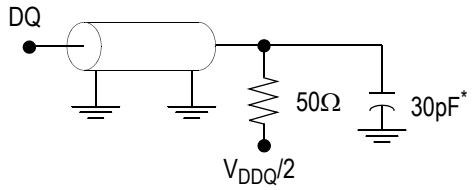
JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

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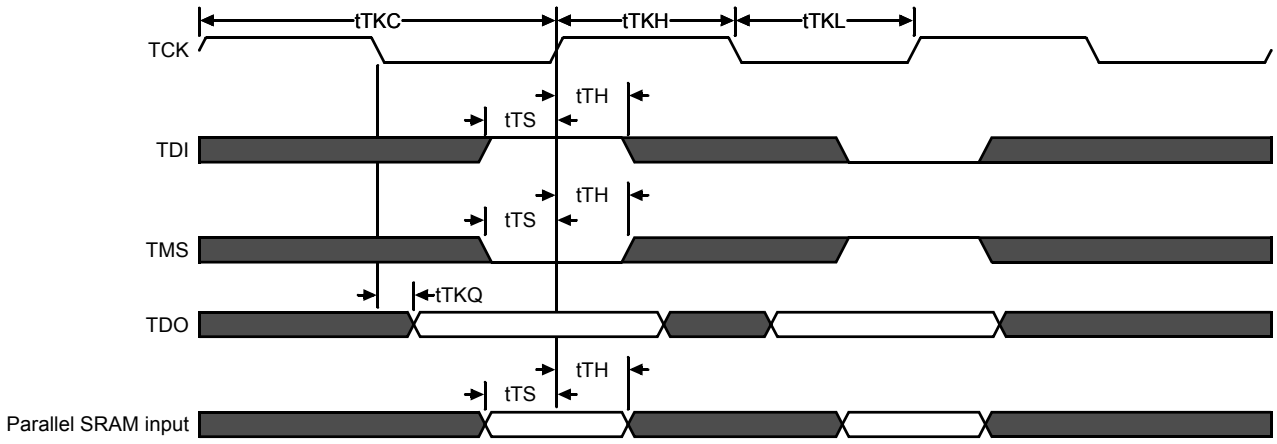
JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

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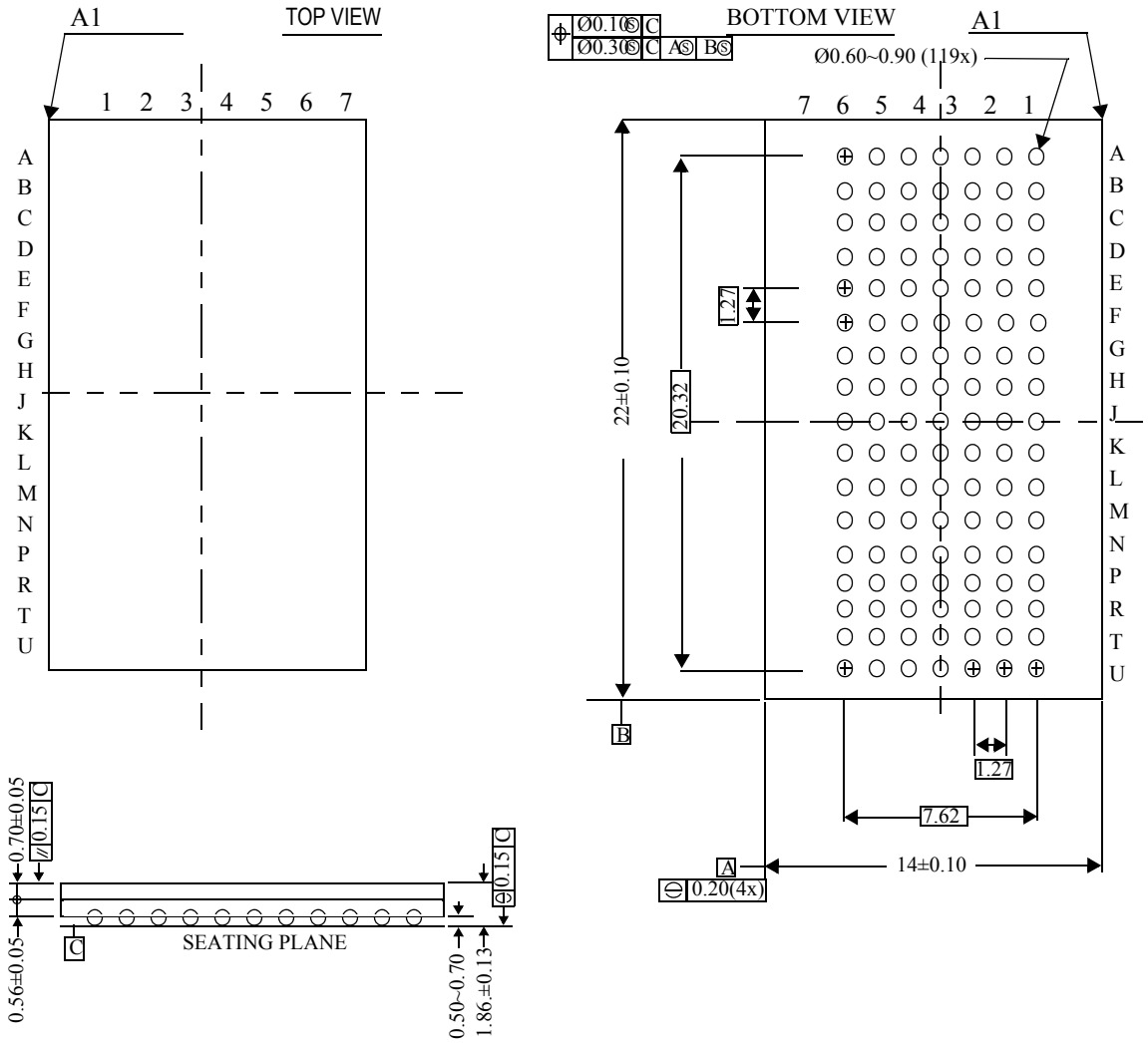
Package Dimensions—119-Bump FPBGA (Package B, Variation 2)



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Ordering Information

Org	Part Number	Type	I/O	Speed (MHz)	T_A
1M x 18	GS8150V18AB-357	Register-Register Late Write SRAM	HSTL	357 MHz	C
1M x 18	GS8150V18AB-333	Register-Register Late Write SRAM	HSTL	333 MHz	C
1M x 18	GS8150V18AB-300	Register-Register Late Write SRAM	HSTL	300 MHz	C
1M x 18	GS8150V18AB-250	Register-Register Late Write SRAM	HSTL	250 MHz	C
512K x 36	GS8150V36AB-357	Register-Register Late Write SRAM	HSTL	357MHz	C
512K x 36	GS8150V36AB-333	Register-Register Late Write SRAM	HSTL	333 MHz	C
512K x 36	GS8150V36AB-300	Register-Register Late Write SRAM	HSTL	300 MHz	C
512K x 36	GS8150V36AB-250	Register-Register Late Write SRAM	HSTL	250 MHz	C
1M x 18	GS8150V18AB-357I	Register-Register Late Write SRAM	HSTL	357 MHz	I
1M x 18	GS8150V18AB-333I	Register-Register Late Write SRAM	HSTL	333 MHz	I
1M x 18	GS8150V18AB-300I	Register-Register Late Write SRAM	HSTL	300 MHz	I
1M x 18	GS8150V18AB-250I	Register-Register Late Write SRAM	HSTL	250 MHz	I
512K x 36	GS8150V36AB-357I	Register-Register Late Write SRAM	HSTL	357 MHz	I
512K x 36	GS8150V36AB-333I	Register-Register Late Write SRAM	HSTL	333 MHz	I
512K x 36	GS8150V36AB-300I	Register-Register Late Write SRAM	HSTL	300 MHz	I
512K x 36	GS8150V36AB-250I	Register-Register Late Write SRAM	HSTL	250 MHz	I
1M x 18	GS8150V18AGB-357	Pb-Free Register-Register Late Write SRAM	HSTL	357 MHz	C
1M x 18	GS8150V18AGB-333	Pb-Free Register-Register Late Write SRAM	HSTL	333 MHz	C
1M x 18	GS8150V18AGB-300	Pb-Free Register-Register Late Write SRAM	HSTL	300 MHz	C
1M x 18	GS8150V18AGB-250	Pb-Free Register-Register Late Write SRAM	HSTL	250 MHz	C
512K x 36	GS8150V36AGB-357	Pb-Free Register-Register Late Write SRAM	HSTL	357MHz	C
512K x 36	GS8150V36AGB-333	Pb-Free Register-Register Late Write SRAM	HSTL	333 MHz	C
512K x 36	GS8150V36AGB-300	Pb-Free Register-Register Late Write SRAM	HSTL	300 MHz	C
512K x 36	GS8150V36AGB-250	Pb-Free Register-Register Late Write SRAM	HSTL	250 MHz	C
1M x 18	GS8150V18AGB-357I	Pb-Free Register-Register Late Write SRAM	HSTL	357 MHz	I
1M x 18	GS8150V18AGB-333I	Pb-Free Register-Register Late Write SRAM	HSTL	333 MHz	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8150V36AB-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

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Ordering Information

Org	Part Number	Type	I/O	Speed (MHz)	T_A
1M x 18	GS8150V18AGB-300I	Pb-Free Register-Register Late Write SRAM	HSTL	300 MHz	I
1M x 18	GS8150V18AGB-250I	Pb-Free Register-Register Late Write SRAM	HSTL	250 MHz	I
512K x 36	GS8150V36AGB-357I	Pb-Free Register-Register Late Write SRAM	HSTL	357 MHz	I
512K x 36	GS8150V36AGB-333I	Pb-Free Register-Register Late Write SRAM	HSTL	333 MHz	I
512K x 36	GS8150V36AGB-300I	Pb-Free Register-Register Late Write SRAM	HSTL	300 MHz	I
512K x 36	GS8150V36AGB-250I	Pb-Free Register-Register Late Write SRAM	HSTL	250 MHz	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8150V36AB-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

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18Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8150VxxA_r1		• Creation of new datasheet
8150VxxA_r1; 8150VxxA_r1_01	Content/Format	• Corrected L3 from VSS to NC • Updated entire format • Placed corrected BGA diagram in document
8150VxxA_r1_01; 8150VxxA_r1_02	Content/Format	• Updated format • Added variation information to 119 BGA mechanical drawing
8150VxxA_r1_02; 8150VxxA_r1_03	Content	• Updated AC Characteristics table • Updated /G Controlled Read-Write timing diagram
8150VxxA_r1_03; 8150VxxA_r1_04	Content	• Pb-Free information added

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