

Document Title**128K x8 bit 3.3V Low Power CMOS slow SRAM**Revision History

| <u>Revision No</u> | <u>History</u>                                                                | <u>Draft Date</u> | <u>Remark</u> |
|--------------------|-------------------------------------------------------------------------------|-------------------|---------------|
| 10                 | Initial Revision History Insert                                               | Jul.14.2000       | Final         |
| 11                 | Change the Notch Location of sTSOP<br>- Left-Top => Left-Center               | Sep.04.2000       | Final         |
| 12                 | Marking Information Add<br>Revised<br>- AC Test Condition Add : 5pF Test Load | Dec.04.2000       | Final         |
| 13                 | Changed Logo<br>- HYUNDAI -> hynix<br>- Marking Information Change            | Apr.30.2001       | Final         |

## DESCRIPTION

The HY62V8100B is a high speed, low power and 1M bit CMOS SRAM organized as 131,072 words by 8bit. The HY62V8100B uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

## FEATURES

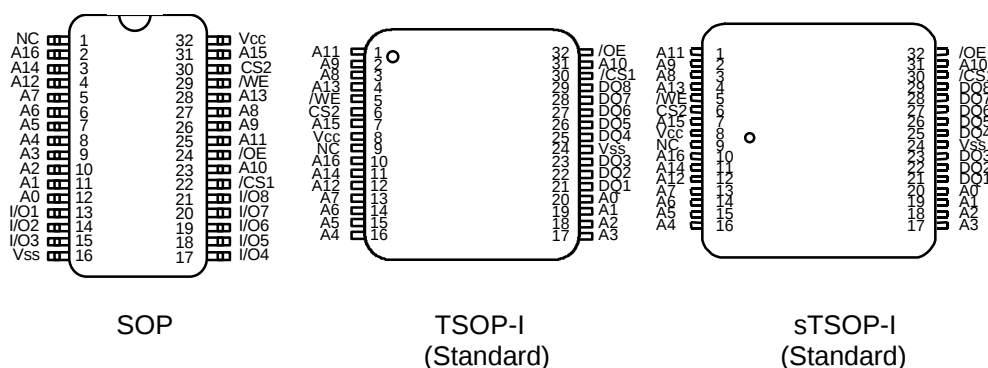
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 32 SOP - 525mil
  - 32 TSOP-I - 8X20(Standard and Reversed)
  - 32 sTSOP-I - 8X13.4 (Standard and Reversed)

| Product No.  | Voltage (V) | Speed (ns) | Operation Current/Icc(mA) | Standby Current(uA) LL | Temperature (°C) |
|--------------|-------------|------------|---------------------------|------------------------|------------------|
| HY62V8100B   | 3.0~3.6     | 70/85/100  | 5                         | 10                     | 0~70             |
| HY62V8100B-E | 3.0~3.6     | 70/85/100  | 5                         | 15                     | -25~85(E)        |
| HY62V8100B-I | 3.0~3.6     | 70/85/100  | 5                         | 15                     | -40~85(I)        |

Note 1. Blank : Commercial, E : Extended, I : Industrial

2. Current value is max.

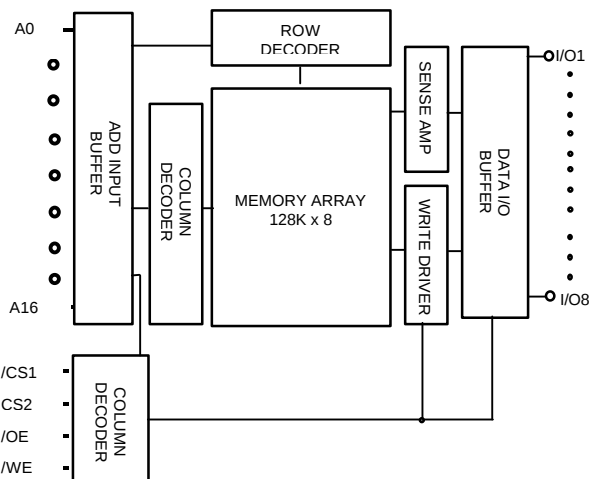
## PIN CONNECTION



## PIN DESCRIPTION

| Pin Name    | Pin Function          |
|-------------|-----------------------|
| /CS1        | Chip Select 1         |
| CS2         | Chip Select 2         |
| /WE         | Write Enable          |
| /OE         | Output Enable         |
| A0 ~ A16    | Address Inputs        |
| I/O1 ~ I/O8 | Data Inputs / Outputs |
| Vcc         | Power(3.0V~3.6V)      |
| Vss         | Ground                |

## BLOCK DIAGRAM



## ORDERING INFORMATION

| Part No.         | Speed     | Power   | Temp. | Package                  |
|------------------|-----------|---------|-------|--------------------------|
| HY62V8100BLLG    | 70/85/100 | LL-part |       | SOP                      |
| HY62V8100BLLT1   | 70/85/100 | LL-part |       | TSOP-I(Standard)         |
| HY62V8100BLLR1   | 70/85/100 | LL-part |       | TSOP-I(Reversed)         |
| HY62V8100BLLST   | 70/85/100 | LL-part |       | smaller TSOP-I(Standard) |
| HY62V8100BLLSR   | 70/85/100 | LL-part |       | smaller TSOP-I(Reversed) |
| HY62V8100BLLG-E  | 70/85/100 | LL-part | E     | SOP                      |
| HY62V8100BLLT1-E | 70/85/100 | LL-part | E     | TSOP-I(Standard)         |
| HY62V8100BLLR1-E | 70/85/100 | LL-part | E     | TSOP-I(Reversed)         |
| HY62V8100BLLST-E | 70/85/100 | LL-part | E     | smaller TSOP-I(Standard) |
| HY62V8100BLLSR-E | 70/85/100 | LL-part | E     | smaller TSOP-I(Reversed) |
| HY62V8100BLLG-I  | 70/85/100 | LL-part | I     | SOP                      |
| HY62V8100BLLT1-I | 70/85/100 | LL-part | I     | TSOP-I(Standard)         |
| HY62V8100BLLR1-I | 70/85/100 | LL-part | I     | TSOP-I(Reversed)         |
| HY62V8100BLLST-I | 70/85/100 | LL-part | I     | smaller TSOP-I(Standard) |
| HY62V8100BLLSR-I | 70/85/100 | LL-part | I     | smaller TSOP-I(Reversed) |

Note 1. Blank : Commercial, E : Extended, I : Industrial

## ABSOLUTE MAXIMUM RATING (1)

| Symbol                                               | Parameter                          | Rating      | Unit   | Remark       |
|------------------------------------------------------|------------------------------------|-------------|--------|--------------|
| V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub> | Power Supply, Input/Output Voltage | -0.3 to 4.6 | V      |              |
| T <sub>A</sub>                                       | Operating Temperature              | 0 to 70     | °C     | HY62V8100B   |
|                                                      |                                    | -25 to 85   | °C     | HY62V8100B-E |
|                                                      |                                    | -40 to 85   | °C     | HY62V8100B-I |
| T <sub>STG</sub>                                     | Storage Temperature                | -65 to 125  | °C     |              |
| P <sub>D</sub>                                       | Power Dissipation                  | 1.0         | W      |              |
| I <sub>OUT</sub>                                     | Data Output Current                | 50          | mA     |              |
| T <sub>SOLDER</sub>                                  | Lead Soldering Temperature & Time  | 260 • 10    | °C•sec |              |

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

## TRUTH TABLE

| /CS1 | CS2 | /WE | /OE | Mode            | I/O      | Power   |
|------|-----|-----|-----|-----------------|----------|---------|
| H    | X   | X   | X   | Deselected      | High-Z   | Standby |
| X    | L   | X   | X   | Deselected      | High-Z   | Standby |
| L    | H   | H   | H   | Output Disabled | High-Z   | Active  |
| L    | H   | H   | L   | Read            | Data Out | Active  |
| L    | H   | L   | X   | Write           | Data In  | Active  |

Note :

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care( V<sub>IH</sub> or V<sub>IL</sub> )

## RECOMMENDED DC OPERATING CONDITION

| Symbol          | Parameter          | Min.    | Typ. | Max.                 | Unit |
|-----------------|--------------------|---------|------|----------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 3.0     | 3.3  | 3.6                  | V    |
| V <sub>SS</sub> | Ground             | 0       | 0    | 0                    | V    |
| V <sub>IH</sub> | Input High Voltage | 2.2     | -    | V <sub>CC</sub> +0.3 | V    |
| V <sub>IL</sub> | Input Low Voltage  | -0.3(1) | -    | 0.6                  | V    |

Note :

1. V<sub>IL</sub> = -1.5V for pulse width less than 30ns and not 100% tested

## DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 3.0V~3.6V, T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E) / -40i 85i (E), unless otherwise specified

| Symbol           | Parameter                       |              | Test Condition                                                                                                                                                     | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| I <sub>LI</sub>  | Input Leakage Current           |              | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                                                                                                | -1   | -    | 1    | uA   |
| I <sub>LO</sub>  | Output Leakage Current          |              | V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> ,<br>/CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub><br>or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>     | -1   | -    | 1    | uA   |
| I <sub>CC</sub>  | Operating Power Supply Current  |              | /CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> ,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA                                  | -    |      | 5    | mA   |
| I <sub>CC1</sub> | Average Operating Current       |              | /CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> ,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>Cycle Time = Min, 100% duty,<br>I <sub>I/O</sub> = 0mA | -    |      | 35   | mA   |
| I <sub>SB</sub>  | TTL Standby Current (TTL Input) |              | /CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> ,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                                          | -    | -    | 0.5  | mA   |
| I <sub>SB1</sub> | Standby Current (CMOS Input)    | HY62V8100B   | /CS1 ≥ V <sub>CC</sub> - 0.2V or CS2 ≤ 0.2V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V                            | -    | 0.5  | 10   | uA   |
|                  |                                 | HY62V8100B-E |                                                                                                                                                                    | -    | 0.5  | 15   | uA   |
|                  |                                 | HY62V8100B-I |                                                                                                                                                                    | -    | 0.5  | 15   | uA   |
| V <sub>OL</sub>  | Output Low Voltage              |              | I <sub>OL</sub> = 2.1mA                                                                                                                                            | -    | -    | 0.4  | V    |
| V <sub>OH</sub>  | Output High Voltage             |              | I <sub>OH</sub> = -1mA                                                                                                                                             | 2.2  | -    | -    | V    |

Note : Typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C

## CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

| Symbol           | Parameter          | Condition             | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 0V  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>I/O</sub> = 0V | 8    | pF   |

Note : These parameters are sampled and not 100% tested

## AC CHARACTERISTICS

V<sub>cc</sub> = 3.0V~3.6V, T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E) / -25; 85; 100, unless otherwise specified

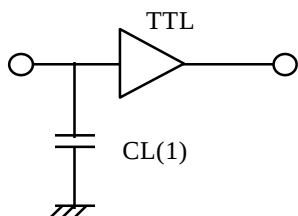
| #           | Symbol | Parameter                            | -70  |      | -85  |      | -10 |      | Unit |
|-------------|--------|--------------------------------------|------|------|------|------|-----|------|------|
|             |        |                                      | Min. | Max. | Min. | Max. | Min | Max. |      |
| READ CYCLE  |        |                                      |      |      |      |      |     |      |      |
| 1           | tRC    | Read Cycle Time                      | 70   | -    | 85   | -    | 100 | -    | ns   |
| 2           | tAA    | Address Access Time                  | -    | 70   | -    | 85   | -   | 100  | ns   |
| 3           | tACS   | Chip Select Access Time              | -    | 70   | -    | 85   | -   | 100  | ns   |
| 4           | tOE    | Output Enable to Output Valid        | -    | 40   | -    | 45   | -   | 50   | ns   |
| 5           | tCLZ   | Chip Select to Output in Low Z       | 10   | -    | 10   | -    | 10  | -    | ns   |
| 6           | tOLZ   | Output Enable to Output in Low Z     | 5    | -    | 5    | -    | 5   | -    | ns   |
| 7           | tCHZ   | Chip Deselection to Output in High Z | 0    | 30   | 0    | 30   | 0   | 30   | ns   |
| 8           | tOHZ   | Out Disable to Output in High Z      | 0    | 30   | 0    | 30   | 0   | 30   | ns   |
| 9           | tOH    | Output Hold from Address Change      | 10   | -    | 10   | -    | 15  | -    | ns   |
| WRITE CYCLE |        |                                      |      |      |      |      |     |      |      |
| 10          | tWC    | Write Cycle Time                     | 70   | -    | 85   | -    | 100 | -    | ns   |
| 11          | tCW    | Chip Selection to End of Write       | 60   | -    | 70   | -    | 80  | -    | ns   |
| 12          | tAW    | Address Valid to End of Write        | 60   | -    | 70   | -    | 80  | -    | ns   |
| 13          | tAS    | Address Set-up Time                  | 0    | -    | 0    | -    | 0   | -    | ns   |
| 14          | tWP    | Write Pulse Width                    | 50   | -    | 55   | -    | 75  | -    | ns   |
| 15          | tWR    | Write Recovery Time                  | 0    | -    | 0    | -    | 0   | -    | ns   |
| 16          | tWHZ   | Write to Output in High Z            | 0    | 25   | 0    | 30   | 0   | 35   | ns   |
| 17          | tDW    | Data to Write Time Overlap           | 30   | -    | 40   | -    | 45  | -    | ns   |
| 18          | tDH    | Data Hold from Write Time            | 0    | -    | 0    | -    | 0   | -    | ns   |
| 19          | tOW    | Output Active from End of Write      | 5    | -    | 5    | -    | 10  | -    | ns   |

## AC TEST CONDITIONS

T<sub>A</sub> = 0°C to 70°C / -25°C to 85°C (E) / -25; 85; 100, unless otherwise specified

| Parameter                               |                                                                                              | Value                  |
|-----------------------------------------|----------------------------------------------------------------------------------------------|------------------------|
| Input Pulse Level                       |                                                                                              | 0.4V to 2.2V           |
| Input Rise and Fall Time                |                                                                                              | 5ns                    |
| Input and Output Timing Reference Level |                                                                                              | 1.5V                   |
| Output Load                             | t <sub>CLZ</sub> , t <sub>OLZ</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> | CL = 5pF + 1TTL Load   |
|                                         | Others                                                                                       | CL = 100pF + 1TTL Load |

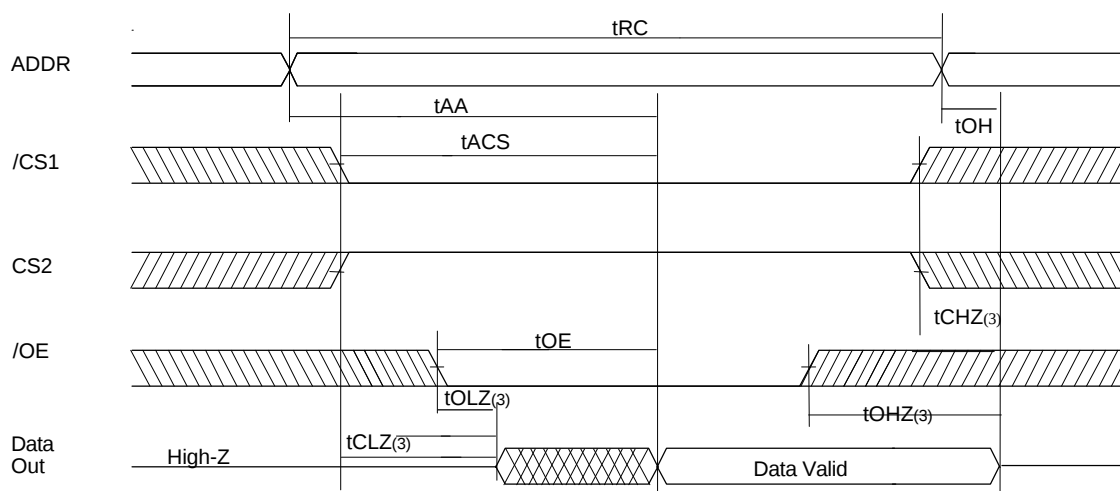
## AC TEST LOADS



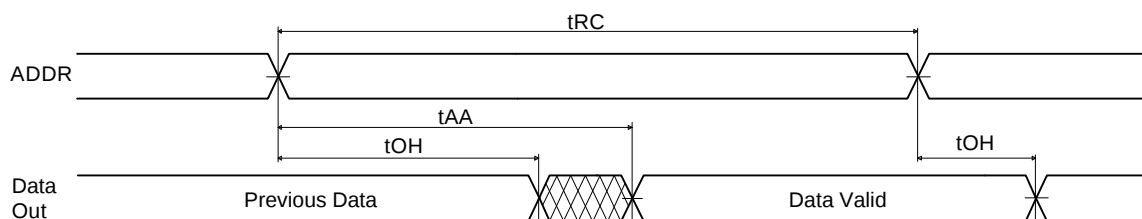
Note : 1 Including jig and scope capacitance

## TIMING DIAGRAM

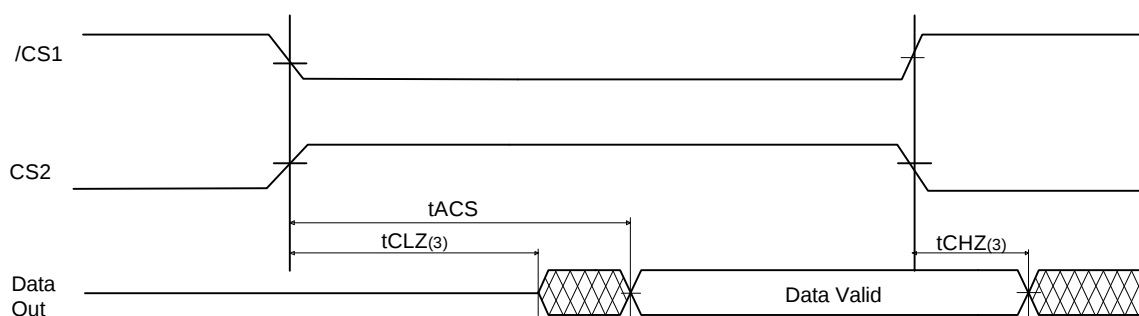
### READ CYCLE 1(Note 1,4)



### READ CYCLE 2(Note 1,2,4)



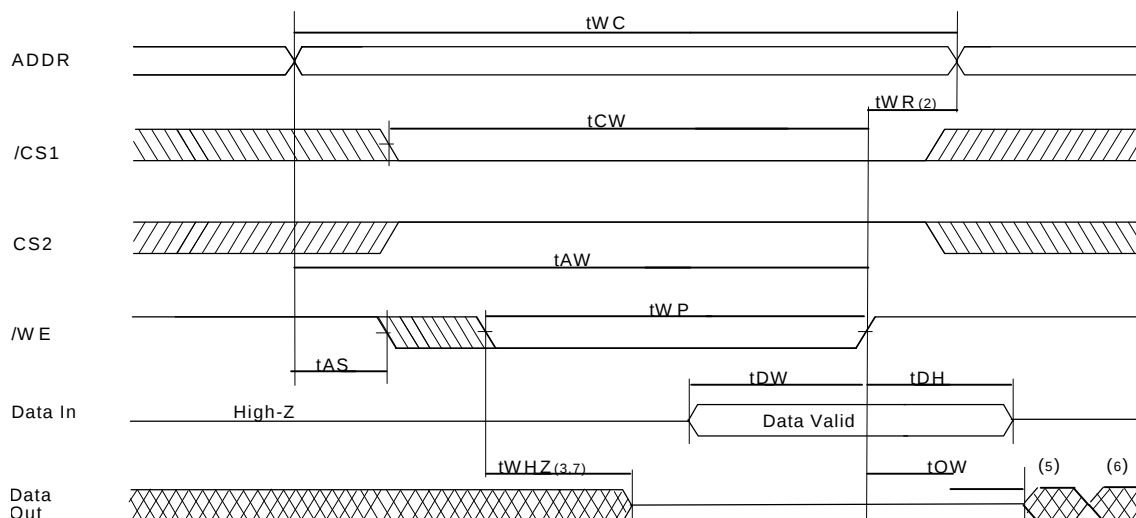
### READ CYCLE 3(Note 1,2,4)



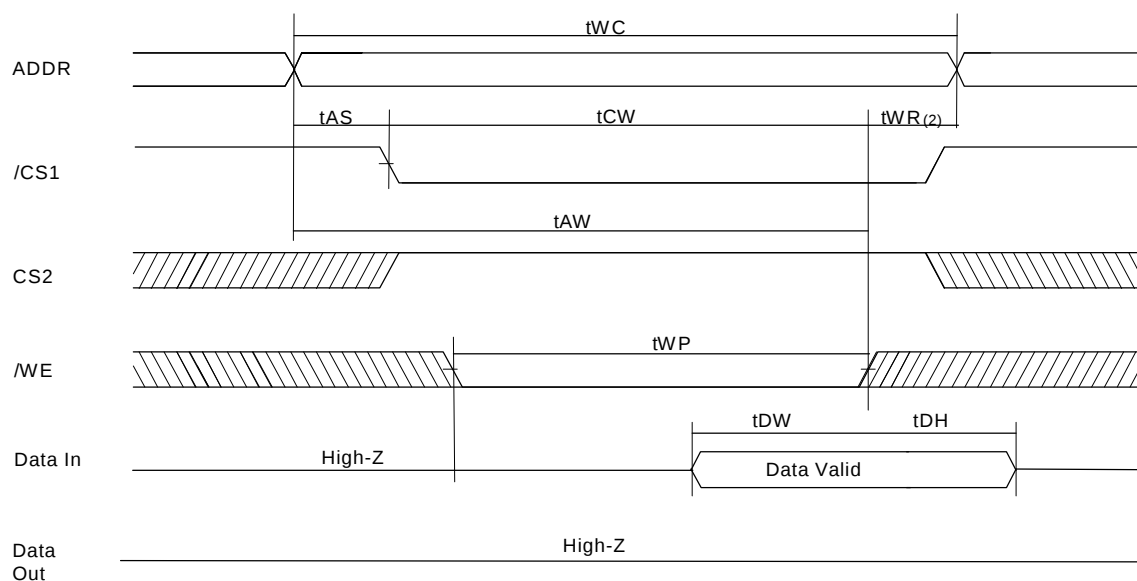
#### Notes:

1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS1 and a high CS2.
2. /OE =  $V_{IL}$
3. Transition is measured  $\pm 200\text{mV}$  from steady state voltage.  
This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active

### WRITE CYCLE 1(1,4,5,8) (/WE Controlled)



### WRITE CYCLE 2 (Note 1,4,5,8) (/CS1, CS2 Controlled)



#### Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1 and a high CS2.
2. tWR is measured from the earlier of /CS1 or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the the /CS1 low transition and CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured  $\pm 200\text{mV}$  from steady state.  
This parameter is sampled and not 100% tested.
8. /CS1 in high for the standby, low for active  
CS2 in low for the standby, high for active

## DATA RETENTION ELECTRIC CHARACTERISTIC

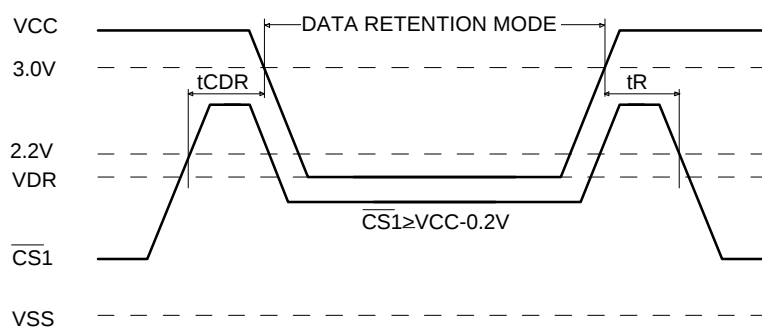
$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  /  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  (E) /  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  (J)

| Sym   | Parameter                            |              | Test Condition                                                                                               | Min    | Typ | Max | Unit          |
|-------|--------------------------------------|--------------|--------------------------------------------------------------------------------------------------------------|--------|-----|-----|---------------|
| VDR   | Vcc for Data Retention               |              | $/CS1 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$ ,<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$ | 2.0    | -   | -   | V             |
| ICCDR | Data Retention Current               | HY62V8100B   | $V_{CC} = 3.0V$ ,                                                                                            | -      | 0.5 | 10  | $\mu\text{A}$ |
|       |                                      | HY62V8100B-E | $/CS1 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$ ,                                                               | -      | 0.5 | 15  | $\mu\text{A}$ |
|       |                                      | HY62V8100B-I | $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$                                                   | -      | 0.5 | 15  | $\mu\text{A}$ |
| tCDR  | Chip Deselect to Data Retention Time |              | See Data Retention Timing Diagram                                                                            | 0      | -   | -   | ns            |
| tR    | Operating Recovery Time              |              |                                                                                                              | tRC(2) | -   | -   | ns            |

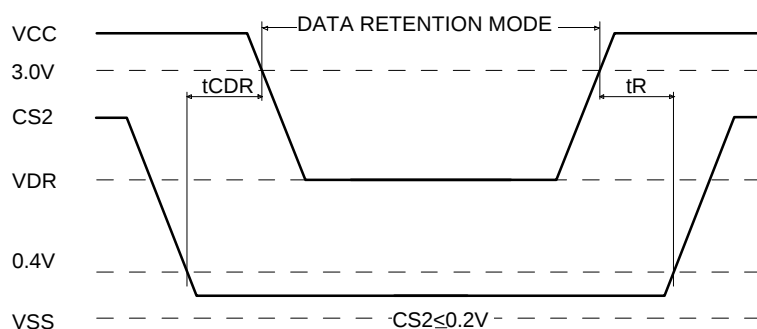
Notes:

1. Typical values are under the condition of  $T_A = 25^\circ\text{C}$ .
2. tRC is read cycle time.

### DATA RETENTION TIMING DIAGRAM 1

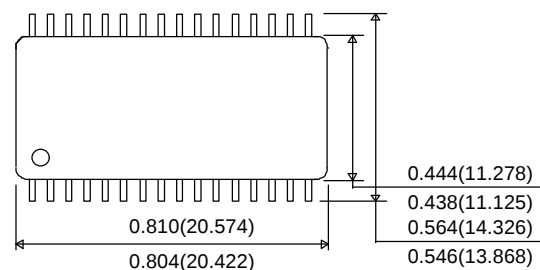


### DATA RETENTION TIMING DIAGRAM 2

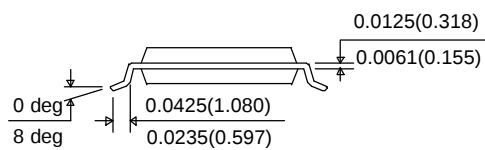
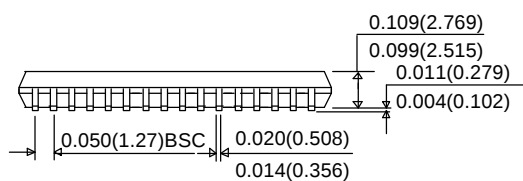


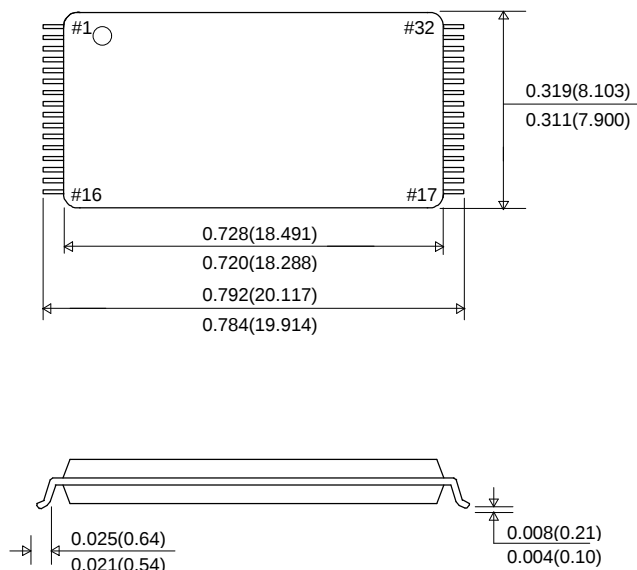
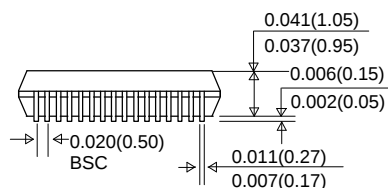
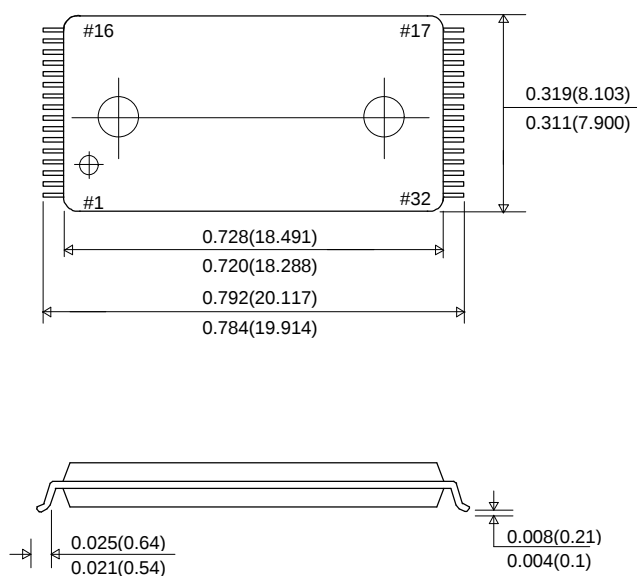
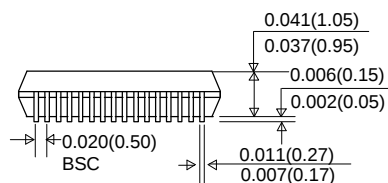
## PACKAGE INFORMATION

32pin 525mil Small Outline Package(G)

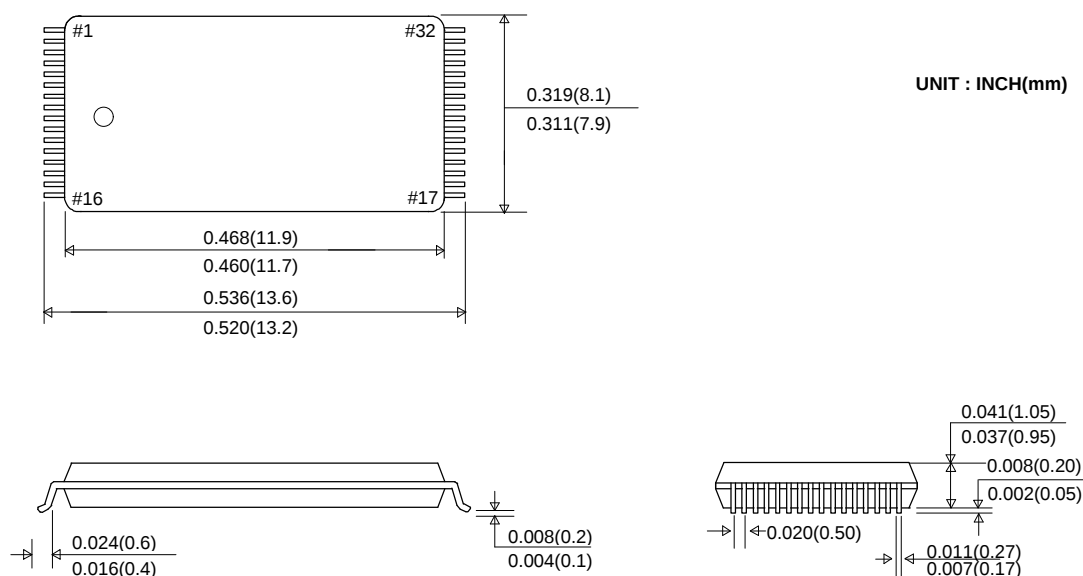


UNIT : INCH(mm)

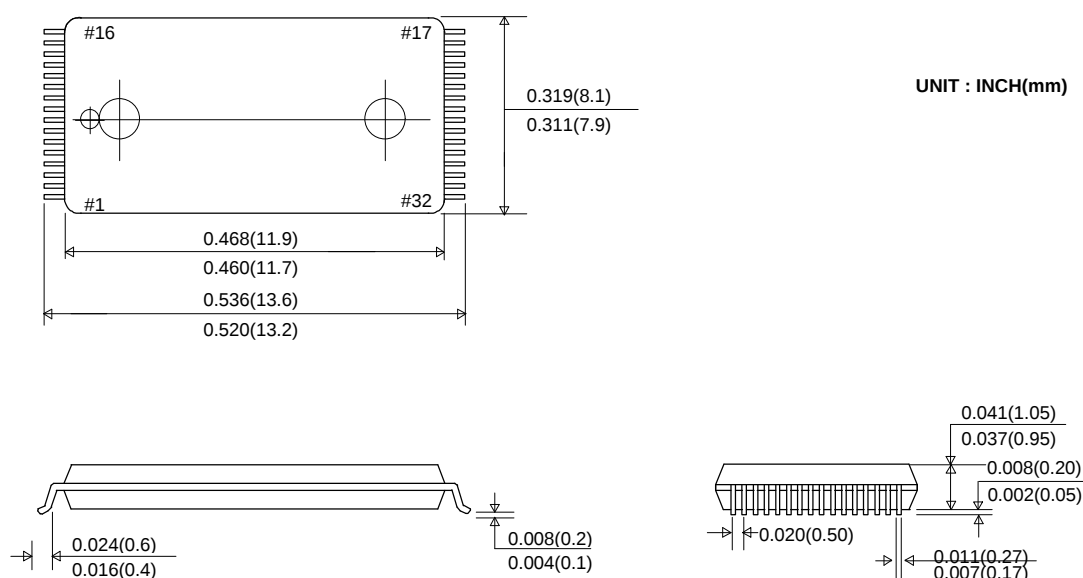


**32pin 8x20mm Thin Small Outline Package Standard(T1)**

**UNIT : INCH(mm)**

**32pin 8x20mm Thin Small Outline Package Reversed(R1)**

**UNIT : INCH(mm)**


32pin 8x13.4mm Samller Thin Small Outline Package Standard(ST)



32pin 8x13.4mm Smaller Thin Small Outline Package Reversed(SR)



# MARKING INFORMATION

| Package | Marking Example                                                                                              |
|---------|--------------------------------------------------------------------------------------------------------------|
| SOP     | <div>h y n i x      K O R E A</div> <div>H Y 6 2 V 8 1 0 0 B</div> <div>y y w w p      c c G - s s t</div>   |
| TSOP-I  | <div>h y n i x      K O R E A</div> <div>H Y 6 2 V 8 1 0 0 B</div> <div>y y w w p      c c T 1 - s s t</div> |
| sTSOP   | <div>H Y 6 2 V 8 1 0 0 B</div> <div>c c S T - s s t</div> <div>y y w w p      K O R</div>                    |

| Index            |                                                |                              |
|------------------|------------------------------------------------|------------------------------|
| • hynix          | : hynix Logo                                   |                              |
| • KOREA / KOR    | : Origin Country                               |                              |
| • HY62V8100B     | : Part Name                                    |                              |
| • yy             | : Year ( ex : 00 = year 2000, 01 = year 2001 ) |                              |
| • ww             | : Work Week ( ex : 12 = ww12 )                 |                              |
| • p              | : Process Code                                 |                              |
| • cc             | : Power Consumption                            |                              |
|                  | - L                                            | : Low Power                  |
|                  | - LL                                           | : Low Low Power              |
| • G / T1 / ST    | : Package Type                                 |                              |
|                  | - G                                            | : SOP                        |
|                  | - T1                                           | : TSOP-I                     |
|                  | - ST                                           | : sTSOP                      |
| • ss             | : Speed                                        |                              |
|                  | - 70                                           | : 70ns                       |
|                  | - 85                                           | : 85ns                       |
| • t              | : Temperature                                  |                              |
|                  | - Blank                                        | : Commercial ( 0 ~ 70 °C )   |
|                  | - E                                            | : Extended ( -25 ~ 85 °C )   |
|                  | - I                                            | : Industrial ( -40 ~ 85 °C ) |
| <b>Note</b>      |                                                |                              |
| - Capital Letter | : Fixed Item                                   |                              |
| - Small Letter   | : Non-fixed Item (Except hynix)                |                              |