National Semiconductor

March 21, 2008

LM3668
1A, High Efficiency Dual Mode Single Inductor Buck-Boost DC/DC Converter

General Description

The LM3668 is a synchronous buck-boost DC-DC converter optimized for powering low voltage circuits from a Li-Ion battery and input voltage rails between 2.5V and 5.5V. It has the capability to support up to 1A output current over the output voltage range. The LM3668 regulates the output voltage over the complete input voltage range by automatically switching between buck or boost modes depending on the input voltage.

The LM3668 has 2 N-channel MOSFETS and 2 P-channel MOSFETS arranged in a topology that provides continuous operation through the buck and boost operating modes. There is a MODE pin that allows the user to choose between an intelligent automatic PFM-PWM mode operation and forced PWM operation. During PWM mode, a fixed-frequency 2.2MHz (typ.) is used. PWM mode drives load up to 1A. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 45µA (typ.) at light loads during system standby. Internal synchronous rectification provides high efficiency. In shutdown mode (Enable pin pulled low) the device turns off and reduces battery consumption to 0.01µA (typ.).

The LM3668 is available in a 12-pin LLP package. A high switching frequency of 2.2MHz (typ.) allows the use of tiny surface-mount components including a 2.2µH inductor, a 10µF input capacitor, and a 22µF output capacitor.

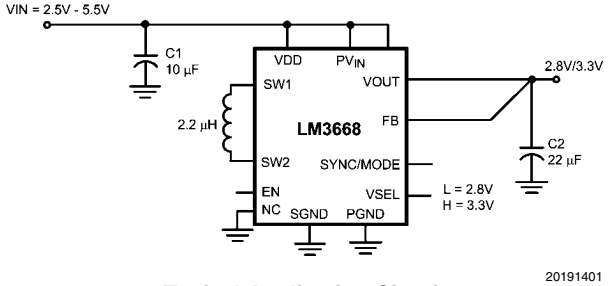
Features

- 45µA typical quiescent current
- For 2.8V/3.3V and 3.0/3.4V versions:
  - 1A maximum load current for V_{IN} = 2.8V to 5.5V
  - 800mA maximum load current for V_{IN} = 2.7V
  - 600mA maximum load current for V_{IN} = 2.5V
- For 4.5/5V
  - 1A maximum load current for V_{IN} = 3.9V to 5.5V
  - 800mA maximum load current for V_{IN} = 3.4V to 3.8V
  - 700mA maximum load current for V_{IN} = 3.0V to 3.3V
  - 600mA maximum load current for V_{IN} = 2.7V to 2.9V
- 2.2MHz PWM fixed switching frequency (typ.)
- Automatic PFM-PWM Mode or Forced PWM Mode
- Wide Input Voltage Range: 2.5V to 5.5V
- Internal synchronous rectification for high efficiency
- Internal soft start: 600µs Maximum start-up time after V_{IN} settled
- 0.01µA typical shutdown current
- Current overload and Thermal shutdown protection
- Frequency Sync Pin: 1.6MHz to 2.7MHz

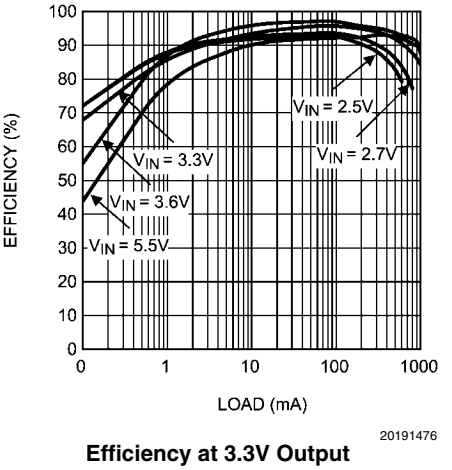
Applications

- Handset Peripherals
- MP3 players
- Pre-Regulation for linear regulators
- PDAs
- Portable Hard Disk Drives
- WiMax Modems

Typical Applications



Typical Application Circuit



Efficiency at 3.3V Output

Functional Block Diagram

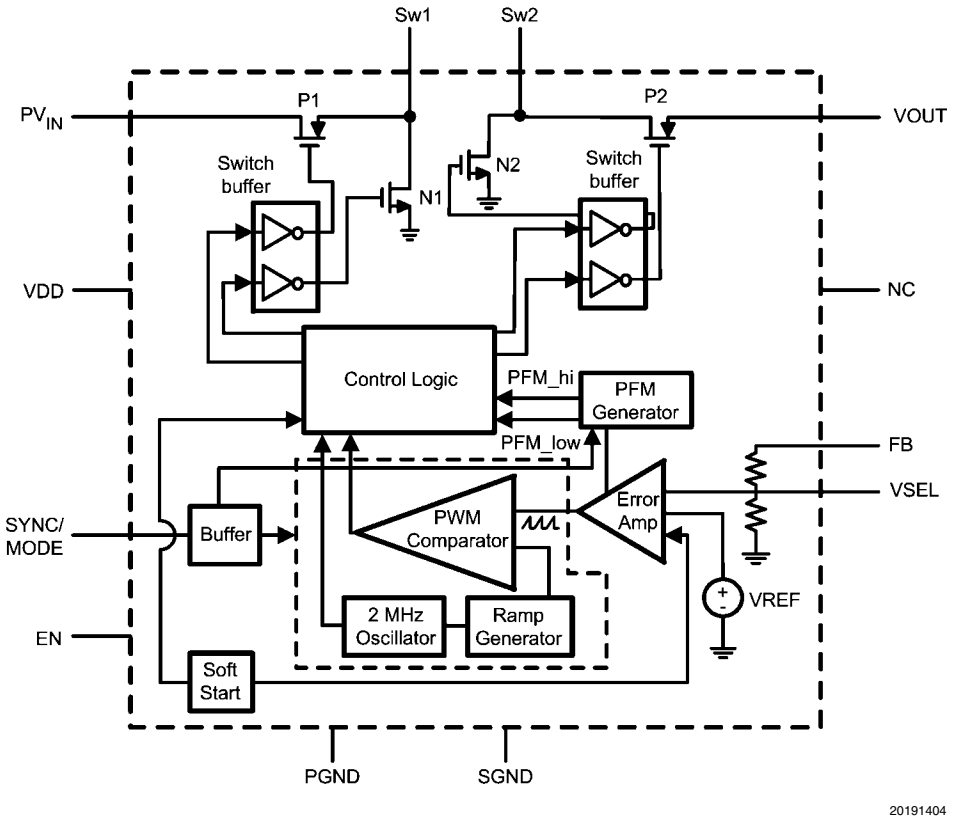
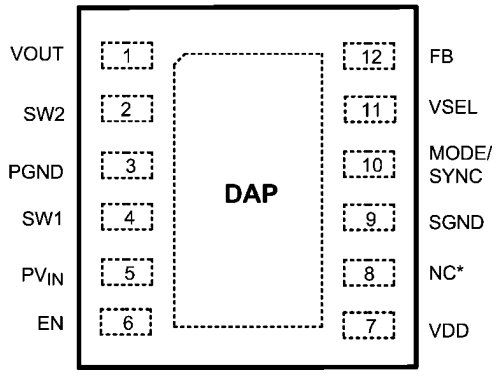
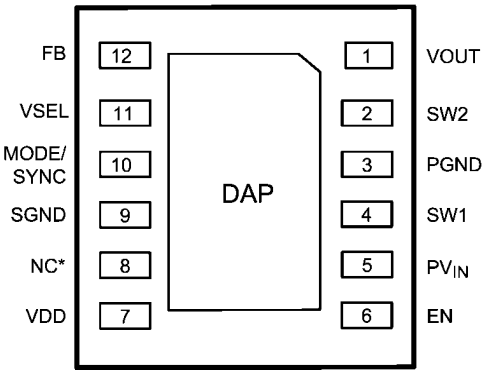


FIGURE 1. Functional Block Diagram

Connection Diagrams and Package Mark Information



Top View



Bottom View

Pin Descriptions

Pin #	Pin Name	Description
1	VOUT	Connect to output capacitor.
2	SW2	Switching Node connection to the internal PFET switch (P2) and NFET synchronous rectifier (N2).
3	PGND	Power Ground.
4	SW1	Switching Node connection to the internal PFET switch (P1) and NFET synchronous rectifier (N1).
5	PV_{IN}	Supply to the power switch, connect to the input capacitor.
6	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
7	VDD	Signal Supply input. If board layout is not optimum an optional 1µF ceramic capacitor is suggested as close to this pin as possible.
8	NC*	No connect. Connect this pin to GND on PCB layout.
9	SGND	Analog and Control Ground.
10	MODE/SYNC	Mode = LOW, Automatic Mode. Mode= HI, Forced PWM Mode SYNC = external clock synchronization from 1.6MHz to 2.7MHz (When SYNC function is used, device is forced in PWM mode).
11	VSEL	Voltage selection pin; (ie: 2.8V/3.3V option) Logic input low = 2.8V and logic high = 3.3V to set output Voltage.
12	FB	Feedback Analog Input. Connect to the output at the output filter.
DAP	DAP	Die Attach Pad, connect the DAP to SGND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

Ordering Information

Order Number	Package	NSC Package Marking	Supplied As
LM3668SD - 3.3[1]	LLP-12	S016B	1000 units, Tape and Reel
LM3668SDX - 3.3[1]			4500 units, Tape and Reel
LM3668SD-3034[2]	LLP-12	S018B	1000 units, Tape and Reel
LM3668SDX-3034[2]			4500 units, Tape and Reel
LM3668SD - 4550	LLP-12	S019B	1000 units, Tape and Reel
LM3668SDX - 4550			4500 units, Tape and Reel

Note 1: LM3668SD/X-3.3V will soon be replaced by new option LM3668SD/X-2833.
Note 2: As an example, if V_{OUT} option is 3.0V/3.4V, when V_{SEL} = Low, set V_{OUT} to 3V; when V_{SEL} = high, set V_{OUT} = 3.4V.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

PV_{IN}, V_{DD} Pin, SW1, SW2 & V_{OUT}: Voltage to SGND & PGND	−0.2V to +6.0V
FB, EN ,MODE, SYNC pins:	(PGND & SGND-0.2V) to (PV_{IN} + 0.2)
PGND to SGND	-0.2V to 0.2V
Continuous Power Dissipation (Note 3)	Internally Limited
Maximum Junction Temperature (T_{J-MAX})	+125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)	+260°C

Operating Ratings

Input Voltage Range	2.5V to 5.5V
Recommended Load Current	0mA to 1A
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range (Note 3)	−40°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), Leadless Lead frame Package (Note 5)	34°C/W

Electrical Characteristics (Notes 6, 7)

Limits in standard typeface are for T_J = +25°C. Limits in **boldface** type apply over the full operating ambient temperature range (−40°C ≤ = T_A ≤ +85°C). Unless otherwise noted, specifications apply to the LM3668. V_{IN} = 3.6V = EN, V_{OUT} = 3.3V. For V_{OUT} = 4.5/5.0V, V_{IN} = 4V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	(Note 7)	**-3**		**3**	%
I_{LIM}	Switch Peak Current Limit	Open loop(Note 2)	**1.6**	1.85	**2.05**	A
I_{SHDN}	Shutdown Supply Current	EN =0V		0.01	**1**	µA
I_{Q_PFM}	DC Bias Current in PFM	No load, device is not switching (FB forced higher than programmed output voltage)		45	**60**	µA
I_{Q_PWM}	DC Bias Current in PWM	PWM Mode, No Switching		600	**750**	µA
$R_{DSON(P)}$	Pin-Pin Resistance for PFET	Switches P1 and P2		130	180	mΩ
$R_{DSON(N)}$	Pin-Pin Resistance for NFET	Switches N1 and N2		100	150	mΩ
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**1.9**	2.2	**2.5**	MHz
F_{SYNC}	Sync Frequency Range	V_{IN} = 3.6V	1.6		2.7	MHz
V_{IH}	Logic High Input for EN, MODE/ SYNC pins		**1.1**			V
V_{IL}	Logic Low Input for EN, MODES/ SYNC pins				**0.4**	V
$I_{EN, MODE, SYNC}$	EN, MODES/SYNC pins Input Current			0.3	**1**	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle current limits is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

Note 3: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 4: The Human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 5: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 101.6mm x 76.2mm x 1.6mm. Thickness of the copper layers are 2oz/1oz/1oz/ 2oz. The middle layer of the board is 60mm x 60mm. Ambient temperature in simulation is 22°C, still air.

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 6: All voltage is with respect to SGND.

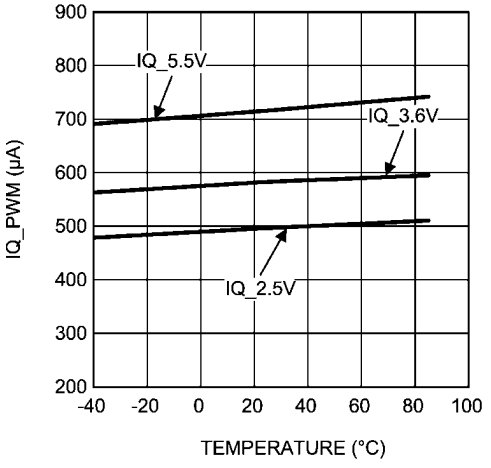
Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: C_{IN} and C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Typical Performance Characteristics

Typical Application Circuit (Figure 1): V_{IN} = 3.6V, L = 2.2µH, C_{IN} = 10µF, C_{OUT} = 22µF (Note 8), T_A = 25°C , unless otherwise stated.

Supply Current vs. Temperature (Not switching) (V_{OUT} = 3.4V)



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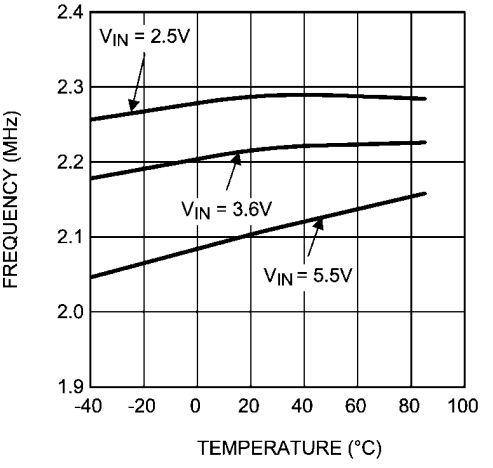
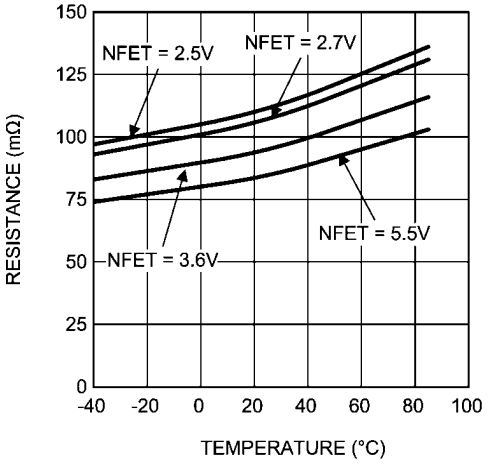
Switching Frequency vs. Temperature (V_{OUT} = 3.4V)



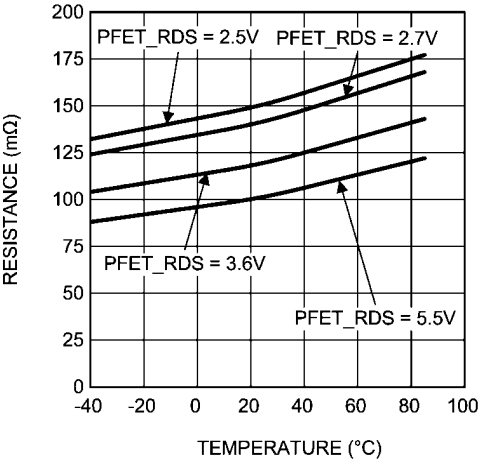
20191482

NFET_RDS (on) vs. Temperature (V_{OUT} = 3.4V)



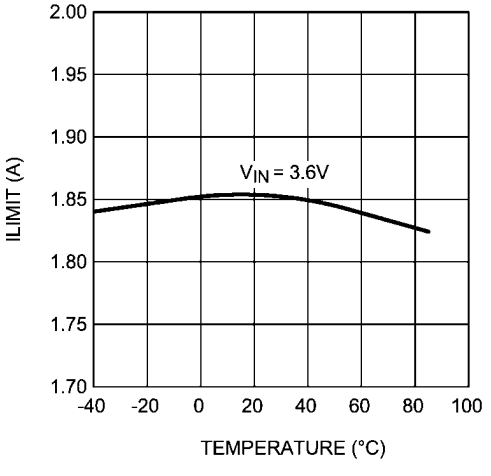
20191481

PFET_RDS (on) vs. Temperature (V_{OUT} = 3.4V)



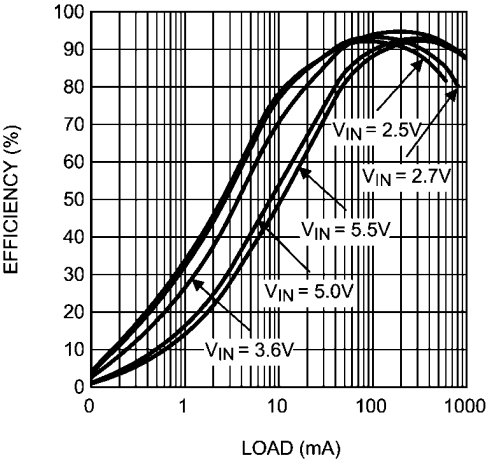
20191483

ILIMIT vs. Temperature (V_{OUT} = 3.4V)



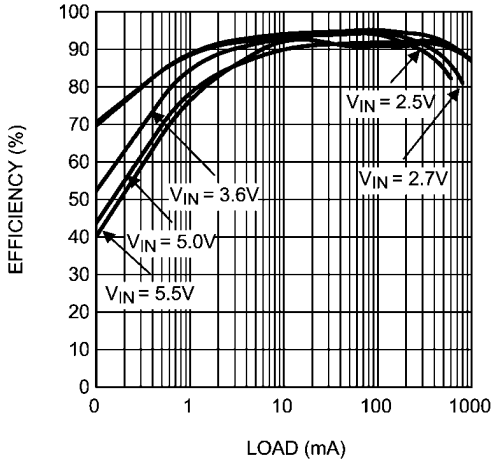
20191480

Efficiency at V_{OUT} = 3.0V (Forced PWM Mode)



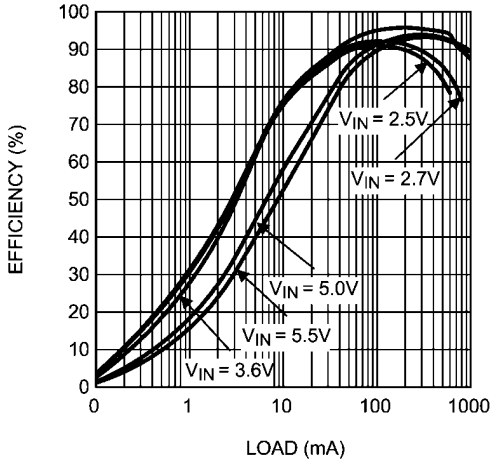
20191473

Efficiency at V_{OUT} = 3.0V (Auto Mode)



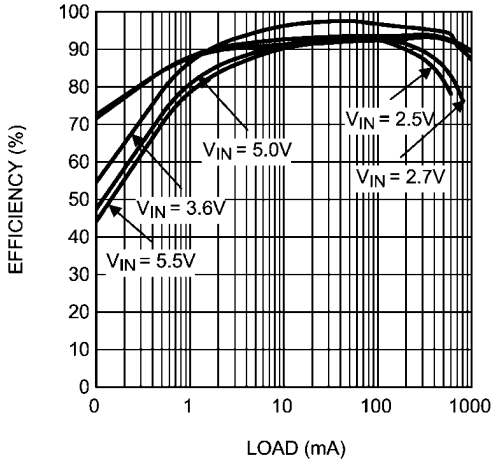
20191428

Efficiency at V_{OUT} = 3.4V (Forced PWM Mode)



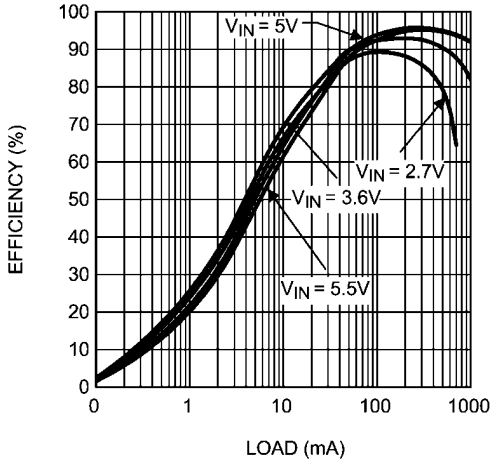
20191479

Efficiency at V_{OUT} = 3.4V (Auto Mode)



20191478

Efficiency at V_{OUT} = 4.5V (Forced PWM Mode)



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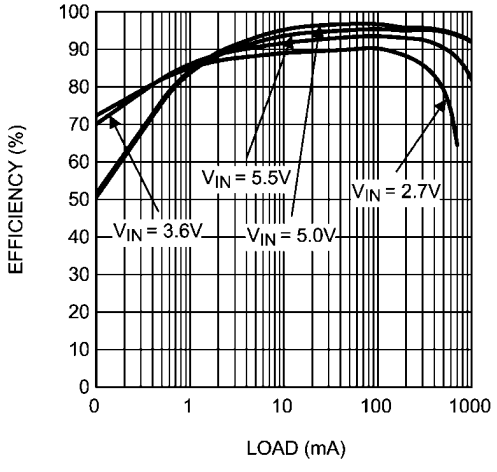
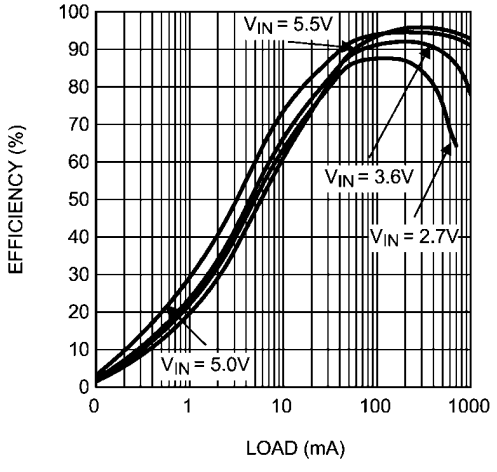
Efficiency at V_{OUT} = 4.5V (Auto Mode)



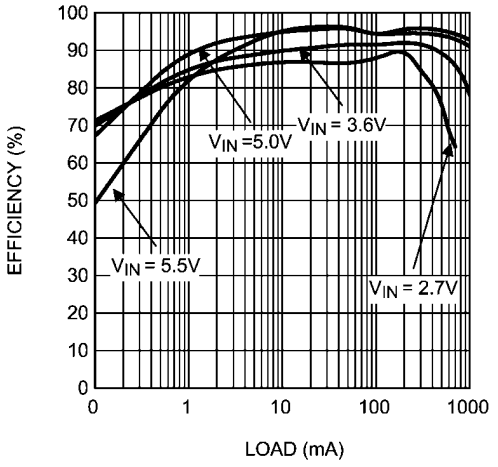
20191474

Efficiency at V_{OUT} = 5.0V (Forced PWM Mode)



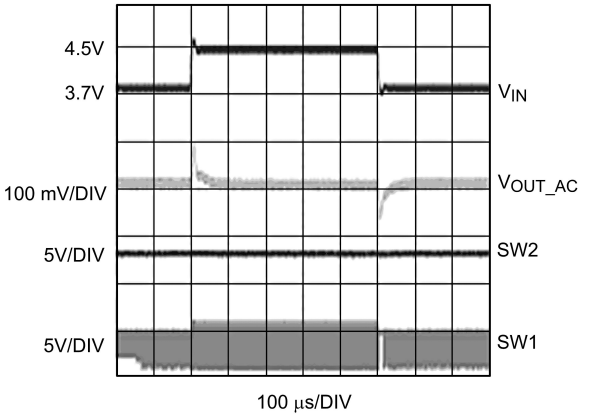
20191471

Efficiency at V_{OUT} = 5.0V (Auto Mode)



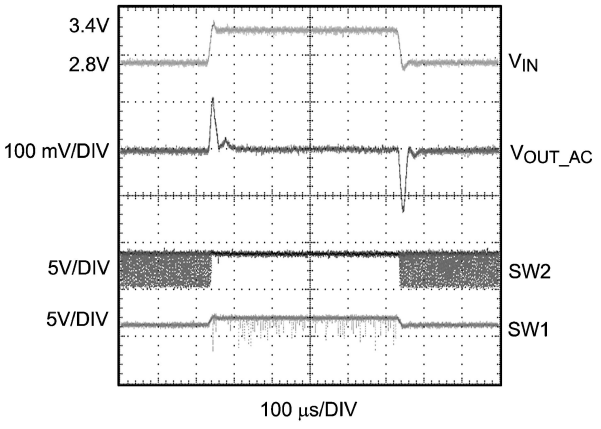
20191470

Line Transient in Buck Mode (V_{OUT} = 3.4V, Load = 500mA)



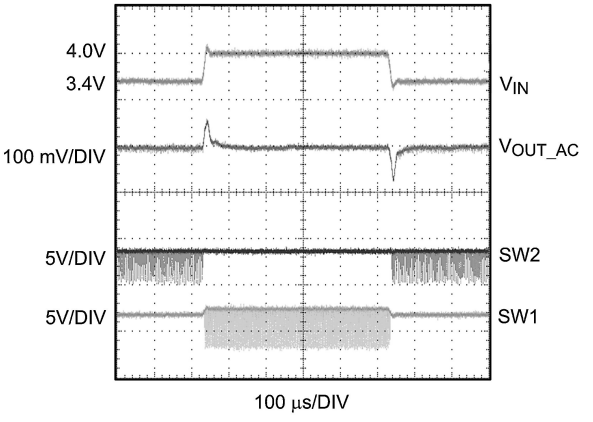
20191431

Line Transient in Boost Mode (V_{OUT} = 3.4V, Load = 500mA)



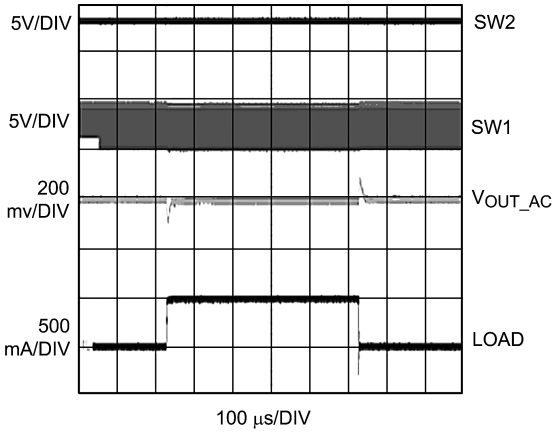
20191451

Line Transient in Buck-Boost Mode (V_{OUT} = 3.4V, Load = 500mA)



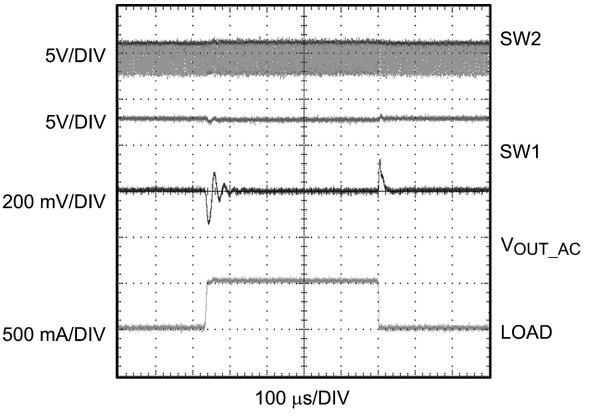
20191452

Load Transient in Buck Mode (Forced PWM Mode) V_{IN} = 4.2V, V_{OUT} = 3.4V, Load = 0-500mA



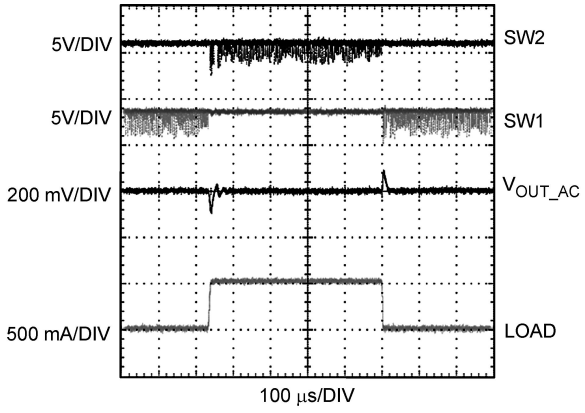
20191453

Load Transient in Boost Operation (Forced PWM Mode) V_{IN} = 2.7V, V_{OUT} = 3.4V, Load = 0-500mA



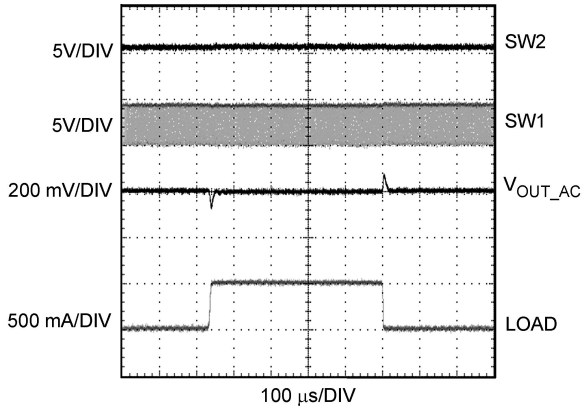
20191454

Load Transient in Buck-Boost Operation (Forced PWM Mode)
V_{IN} = 3.44V, V_{OUT} = 3.4V, Load = 0-500mA



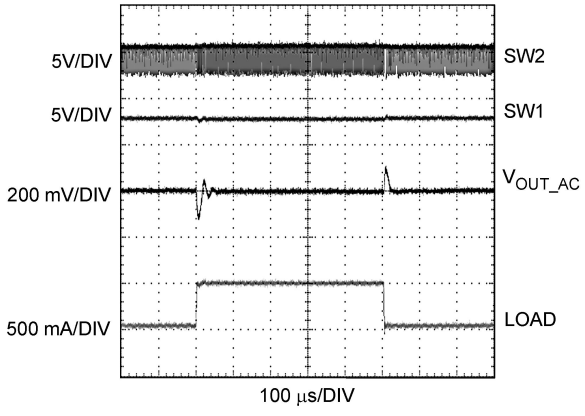
20191455

Load Transient in Buck Mode (Forced PWM Mode)
V_{IN} = 4.2V, V_{OUT} = 3.0V, Load = 0-500mA



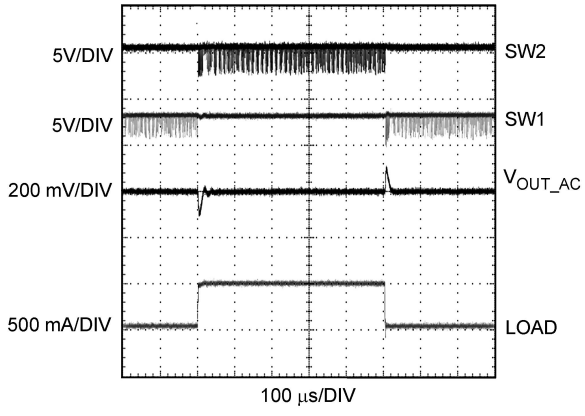
20191456

Load Transient in Boost Mode (Forced PWM Mode)
V_{IN} = 2.7V, V_{OUT} = 3.0V, Load = 0-500mA



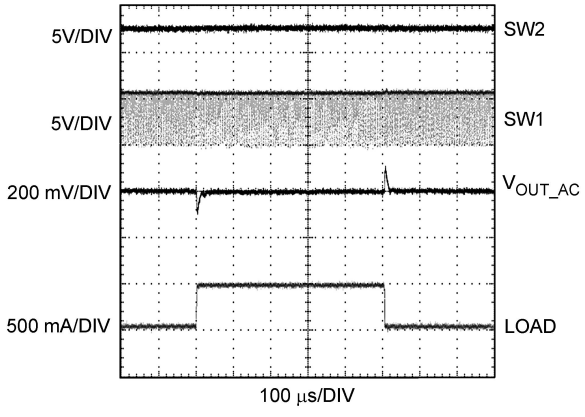
20191457

Load Transient in Buck-Boost Mode (Forced PWM Mode)
V_{IN} = 3.05V, V_{OUT} = 3.0V, Load = 0-500mA



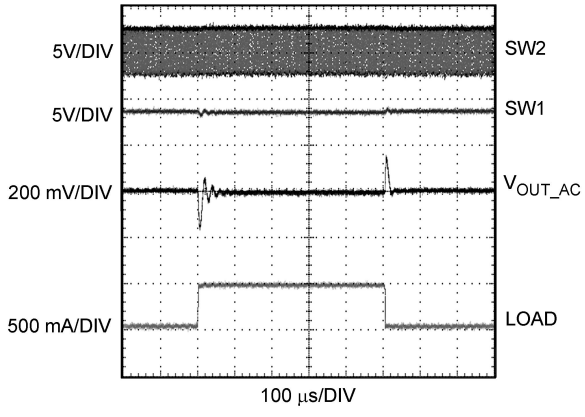
20191458

Load Transient in Buck Mode (Forced PWM Mode)
V_{IN} = 5.5V, V_{OUT} = 5.0V, Load = 0-500mA



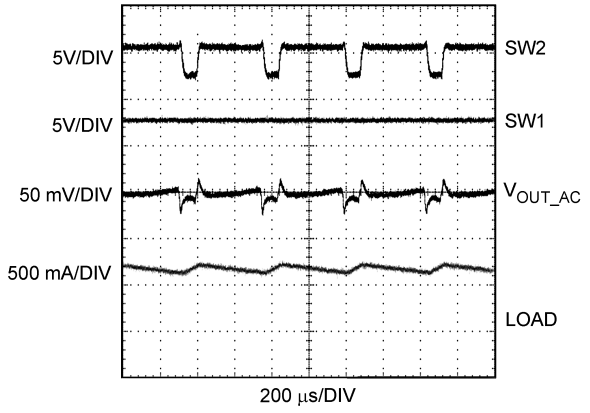
20191459

Load Transient in Boost Mode (Forced PWM Mode)
V_{IN} = 3.5V, V_{OUT} = 5.0V, Load = 0-500mA



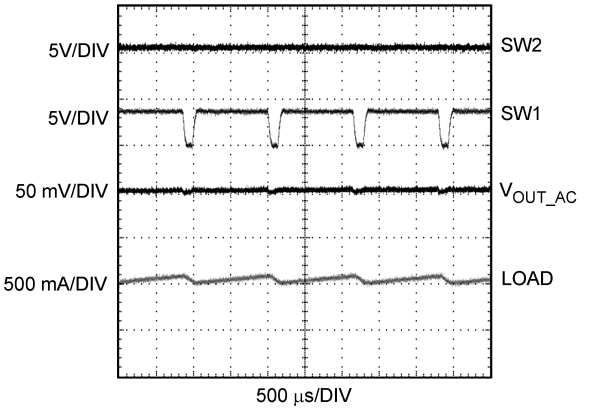
20191460

Typical Switching Waveform in Boost Mode (PWM Mode)
V_{IN} = 2.7V, V_{OUT} = 3.0V, Load = 500mA



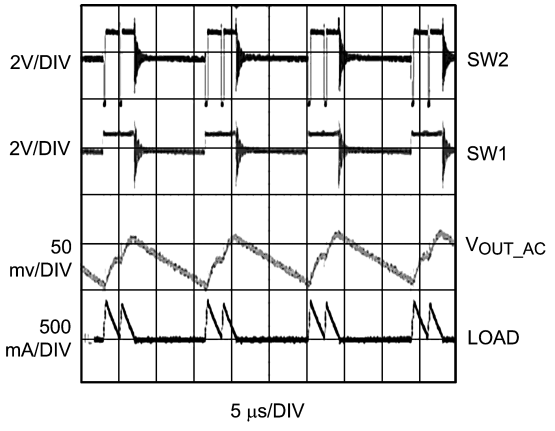
20191461

Typical Switching Waveform in Buck Mode (PWM Mode)
V_{IN} = 3.6V, V_{OUT} = 3.0V, Load = 500mA



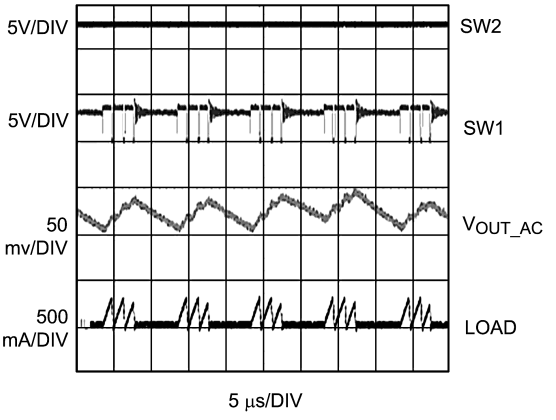
20191462

Typical Switching Waveformt in Boost Mode (PFM Mode)
V_{IN} = 2.7V, V_{OUT} = 3.0V, Load = 50mA



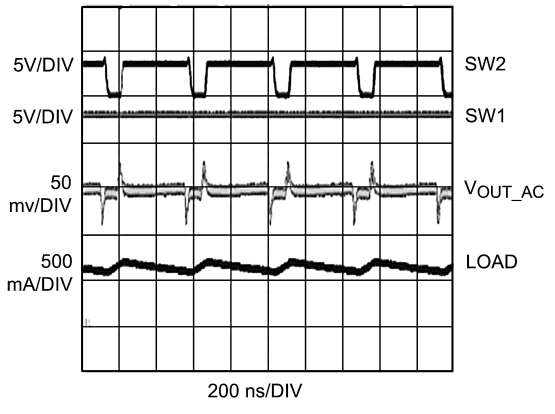
20191463

Typical Switching Waveform in Buck Mode (PFM Mode)
V_{IN} = 3.6V, V_{OUT} = 3.0V, Load = 50mA



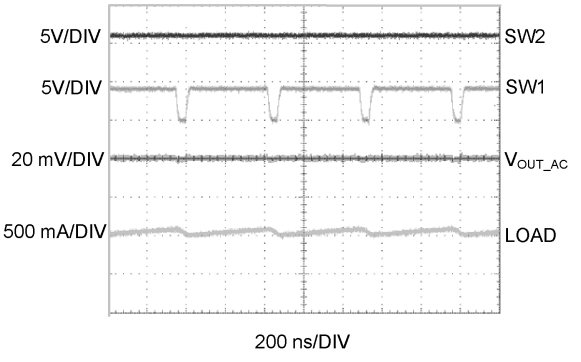
20191464

Typical Switching Waveform in Boost Mode (PWM Mode)
V_{IN} = 3V, V_{OUT} = 3.4V, Load = 500mA



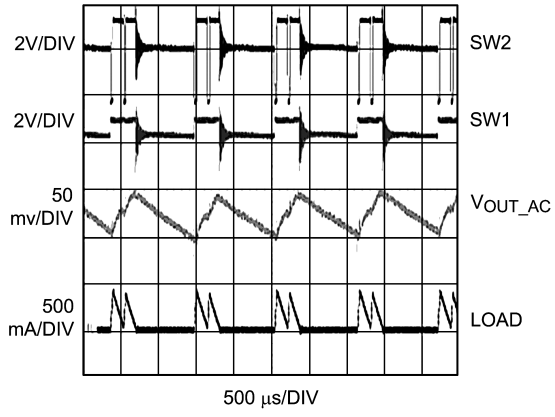
20191465

Typical Switching Waveform in Buck Mode (PWM Mode)
V_{IN} = 4V, V_{OUT} = 3.4V, Load = 500mA



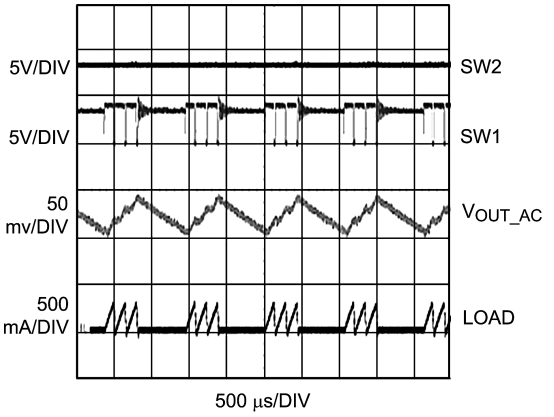
20191466

Typical Switching Waveform in Boost Mode (PFM Mode)
V_{IN} = 3V, V_{OUT} = 3.4V, Load = 50mA



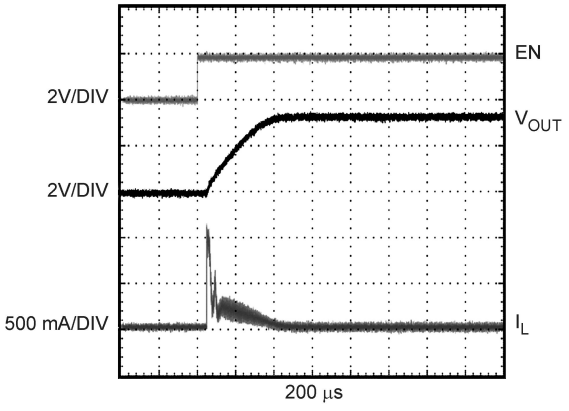
20191467

Typical Switching Waveform in Buck Mode (PFM Mode)
V_{IN} = 4V, V_{OUT} = 3.4V, Load = 50mA



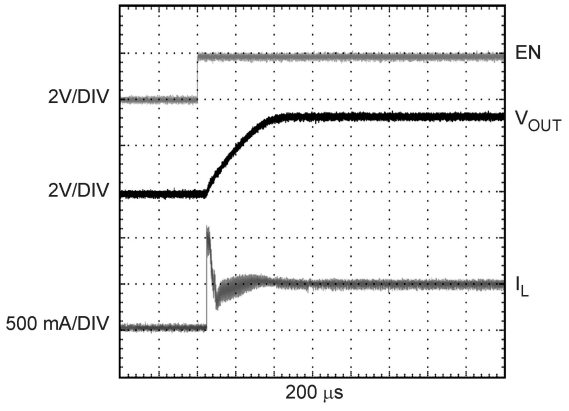
20191468

Start up in PWM Mode (V_{OUT} = 3.4V, Load = 1mA)



20191429

Start up in PWM Mode (V_{OUT} = 3.4V, Load = 500mA)



20191430

Circuit Description

The LM3668, a high-efficiency Buck or Boost DC-DC converter, delivers a constant voltage from either a single Li-Ion or three cell NIMH/NiCd battery to portable devices such as mobile phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3668 has the ability to deliver up to 1A depending on the input voltage, output voltage, ambient temperature and the chosen inductor.

In addition, the device incorporates a seamless transition from buck-to-boost or boost-to-buck mode. The internal error amplifier continuously monitors the output to determine the transition from buck-to-boost or boost-to-buck operation. *Figure 2* shows the four switches network used for the buck and boost operation. Table 1 summarizes the state of the switches in different modes.

There are three modes of operation depending on the current required: PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. The device operates in PWM mode at load currents of approximately 80mA or higher to improve efficiency. Lighter load current causes the device to automatically switch into PFM mode to reduce current consumption and extend battery life. Shutdown mode turns off the device, offering the lowest current consumption.

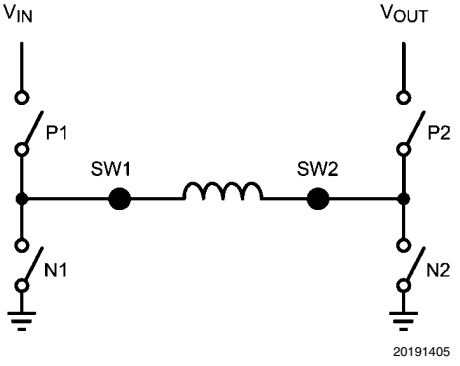


FIGURE 2. Simplified Diagram of Switches

State of Switches in Different Modes

Mode	Always ON	Always OFF	Switching
Buck	SW P2	SW N2	SW P1 & N1
Boost	SW P1	SW N1	SW N2 & P2

TABLE 1

Buck Operation

When the input voltage is greater than the output voltage, the device operates in buck mode where switch P2 is always ON and P1 & N1 control the output . Figure 3 shows the simplified circuit for buck mode operation.

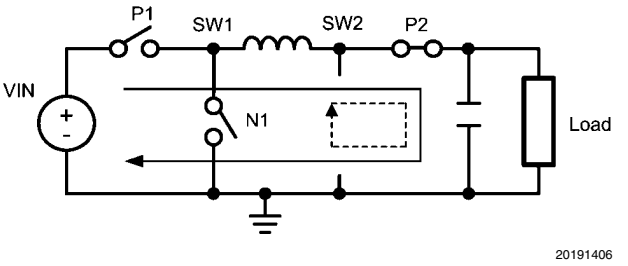


FIGURE 3. Simplified Circuit for Buck Operation

Boost Operation

When the input voltage is smaller than the output voltage, the device enters boost mode operation where P1 is always ON, while switches N2 & P2 control the output. Figure 4 shows the simplified circuit for boost mode operation.

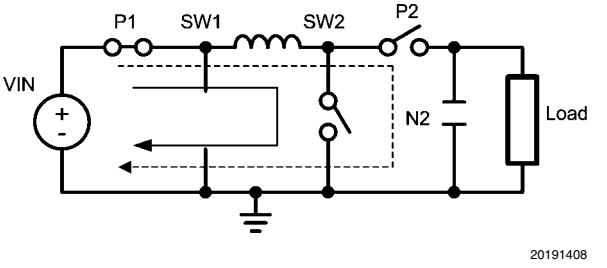


FIGURE 4. Simplified Circuit for Boost Operation

PWM Operation

In PWM operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. In Normal operation, the internal error amplifier provides an error signal, Vc, from the feedback voltage and Vref. The error amplifier signal, Vc, is compared with a voltage, Vcenter, and used to generate the PWM signals for both Buck & Boost modes. Signal Vcenter is a DC signal which sets the transition point of the buck and boost modes. Below are three regions of operation:

- Region I: If Vc is less than Vcenter, Buck mode.
- Region II: If Vc and Vcenter are equal, both PMOS switches (P1, P2) are on and both NMOS switches (N1, N2) are off. The power passes directly from input to output via P1 & P2
- Region III: If Vc is greater than Vcenter, Boost mode.

The Buck-Boost operation is avoided, to improve the efficiency across V_{IN} and load range.

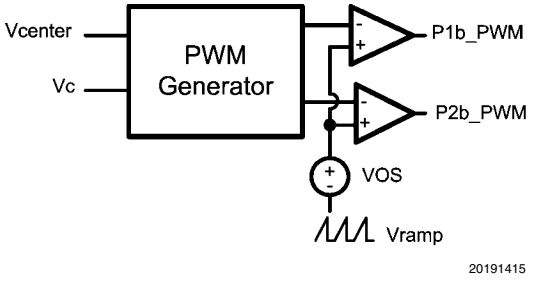


FIGURE 5. PWM Generator Block Diagram

Internal Synchronous Rectification

While in PWM mode, the LM3668 uses an internal MOSFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compare to the voltage drop across an ordinary rectifier diode.

PFM Operation

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. The part automatically transitions into PFM mode when either of two following conditions occur for a duration of 128 or more clock cycles:

A. The inductor current reaches zero.

B. The peak inductor current drops below the I_{MODE} level, (Typically I_{MODE} < 45mA + V_{IN}/80 Ω).

In PFM operation, the compensation circuit in the error amplifier is turned off. The error amplifier works as a hysteretic comparator. The PFM comparator senses the output voltage via the feedback pin and controls the switching of the output FETs such that the output voltage ramps between ~0.8% and ~1.6% of the nominal PWM output voltage (*Figure 6*). If the output voltage is below the 'high' PFM comparator threshold, the P1 & P2 (Buck mode) or N2 & P1 (Boost mode) power switches are turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 220mA

Once the P1 (Buck mode) or N2 (Boost mode) power switch is turned off, the N1 & P2 (Buck mode) or P1 & P2 (Boost mode) power switches are turned on until the inductor current ramps to zero. When the zero inductor current condition is detected, the N1(Buck mode) or P2 (Boost mode) power switches are turned off. If the output voltage is below the 'high' PFM comparator threshold, the P1 & P2 (Buck mode) or N2 & P1 (Boost mode) switches are again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the N1 & P2 (Buck mode) or P1 & P2 (Boost mode) switches are turned on briefly to ramp the inductor current to zero, then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 45µA (typ), which allows the part to achieve high efficiency under extremely light load conditions.

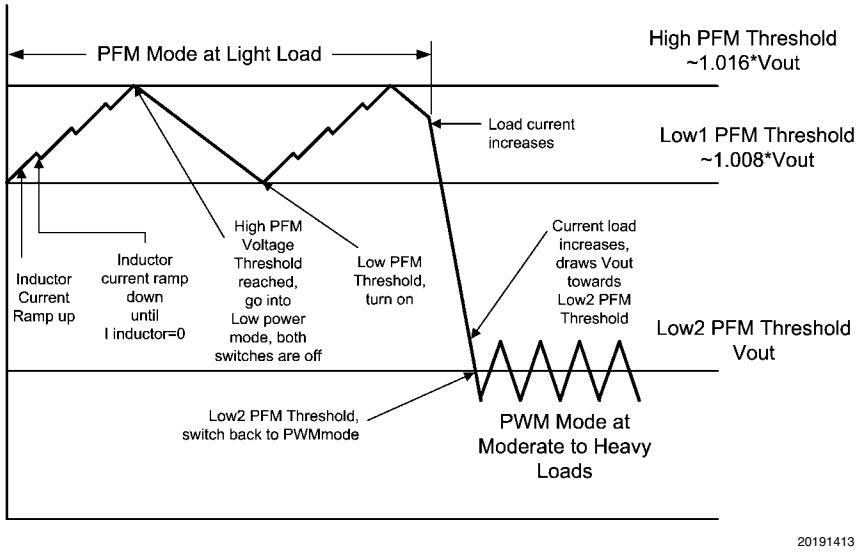


FIGURE 6. PFM to PWM Mode Transition

In addition to the auto mode transition, the LM3668 operates in PFM Buck or PFM Boost based on the following conditions. There is a small delta (~500mV) known as dv1(~200mV) & dv2(~300mV) when V_{OUT_TARGET} is very close to V_{IN} where the LM3668 can be in either Buck or Boost mode. For example, when V_{OUT_TARGET} = 3.3V and V_{IN} is between 3.1V & 3.6V, the LM3668 can be in either mode depending on the V_{IN} vs V_{OUT_TARGET} .

- Region I: If V_{IN} < V_{OUT_TARGET} - dv1, the regulator operates in Boost mode.
- Region II: If V_{OUT_TARGET} - dv1 < V_{IN} < V_{OUT_TARGET}+ dv2 ,the regulator operates in either Buck or Boost mode.
- Region III: If V_{IN} > V_{OUT_TARGET} + dv2, the regulator operates in Buck mode.

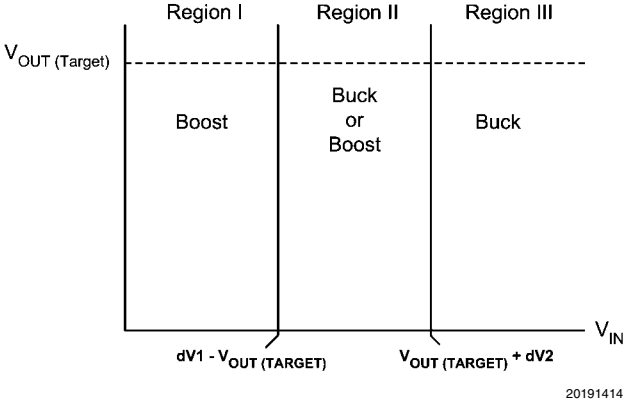


FIGURE 7. V_{OUT} vs V_{IN} Transition

In the buck PFM operation, P2 is always turned on and N2 is always turned off , P1 and N1 power switches are switching. P1 and N1 are turned off to enter " sleep mode" when the output voltage reaches the "high" comparator threshold. In boost PFM operation, P2 and N2 are switching. P1 is turned on and N1 is turned off when the output voltage is below the "high" threshold. Unlike in buck mode, all four power switches are turned off to enter "sleep" mode when the output voltage reaches the "high" threshold in boost mode. In addition, the internal current sensing of the I_{PFM} is used to determine the precise condition to switch over to buck or boost mode via the PFM generator.

Current Limit Protection

The LM3668 has current limit protection to prevent excessive stress on itself and external components during overload conditions. The internal current limit comparator will disable the power device at a typical switch peak current limit of 1.85A (typ.).

Under Voltage Protection

The LM3668 has an UVP comparator to turn the power device off in case the input voltage or battery voltage is too low . The typical UVP threshold is around 2V.

Short Circuit Protection

When the output of the LM3668 is shorted to GND, the current limit is reduced to about half of the typical current limit value until the short is removed.

Shutdown

When the EN pin is pulled low, P1 and P2 are off; N1 and N2 are turned on to pull SW1 and SW2 to ground.

Thermal Shutdown

The LM3668 has an internal thermal shutdown function to protect the die from excessive temperatures. The thermal shutdown trip point is typically 150°C; normal operation resumes when the temperature drops below 125°C.

Start-up

The LM3668 has a soft-start circuit that smooth the output voltage and ramp current during start-up. During start-up the bandgap reference is slowly ramped up and switch current limit is reduced to half the typical value. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.5V. The start-up time thereby depends on the output capacitor and load current demanded at start-up. It is not recommended to start up the device at full load while in soft-start.

Application Information

SYNC/MODE PIN

If the SYNC/MODE pin is set high, the device is set to operate at PWM mode only. If SYNC/MODE pin is set low, the device is set to automatically transition from PFM to PWM or PWM to PFM depending on the load current. **Do not leave this pin floating**. The SYNC/MODE pin can also be driven by an external clock to set the desired switching frequency between 1.6MHz to 2.7MHz.

V_{SEL} Pin

The LM3668 has built in logic for conveniently setting the output voltage, for example if V_{SEL} high, the output is set to 3.3V; with V_{SEL} low the output is set to 2.8V. It is not recommended to use this function for dynamically switching between 2.8V and 3.3V or switching at maximum load.

Maximum Current

The LM3668 is designed to operate up to 1A. For input voltages at 2.5V, the maximum operating current is 600mA and 800mA for 2.7V input voltage. In any mode it is recommended to avoid starting up the device at minimum input voltage and maximum load. Special attention must be taken to avoid operating near thermal shutdown when operating in boost mode at maximum load (1A). A simple calculation can be used to determine the power dissipation at the operating condition; $P_{D\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - T_{A\text{-}MAX})/\theta_{JA}$. The LM3668 has thermal resistance θ_{JA} = 34°C/W ((Note 3) and (Note 5)), and maximum operating ambient of 85°C. As a result, the maximum power dissipation using the above formula is around 1176mW. Refer to dissipation table below for $P_{D\text{-}MAX}$ value at different ambient temperatures.

Dissipation Rating Table

θ_{JA}	$T_A \le 25°C$	$T_A \le 60°C$	$T_A \le 85°C$
34°C/W (4 layers board per JEDEC standard)	2941mW	1912mW	1176mW

Inductor Selection

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

In the case of the LM3668, there are two modes (Buck & Boost) of operation that must be consider when selecting an inductor with appropriate saturation current. The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. The first equation shows the buck mode operation for worst case conditions and the second equation for boost condition.

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE} \quad \text{For Buck}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{(2 \times L \times f)} \times \frac{V_{OUT}}{V_{IN}}$$

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ \& } D' = (1\text{-}D)$$

- I_{RIPPLE}: Peak inductor current
- I_{OUTMAX}: Maximum load current
- V_{IN}: Maximum input voltage in application
- L : Min inductor value including worst case tolerances (30% drop can be considered)
- f : Minimum switching frequency
- V_{OUT}: Output voltage
- D: Duty Cycle for CCM Operation
- V_{OUT} : Output Voltage
- V_{IN}: Input Voltage

Example using above equations:

- V_{IN} = 2.8V to 4V
- V_{OUT} = 3.3V
- I_{OUT} = 500mA
- L = 2.2µH
- F = 2MHz
- Buck: I_{SAT} = 567mA
- Boost: I_{SAT} = 638mA

As a result, the inductor should be selected according to the highest of the two I_{SAT} values.

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 2.05A.

A 2.2µH inductor with a saturation current rating of at least 2.05A is recommended for most applications. The inductor's resistance should be less than 100mΩ for good efficiency. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin model is unacceptable.

Suggest Inductors and Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (max)	I_{SAT}
LPS4012-222L	Coilcraft	4 x 4 x 1.2	100 mΩ	2.1A
LPS4018-222L	Coilcraft	4 x 4 x 1.8	70 mΩ	2.5A
1098AS-2R0M (2µF)	TOKO	3 x 2.8x 1.2	67 mΩ	1.8A (lower current applications)

Input Capacitor Selection

A ceramic input capacitor of at least 10 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the PV_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 or 0603. The input filter capacitor supplies current to the PFET switch of the LM3668 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. For applications where input voltage is 4V or higher, it is best to use a higher voltage rating capacitor to eliminate the DC bias affect over capacitance.

Output Capacitor Selection

A ceramic output capacitor of 22µF, 6.3V (use 10V or higher rating for 4.5/5V output option) is sufficient for most applications. Multilayer ceramic capacitors such as X5R or X7R with low ESR is a good choice for this as well. These capacitors provide an ideal balance between small size, cost, reliability and performance. Do not use Y5V ceramic capacitors as they have poor dielectric performance over temperature and poor voltage characteristic for a given value.

Extra attention is required if a smaller case size capacitor is used in the application. Smaller case size capacitors typically have less capacitance for a given bias voltage as compared to a larger case size capacitor with the same bias voltage. Please contact the capacitor manufacturer for detail information regarding capacitance verses case size. Table 1 lists several capacitor suppliers.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

TABLE 1. Suggested Capacitors and Suppliers

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
10 µF for C_{IN} (For 4.5/5V option, use 10V or higher rating capacitor)				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)
LMK212 BJ106MG (+/-20%)	Ceramic, X5R	Taiyon-Yuden	10V	0806(2012)
LMK212 BJ106KG (+/-10%)	Ceramic, X5R	Taiyon-Yuden	10V	0805(2012)
22 µF for C_{OUT} (For 4.5/5V option, use 10V or higher rating capacitor)				
JMK212BJ226MG	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
LMK212BJ226MG	Ceramic, X5R	Taiyo-Yuden	10V	0805 (2012)

Layout Considerations

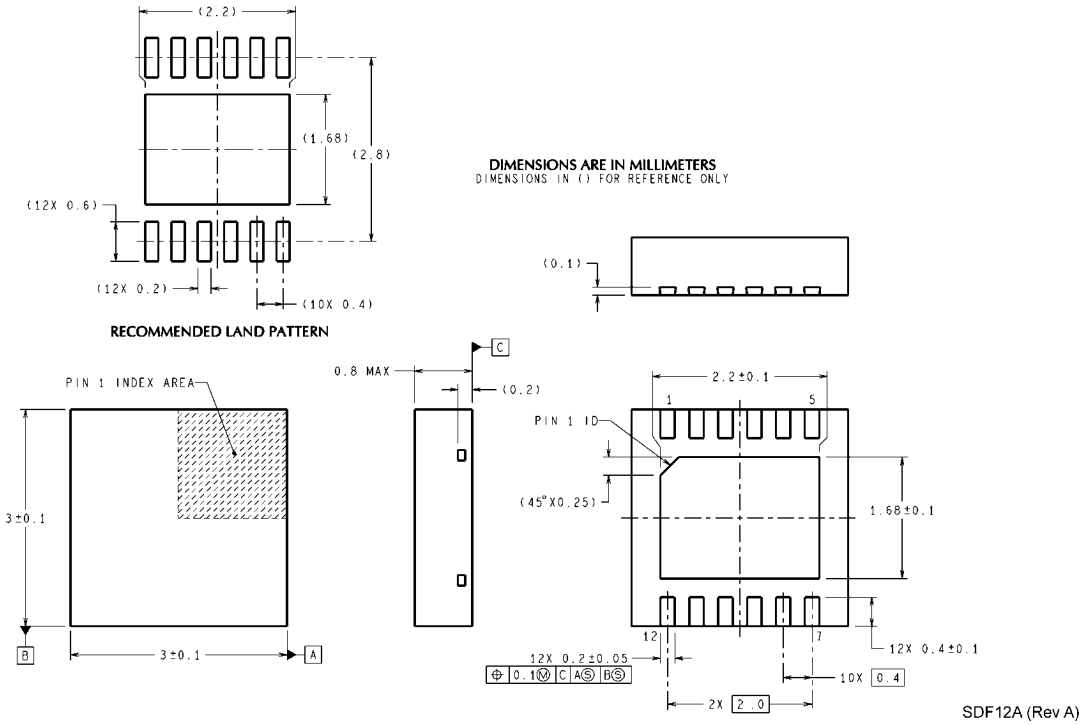
As for any high frequency switcher, it is important to place the external components as close as possible to the IC to maximize device performance. Below are some layout recommendations:

1) Place input filter and output filter capacitors close to the IC to minimize copper trace resistance which will directly effect the overall ripple voltage.

2) Route noise sensitive trace away from noisy power components. Separate power GND (Noisy GND) and Signal GND (quiet GND) and star GND them at a single point on the PCB preferably close to the device GND pin.

3) Connect the ground pins and filter capacitors together via a ground plane to prevent switching current circulating through the ground plane. Additional layout consideration regarding the LLP package can be found in Application AN 1187.

Physical Dimensions inches (millimeters) unless otherwise noted



12–Pin LLP
NS Package Number SDF12A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
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