

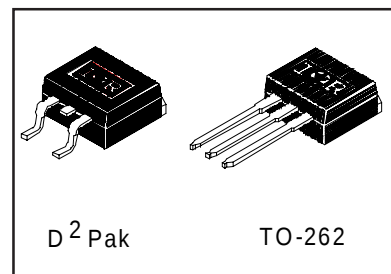
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V_{DSS}	$R_{ds(on)}$ max	I_D
400V	1.0 Ω	5.5A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified (See AN1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V⑥	5.5	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V⑥	3.5	
I_{DM}	Pulsed Drain Current ①⑥	22	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	74	W
	Linear Derating Factor	0.6	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③⑥	4.6	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies:

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset
(Both US Line input only).

Notes ① through ⑥ are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

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	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.5	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.0	Ω	$V_{GS} = 10V, I_D = 3.3A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 320V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.1	—	—	S	$V_{DS} = 50V, I_D = 3.3A$ ⑥
Q_g	Total Gate Charge	—	—	22	nC	$I_D = 3.5A$
Q_{gs}	Gate-to-Source Charge	—	—	5.8		$V_{DS} = 320V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.3		$V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑥
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 200V$
t_r	Rise Time	—	22	—		$I_D = 3.5A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 12\Omega$
t_f	Fall Time	—	16	—		$R_D = 57\Omega$, See Fig. 10 ④ ⑥
C_{iss}	Input Capacitance	—	600	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	103	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	4.0	—		$f = 1.0MHz$, See Fig. 5 ⑥
C_{oss}	Output Capacitance	—	890	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	30	—		$V_{GS} = 0V, V_{DS} = 320V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	45	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 320V$ ⑤ ⑥

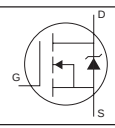
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ② ⑥	—	290	mJ
I_{AR}	Avalanche Current ①	—	5.5	A
E_{AR}	Repetitive Avalanche Energy ① ⑥	—	7.4	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.7	$^\circ\text{C}/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	22		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 5.5A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	370	550	ns	$T_J = 25^\circ\text{C}, I_F = 3.5A$
Q_{rr}	Reverse Recovery Charge	—	1.6	2.4	μC	$di/dt = 100A/\mu s$ ④ ⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

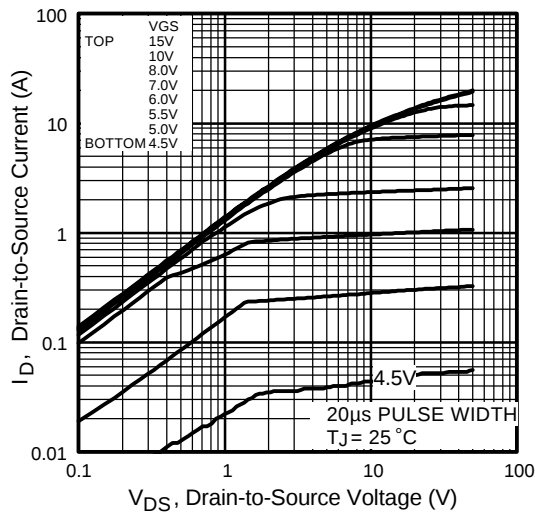


Fig 1. Typical Output Characteristics

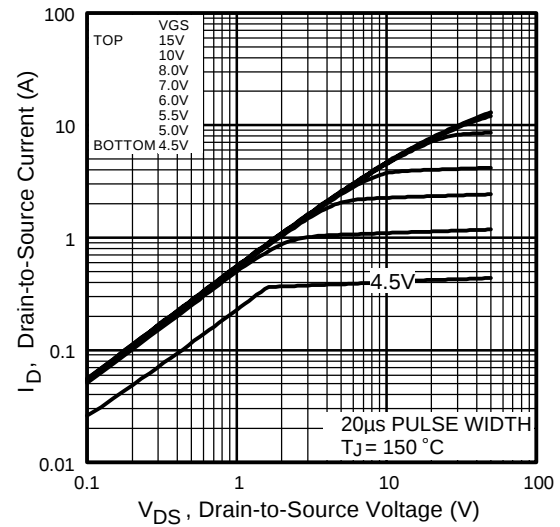


Fig 2. Typical Output Characteristics

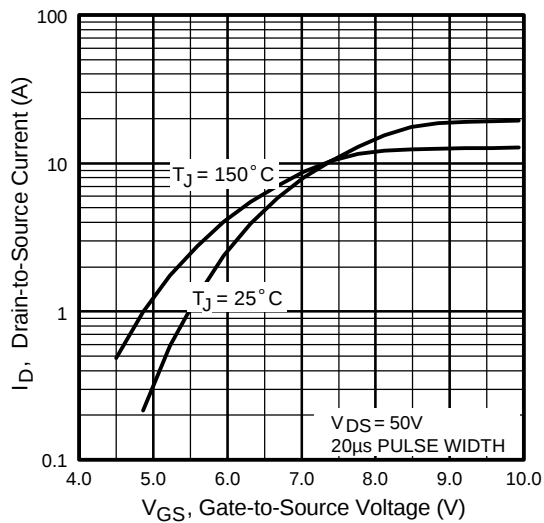


Fig 3. Typical Transfer Characteristics

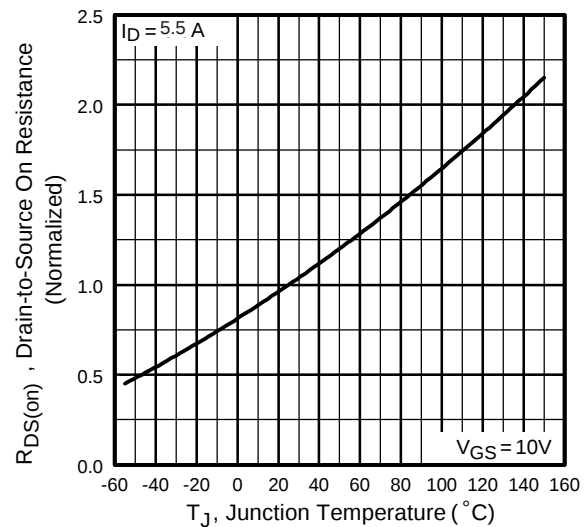
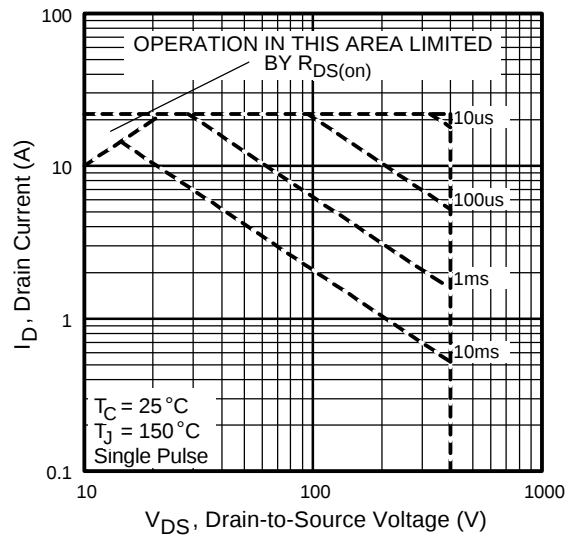
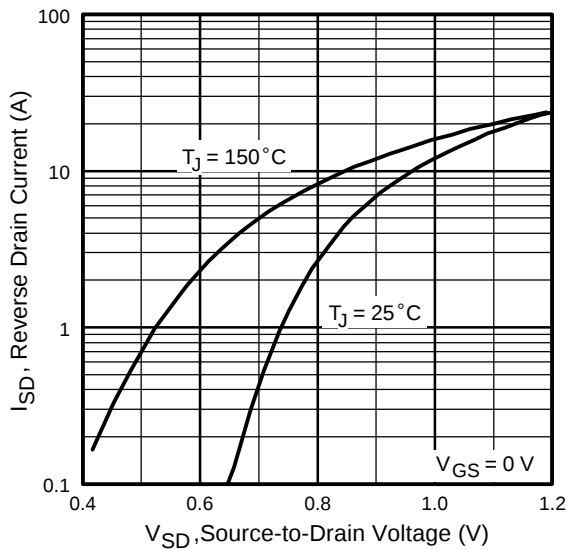
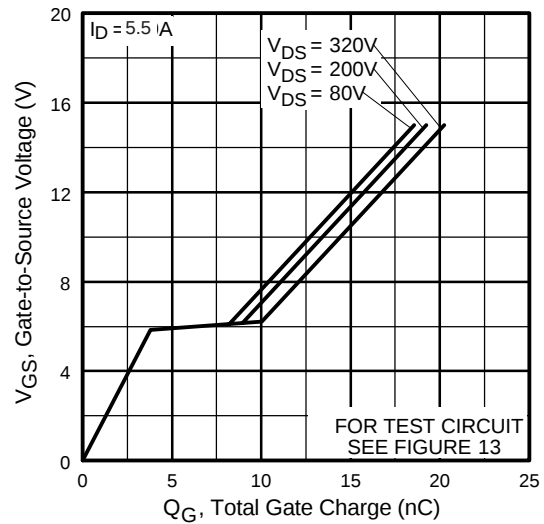
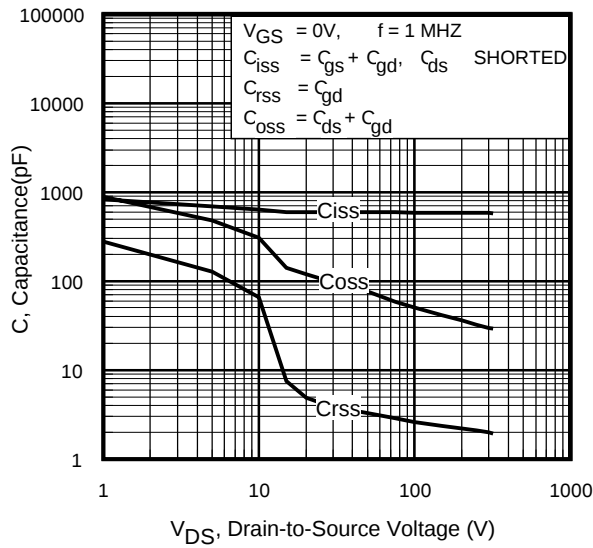


Fig 4. Normalized On-Resistance
Vs. Temperature

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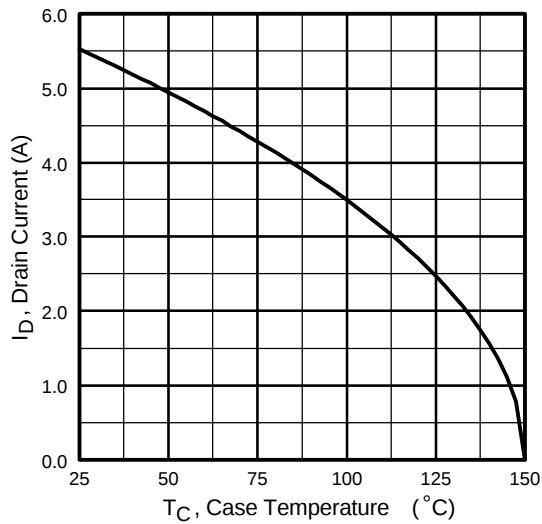


Fig 9. Maximum Drain Current Vs. Case Temperature

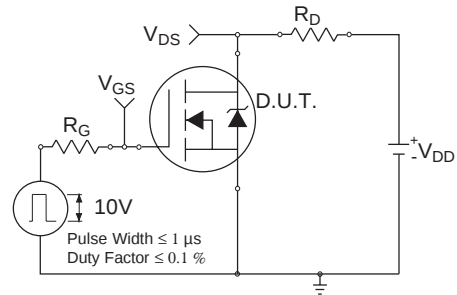


Fig 10a. Switching Time Test Circuit

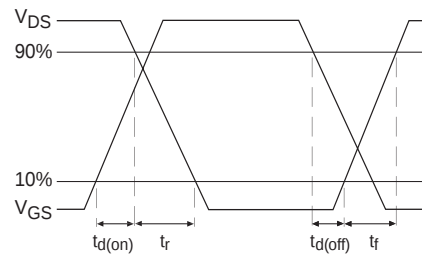


Fig 10b. Switching Time Waveforms

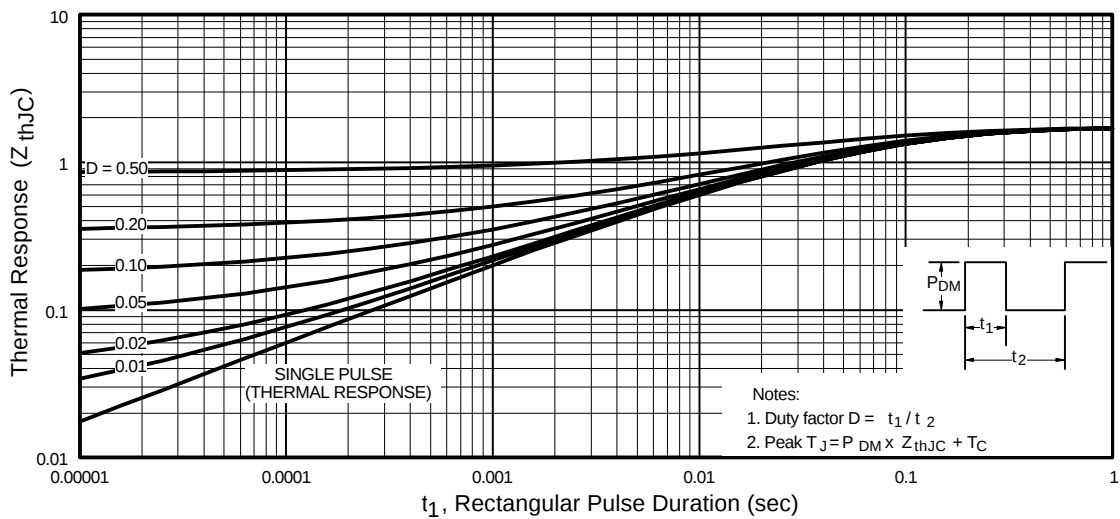


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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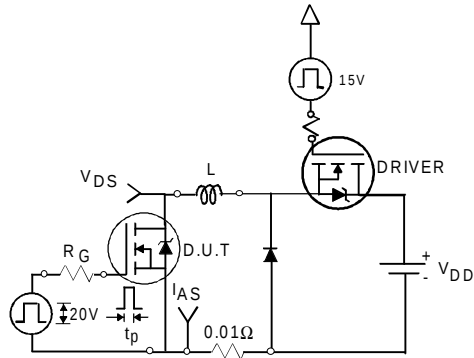


Fig 12a. Unclamped Inductive Test Circuit

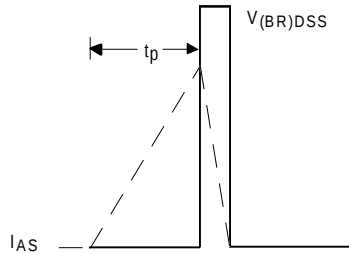


Fig 12b. Unclamped Inductive Waveforms

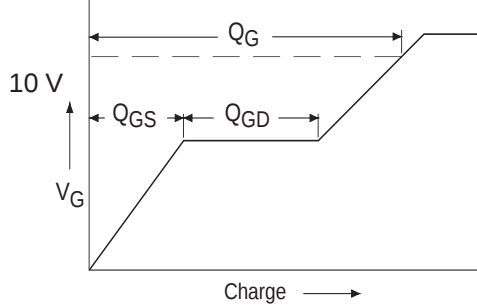


Fig 13a. Basic Gate Charge Waveform

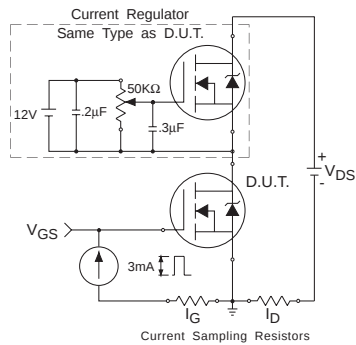


Fig 13b. Gate Charge Test Circuit

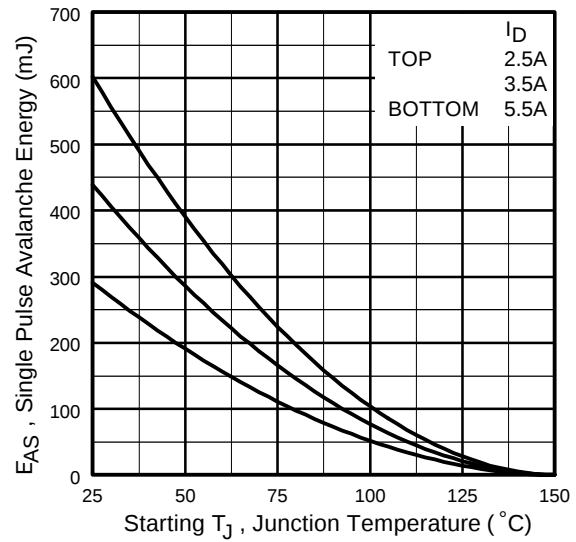


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

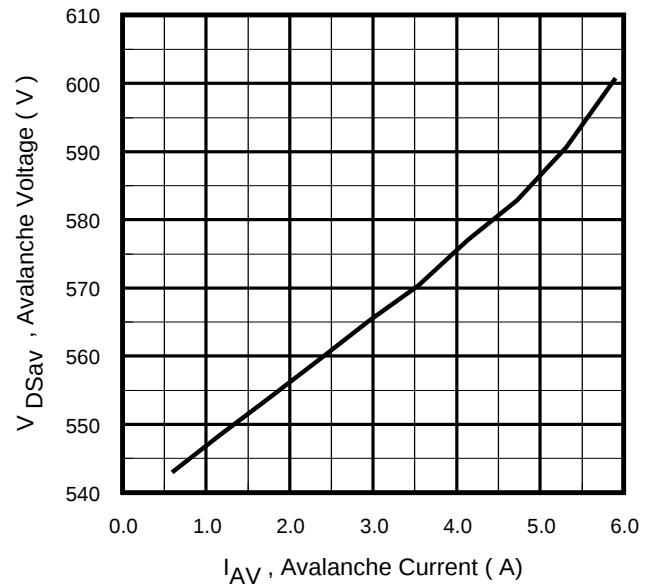
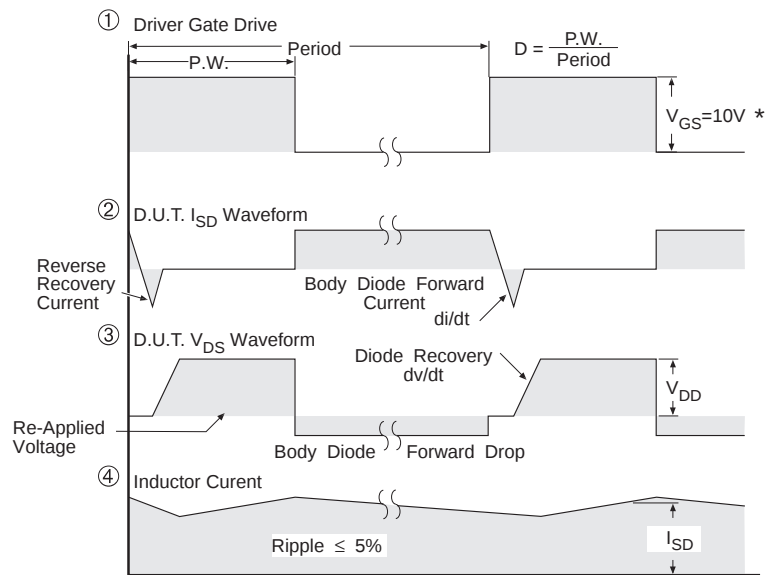
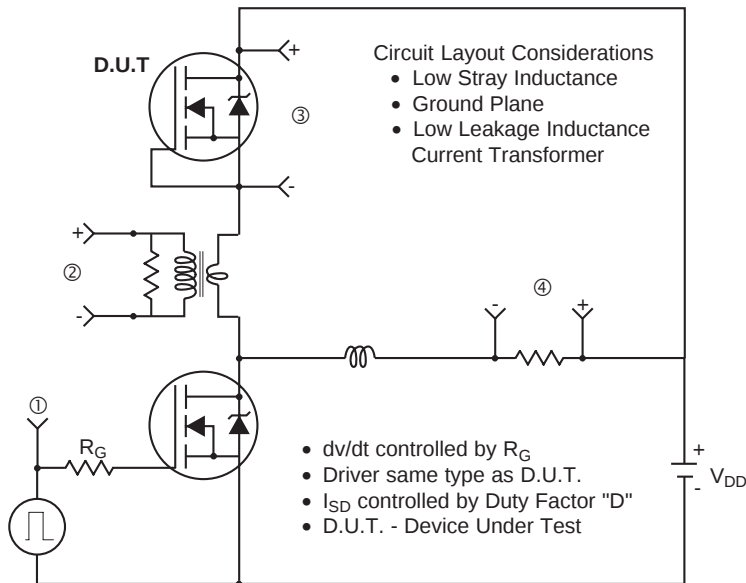


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



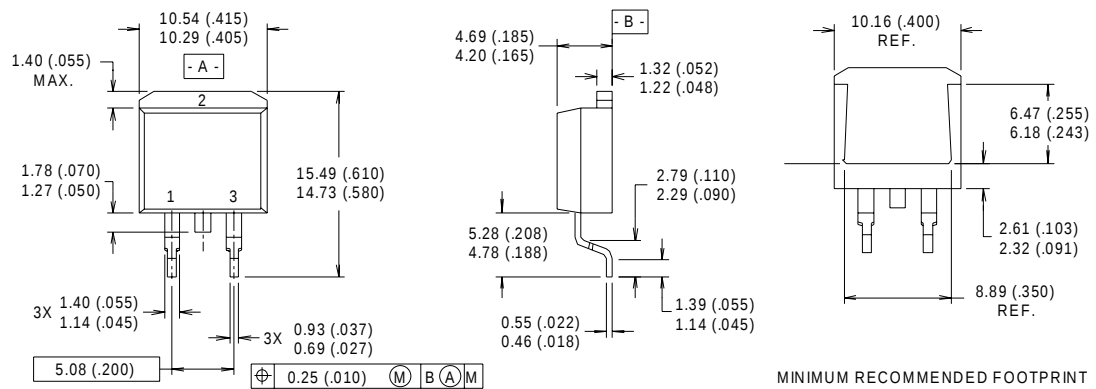
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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D²Pak Package Outline



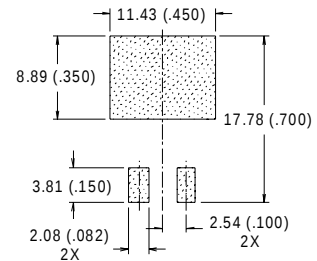
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

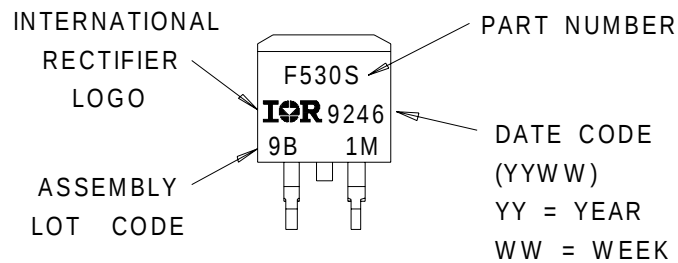
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



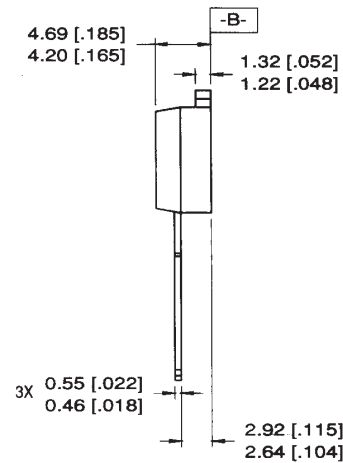
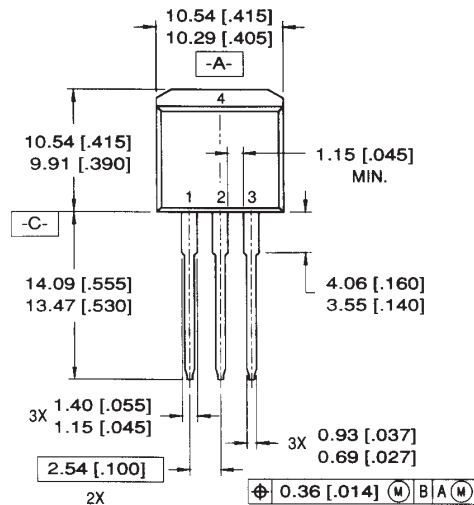
Part Marking Information

D²Pak



Package Outline

TO-262 Outline



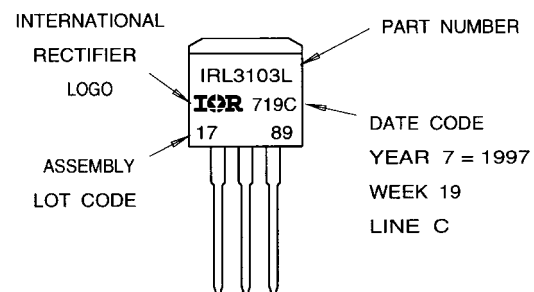
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

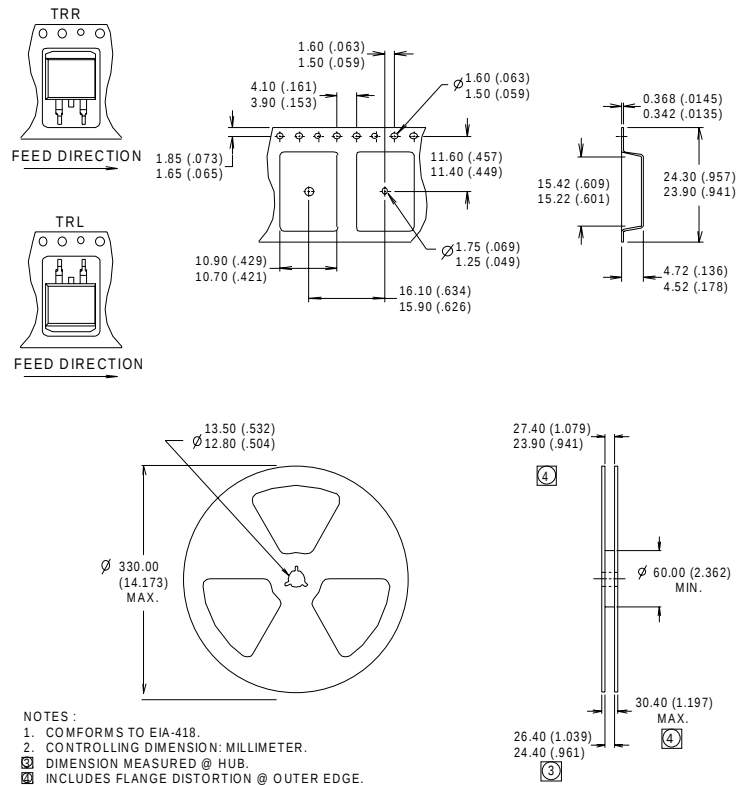


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Tape & Reel Information

D²Pak



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 - ② Starting $T_J = 25^\circ\text{C}$, $L = 19\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 5.5\text{A}$. (See Figure 12)
 - ③ $I_{SD} \leq 5.5\text{A}$, $di/dt \leq 90\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
 - ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 - ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
 - ⑥ Uses IRF730A data and test conditions
- * When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

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IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
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Data and specifications subject to change without notice. 5/00