

IS41C8512 IS41LV8512



512K x 8 (4-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

FEATURES

- Extended Data-Out (EDO) Page Mode access cycle
- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval: 1024 cycles /16 ms
- Refresh Mode: $\overline{\text{RAS}}$ -Only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR), Hidden
- JEDEC standard pinout
- Single power supply:
 - 5V $\pm$ 10% (IS41C8512)
 - 3.3V $\pm$ 10% (IS41LV8512)
- Byte Write and Byte Read operation via $\overline{\text{CAS}}$
- Industrial Temperature Range -40°C to 85°C

DESCRIPTION

The *ICSI* IS41C8512 and IS41LV8512 is a 524,288 x 8-bit high-performance CMOS Dynamic Random Access Memories. The IS41C8512 offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 512 random accesses within a single row with access cycle time as short as 10 ns per 8-bit.

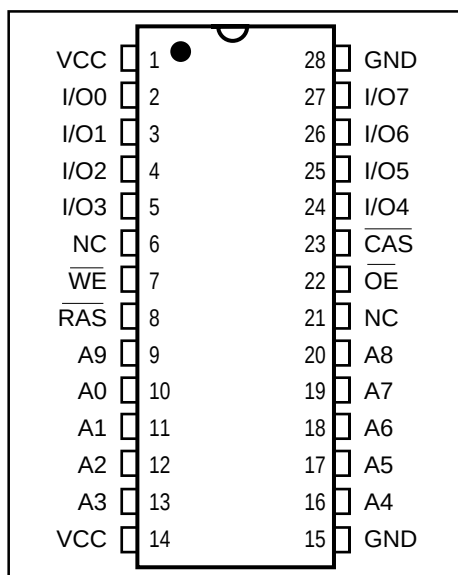
These features make the IS41C8512 and IS41LV8512 ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS41C8512 is packaged in a 28-pin 400mil SOJ and 400mil TSOP-2.

KEY TIMING PARAMETERS

Parameter	-35	-50	-60	Unit
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	35	50	60	ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	10	14	15	ns
Max. Column Address Access Time (t_{AA})	18	25	30	ns
Min. EDO Page Mode Cycle Time (t_{PC})	12	20	25	ns
Min. Read/Write Cycle Time (t_{RC})	60	90	110	ns

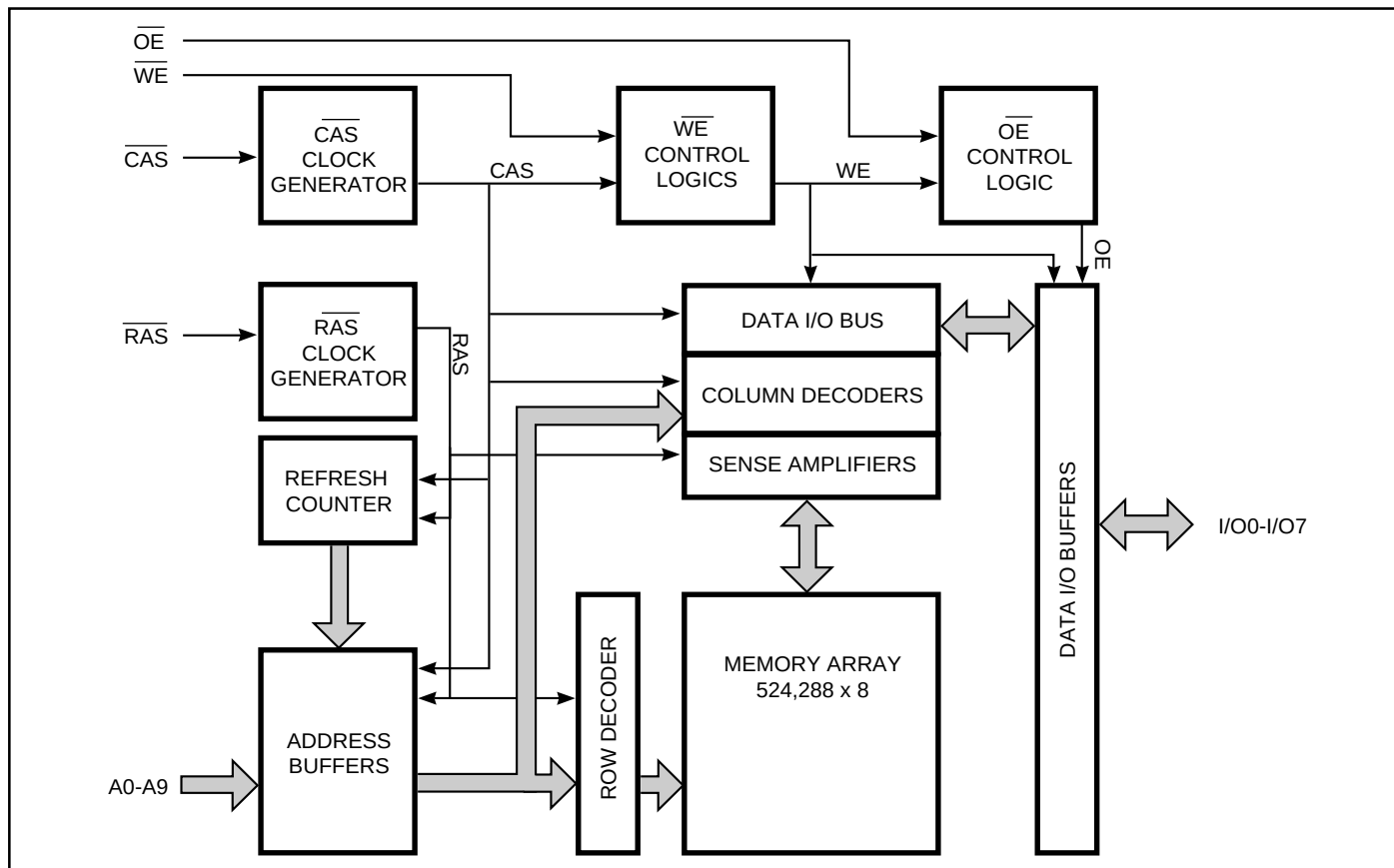
PIN CONFIGURATIONS 28 Pin SOJ, TSOP-2



PIN DESCRIPTIONS

A0-A9	Address Inputs
I/O0-7	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address t_R/t_C	I/O
Standby		H	H	X	X	X	High-Z
Read		L	L	H	L	ROW/COL	D _{OUT}
Write: Word (Early Write)		L	L	L	X	ROW/COL	D _{IN}
Read-Write		L	L	H→L	L→H	ROW/COL	D _{OUT} , D _{IN}
Hidden Refresh	Read	L→H→L	L	H	L	ROW/COL	D _{OUT}
	Write ⁽¹⁾	L→H→L	L	L	X	ROW/COL	D _{OUT}
$\overline{RAS}$ -Only Refresh		L	H	X	X	ROW/NA	High-Z
CBR Refresh		H→L	L	X	X	X	High-Z

Note:

1. EARLY WRITE only.

Functional Description

The IS41C8512 and IS41LV8512 is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 10 address bits. These are entered ten bits (A0-A9) at a time. The row address is latched by the Row Address Strobe ($\overline{\text{RAS}}$). The column address is latched by the Column Address Strobe ($\overline{\text{CAS}}$). $\overline{\text{RAS}}$ is used to latch the first ten bits and $\overline{\text{CAS}}$ is used the latter nine bits.

Memory Cycle

A memory cycle is initiated by bring $\overline{\text{RAS}}$ LOW and it is terminated by returning both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP} , t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{OE}}$, whichever occurs last, while holding $\overline{\text{WE}}$ HIGH. The column address must be held for a minimum time specified by t_{AR} . Data Out becomes valid only when t_{RAC} , t_{AA} , t_{CAC} and t_{OEa} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs first.

Refresh Cycle

To retain data, 1024 refresh cycles are required in each 16 ms period. There are two ways to refresh the memory.

1. By clocking each of the 1024 row addresses (A0 through A9) with $\overline{\text{RAS}}$ at least once every 16 ms. Any read, write, read-modify-write or $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is activated by the falling edge of $\overline{\text{RAS}}$, while holding $\overline{\text{CAS}}$ LOW. In $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle, an internal 10-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Extended Data Out Page Mode

EDO page mode operation permits all 512 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

In EDO page mode, due to the extended data function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one $\overline{\text{RAS}}$ cycle, but the performance is equivalent to that of the fast page mode in that case.

Power-On

After application of the V_{CC} supply, an initial pause of 200 μs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ signal).

During power-on, it is recommended that $\overline{\text{RAS}}$ track with V_{CC} or be held at a valid V_{IH} to avoid current surges.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameters		Rating	Unit
V _T	Voltage on Any Pin Relative to GND	5V	–1.0 to +7.0	V
		3.3V	–0.5 to +4.6	
V _{CC}	Supply Voltage	5V	–1.0 to +7.0	V
		3.3V	–0.5 to +4.6	
I _{OUT}	Output Current		50	mA
P _D	Power Dissipation		1	W
T _A	Commercial Operation Temperature		0 to +70	°C
	Industrial Operating Temperature		–40 to +85	°C
T _{STG}	Storage Temperature		–55 to +125	°C

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	
V _{IH}	Input High Voltage	5V	2.4	—	V _{CC} + 1.0	V
		3.3V	2.0	—	V _{CC} + 0.3	
V _{IL}	Input Low Voltage	5V	–1.0	—	0.8	V
		3.3V	–0.3	—	0.8	
T _A	Commercial Ambient Temperature		0	—	70	°C
	Industrial Ambient Temperature		–40	—	85	°C

CAPACITANCE^(1,2)

Symbol	Parameter	Max.	Unit
C _{IN1}	Input Capacitance: A0-A8	5	pF
C _{IN2}	Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	7	pF
C _{IO}	Data Input/Output Capacitance: I/O0-I/O15	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS⁽¹⁾

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit	
I _{IL}	Input Leakage Current	Any input 0V ≤ V _{IN} ≤ V _{CC} Other inputs not under test = 0V		−10	10	μA	
I _{IO}	Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ V _{OUT} ≤ V _{CC}		−10	10	μA	
V _{OH}	Output High Voltage Level	I _{OH} = −2.5 mA		2.4	—	V	
V _{OL}	Output Low Voltage Level	I _{OL} =+2.1mA		—	0.4	V	
I _{CC1}	Standby Current: TTL	$\overline{RAS}, \overline{CAS} \geq V_{IH}$	Commerical	5V	—	3	mA
			Industrial	5V	—	4	
			Commerical	3V	—	2	
			Industrial	3V	—	3	
I _{CC2}	Standby Current: CMOS	$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2V$	5V	—	2	mA	
			3V	—	1		
I _{CC3}	Operating Current: Random Read/Write ^(2,3,4) Average Power Supply Current	$\overline{RAS}, \overline{CAS}$, Address Cycling, t _{RC} = t _{RC} (min.)	-35	—	230	mA	
			-50	—	180		
			-60	—	170		
I _{CC4}	Operating Current: EDO Page Mode ^(2,3,4) Average Power Supply Current	$\overline{RAS} = V_{IL}, \overline{CAS}$, Cycling t _{PC} = t _{PC} (min.)	-35	—	220	mA	
			-50	—	170		
			-60	—	160		
I _{CC5}	Refresh Current: $\overline{RAS}$ -Only ^(2,3) Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH}$ t _{RC} = t _{RC} (min.)	-35	—	230	mA	
			-50	—	180		
			-60	—	170		
I _{CC6}	Refresh Current: CBR ^(2,3,5) Average Power Supply Current	$\overline{RAS}, \overline{CAS}$ Cycling t _{RC} = t _{RC} (min.)	-35	—	230	mA	
			-50	—	180		
			-60	—	170		

Notes:

1. An initial pause of 200 μs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS^(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35		-50		-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Random READ or WRITE Cycle Time	60	—	90	—	110	—	ns
t _{RAC}	Access Time from $\overline{\text{RAS}}$ ^(6, 7)	35	—	50	—	—	60	ns
t _{CAC}	Access Time from $\overline{\text{CAS}}$ ^(6, 8, 15)	—	10	—	14	—	15	ns
t _{AA}	Access Time from Column-Address ⁽⁶⁾	—	18	—	25	—	30	ns
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	35	10K	50	10K	60	10K	ns
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	20	—	30	—	40	—	ns
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width ⁽²⁶⁾	6	10K	8	10K	10	10K	ns
t _{CP}	$\overline{\text{CAS}}$ Precharge Time ^(9, 25)	5	—	8	—	10	—	ns
t _{CSH}	$\overline{\text{CAS}}$ Hold Time ⁽²¹⁾	35	—	50	—	60	—	ns
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time ^(10, 20)	11	28	19	36	20	45	ns
t _{ASR}	Row-Address Setup Time	0	—	0	—	0	—	ns
t _{RAH}	Row-Address Hold Time	6	—	8	—	10	—	ns
t _{ASC}	Column-Address Setup Time ⁽²⁰⁾	0	—	0	—	0	—	ns
t _{CAH}	Column-Address Hold Time ⁽²⁰⁾	6	—	8	—	10	—	ns
t _{AR}	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$)	30	—	40	—	40	—	ns
t _{RAD}	$\overline{\text{RAS}}$ to Column-Address Delay Time ⁽¹¹⁾	10	20	14	25	15	30	ns
t _{RAL}	Column-Address to $\overline{\text{RAS}}$ Lead Time	18	—	25	—	30	—	ns
t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	—	0	—	0	—	ns
t _{RSH}	$\overline{\text{RAS}}$ Hold Time ⁽²⁷⁾	8	—	14	—	15	—	ns
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z ^(15, 29)	3	—	3	—	3	—	ns
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time ⁽²¹⁾	5	—	5	—	5	—	ns
t _{OD}	Output Disable Time ^(19, 28, 29)	3	12	3	12	3	12	ns
t _{OE}	Output Enable Time ^(15, 16)	0	10	0	15	—	15	ns
t _{OEHC}	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	10	—	10	—	10	—	ns
t _{OEP}	$\overline{\text{OE}}$ HIGH Pulse Width	10	—	10	—	10	—	ns
t _{OES}	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	5	—	ns
t _{RCS}	Read Command Setup Time ^(17, 20)	0	—	0	—	0	—	ns
t _{RRH}	Read Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹²⁾	0	—	0	—	0	—	ns
t _{RCH}	Read Command Hold Time (referenced to $\overline{\text{CAS}}$) ^(12, 17, 21)	0	—	0	—	0	—	ns
t _{WCH}	Write Command Hold Time ^(17, 27)	5	—	8	—	10	—	ns
t _{WCR}	Write Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹⁷⁾	30	—	40	—	50	—	ns
t _{WP}	Write Command Pulse Width ⁽¹⁷⁾	5	—	8	—	10	—	ns
t _{WPZ}	$\overline{\text{WE}}$ Pulse Widths to Disable Outputs	10	—	10	—	10	—	ns
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time ⁽¹⁷⁾	8	—	14	—	15	—	ns
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time ^(17, 21)	8	—	14	—	15	—	ns
t _{WCS}	Write Command Setup Time ^(14, 17, 20)	0	—	0	—	0	—	ns
t _{DHR}	Data-in Hold Time (referenced to $\overline{\text{RAS}}$)	30	—	40	—	40	—	ns

AC CHARACTERISTICS (Continued)^(1,2,3,4,5,6)

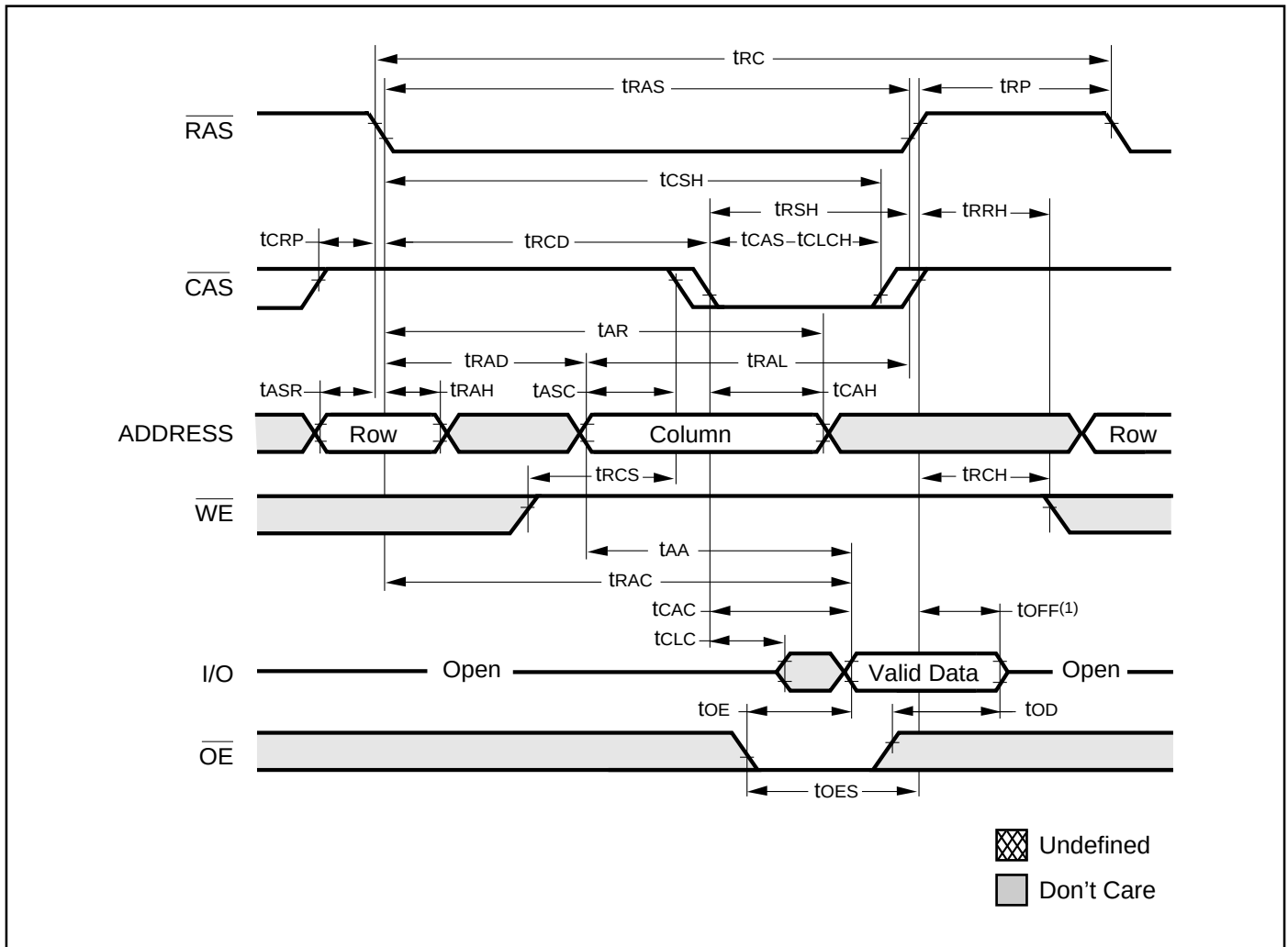
(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35		-50		-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACH}	Column-Address Setup Time to $\overline{\text{CAS}}$ Precharge during WRITE Cycle	15	—	15	—	15	—	ns
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle ⁽¹⁸⁾	8	—	8	—	15	—	ns
t _{DS}	Data-In Setup Time ^(15, 22)	0	—	0	—	0	—	ns
t _{DH}	Data-In Hold Time ^(15, 22)	6	—	6	—	10	—	ns
t _{RWC}	READ-MODIFY-WRITE Cycle Time	80	—	100	—	140	—	ns
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time during READ-MODIFY-WRITE Cycle ⁽¹⁴⁾	45	—	50	—	80	—	ns
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time ^(14, 20)	25	—	30	—	36	—	ns
t _{AWD}	Column-Address to $\overline{\text{WE}}$ Delay Time ⁽¹⁴⁾	30	—	30	—	49	—	ns
t _{PC}	EDO Page Mode READ or WRITE Cycle Time ⁽²⁴⁾	12	—	15	—	25	—	ns
t _{RASP}	$\overline{\text{RAS}}$ Pulse Width in EDO Page Mode	35	100K	40	100K	50	100K	ns
t _{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge ⁽¹⁵⁾	—	21	—	27	—	34	ns
t _{PRWC}	EDO Page Mode READ-WRITE Cycle Time ⁽²⁴⁾	40	—	45	—	56	—	ns
t _{COH}	Data Output Hold after $\overline{\text{CAS}}$ LOW	5	—	5	—	5	—	ns
t _{OFF}	Output Buffer Turn-Off Delay from $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$ ^(13,15,19, 29)	3	15	3	15	3	15	ns
t _{WHZ}	Output Disable Delay from $\overline{\text{WE}}$	3	15	3	15	3	15	ns
t _{CLCH}	Last $\overline{\text{CAS}}$ going LOW to First $\overline{\text{CAS}}$ returning HIGH ⁽²³⁾	10	—	10	—	10	—	ns
t _{CSR}	$\overline{\text{CAS}}$ Setup Time (CBR REFRESH) ^(30, 20)	8	—	10	—	10	—	ns
t _{CHR}	$\overline{\text{CAS}}$ Hold Time (CBR REFRESH) ^(30, 21)	8	—	10	—	10	—	ns
t _{ORD}	$\overline{\text{OE}}$ Setup Time prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH Cycle	0	—	0	—	0	—	ns
t _{REF}	Refresh Period (1024 Cycles)	—	16	16	—	16	—	ms
t _r	Transition Time (Rise or Fall) ^(2, 3)	1	50	1	50	1	50	ns

Notes:

1. An initial pause of 200 μ s is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{\text{CAS}}$ and $\overline{\text{RAS}} = V_{\text{IH}}$, data output is High-Z.
5. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX})$.
9. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ must be pulsed for t_{CP} .
10. Operation with the $t_{\text{RCD}} (\text{MAX})$ limit ensures that $t_{\text{RAC}} (\text{MAX})$ can be met. $t_{\text{RCD}} (\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}} (\text{MAX})$ limit, access time is controlled exclusively by t_{CAC} .
11. Operation within the $t_{\text{RAD}} (\text{MAX})$ limit ensures that $t_{\text{RCD}} (\text{MAX})$ can be met. $t_{\text{RAD}} (\text{MAX})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}} (\text{MAX})$ limit, access time is controlled exclusively by t_{AA} .
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. $t_{\text{OFF}} (\text{MAX})$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
14. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN})$, the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{MIN})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{MIN})$ and $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{MIN})$, the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ or $\overline{\text{OE}}$ go back to V_{IH}) is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW result in a LATE WRITE ($\overline{\text{OE}}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{\text{CAS}}$ input.
16. During a READ cycle, if $\overline{\text{OE}}$ is LOW then taken HIGH before $\overline{\text{CAS}}$ goes HIGH, I/O goes open. If $\overline{\text{OE}}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{\text{WE}}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. The first $\chi\overline{\text{CAS}}$ edge to transition LOW.
21. The last $\chi\overline{\text{CAS}}$ edge to transition HIGH.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling $\chi\overline{\text{CAS}}$ edge to first rising $\chi\overline{\text{CAS}}$ edge.
24. Last rising $\chi\overline{\text{CAS}}$ edge to next cycle's last rising $\chi\overline{\text{CAS}}$ edge.
25. Last rising $\chi\overline{\text{CAS}}$ edge to first falling $\chi\overline{\text{CAS}}$ edge.
26. Each $\chi\overline{\text{CAS}}$ must meet minimum pulse width.
27. Last $\chi\overline{\text{CAS}}$ to go LOW.
28. I/Os controlled, regardless $\overline{\text{CAS}}$.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

READ CYCLE

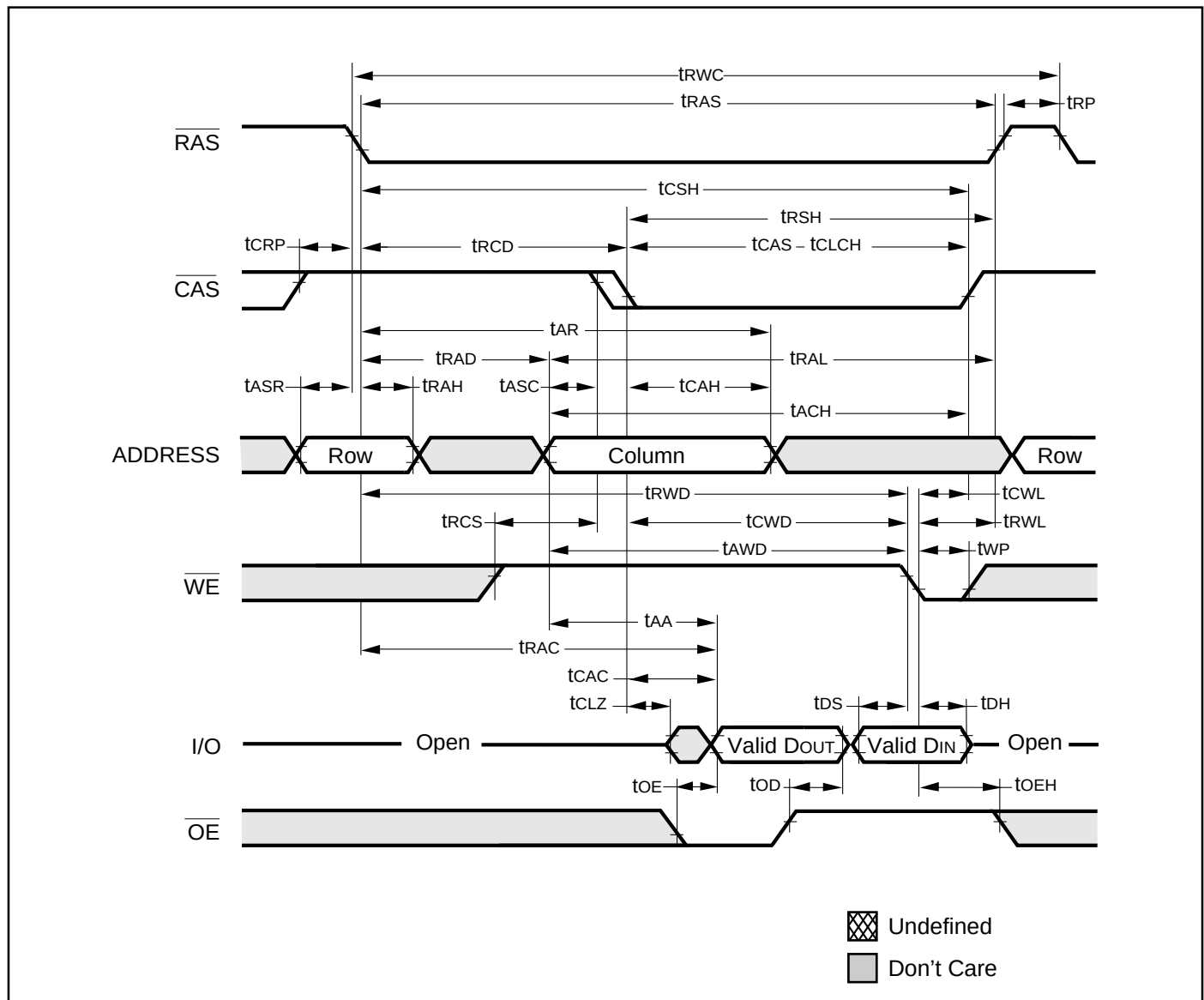


Note:

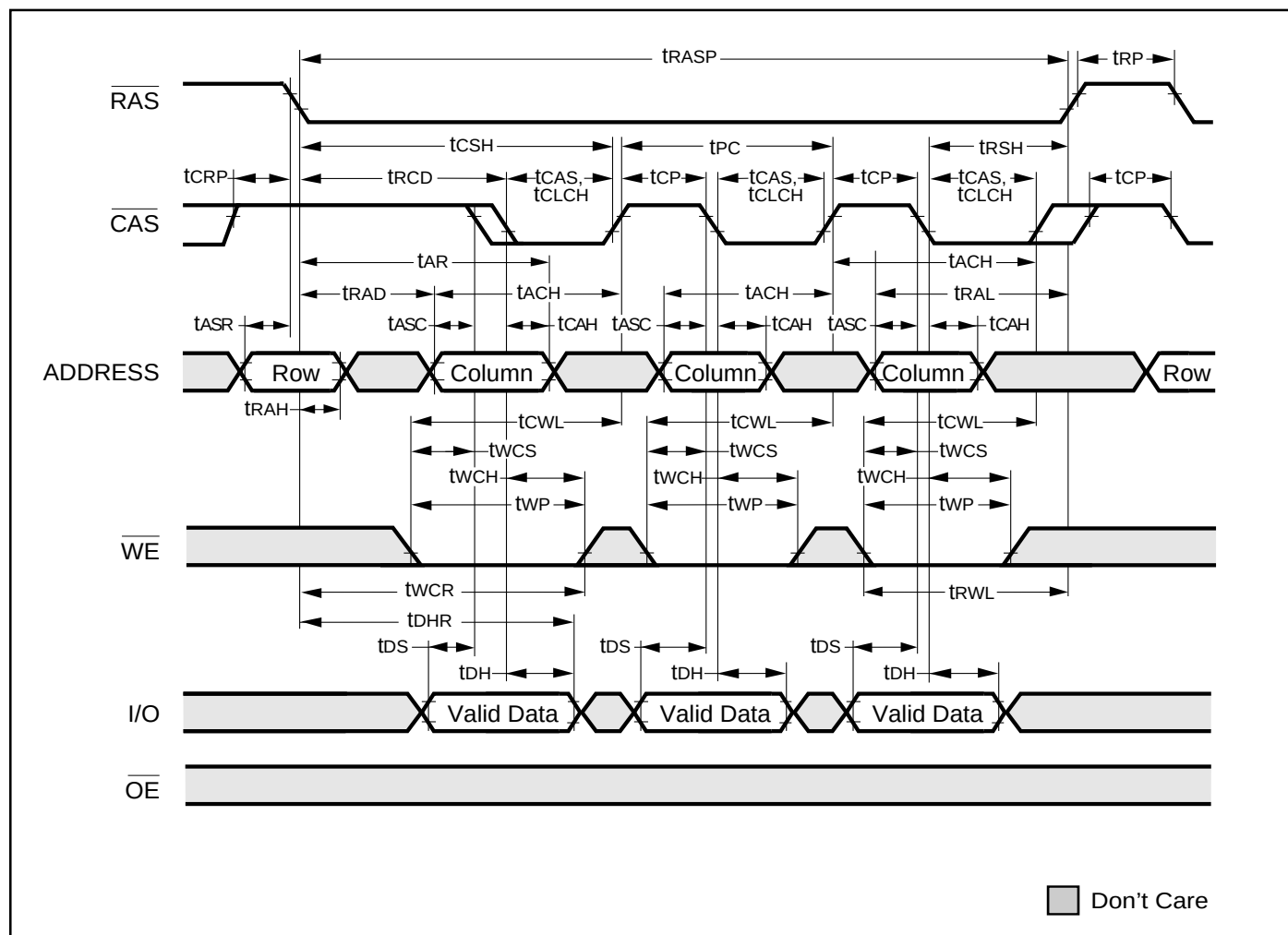
1. t_{OFF} is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

The diagram illustrates the timing relationships for a 2D DRAM array. It shows the signals $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, ADDRESS, $\overline{\text{WE}}$, and I/O. The ADDRESS signal is divided into Row and Column phases. The I/O signal is labeled as Valid Data. Various timing parameters are indicated by arrows, including t_{RC} , t_{RAS} , t_{RCD} , t_{CAS} , t_{RSH} , t_{CSH} , t_{TRP} , t_{CRP} , $t_{\text{CAS}} - t_{\text{CLCH}}$, t_{AR} , t_{RAD} , t_{TRAL} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{ACH} , t_{CWL} , t_{RWL} , t_{WCR} , t_{WCS} , t_{WCH} , t_{WP} , t_{DHR} , t_{DS} , and t_{DH} . A legend indicates that gray shaded areas represent 'Don't Care' states.

READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



EDO-PAGE-MODE EARLY-WRITE CYCLE



The diagram illustrates the timing relationships for a 32Kbit 1T1R DRAM. It shows the signals $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, ADDRESS, $\overline{\text{WE}}$, I/O, and $\overline{\text{OE}}$ over time. The ADDRESS signal is divided into Row and Column phases. The I/O signal shows data output (Dout) and data input (Din) during the Column phases. Various timing parameters are indicated by arrows, such as t_{RASP} (RAS pulse width), t_{CRP} (CAS-to-RAS precharge), t_{RCD} (RAS-to-CAS delay), t_{CAS} (CAS pulse width), t_{CLCH} (column-to-column delay), t_{CP} (column precharge), t_{CAH} (column access time), t_{ASC} (address-to-column delay), t_{RAH} (row access time), t_{RAD} (row address delay), t_{ASR} (address-to-row delay), t_{AR} (row precharge), t_{RWD} (row write delay), t_{RCS} (row-to-column delay), t_{AWD} (address-to-write delay), t_{CWD} (column-to-write delay), t_{AA} (address-to-access time), t_{CPA} (column precharge to access time), t_{DH} (data hold time), t_{DS} (data setup time), t_{CAC} (column access time), t_{CLZ} (column-to-column delay), t_{OE} (output enable delay), t_{OD} (output delay), t_{OEH} (output enable hold time), t_{RP} (RAS precharge), t_{PC} (precharge), t_{PRWC} (precharge to row-to-column delay), t_{TRSH} (trailing-to-row delay), t_{TCP} (trailing-to-column precharge), t_{TCAH} (trailing-to-column access time), t_{TASC} (trailing-to-address delay), t_{TRAL} (trailing-to-row access time), t_{TRWL} (trailing-to-row delay), t_{TCWL} (trailing-to-column delay), t_{TWP} (trailing-to-write precharge), t_{TOD} (trailing-to-output delay), and t_{TOEH} (trailing-to-output enable hold time).

Legend:

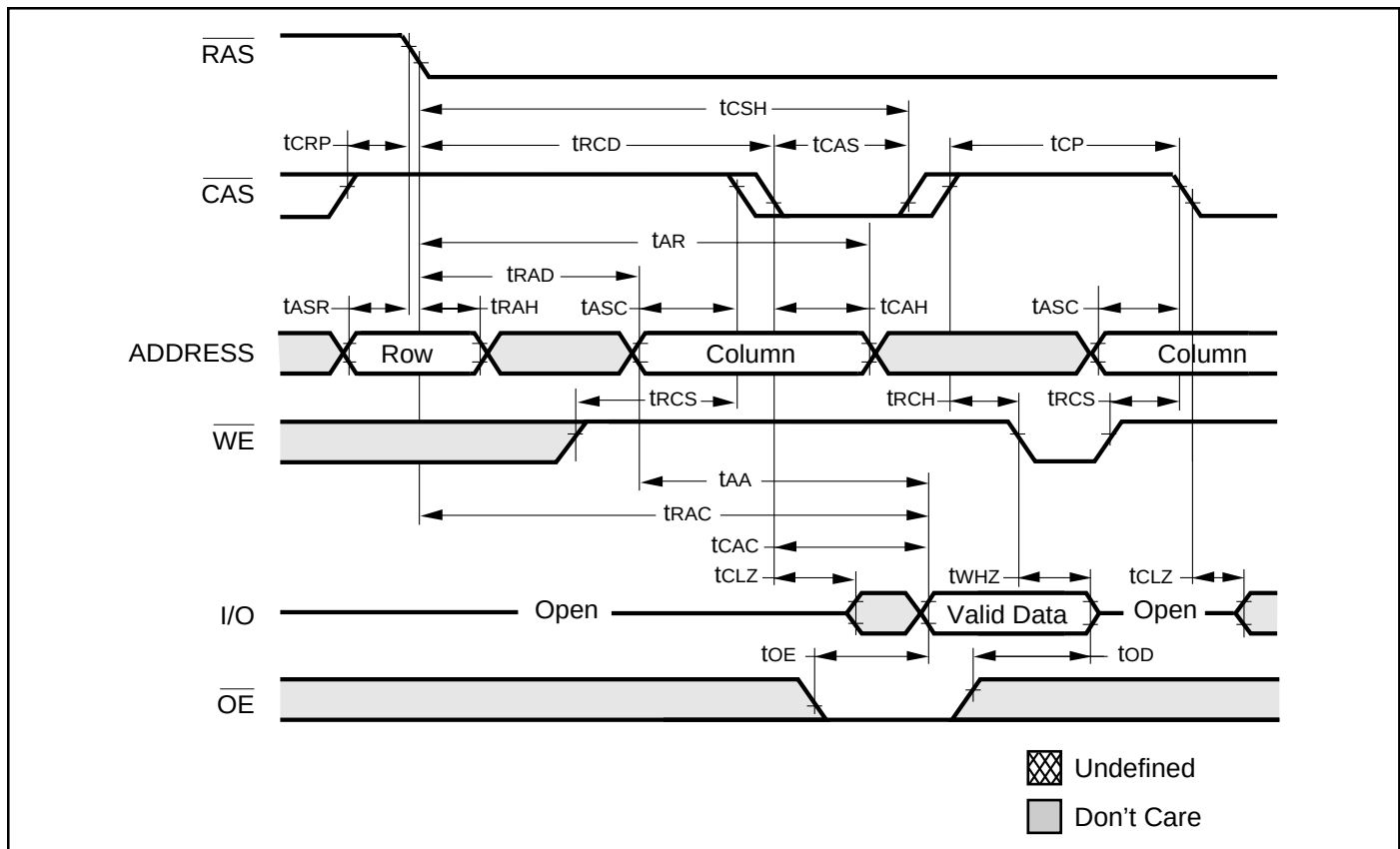
- Undefined (hatched box)
- Don't Care (gray box)

Integrated Circuit Solution Inc.
DR008-0B

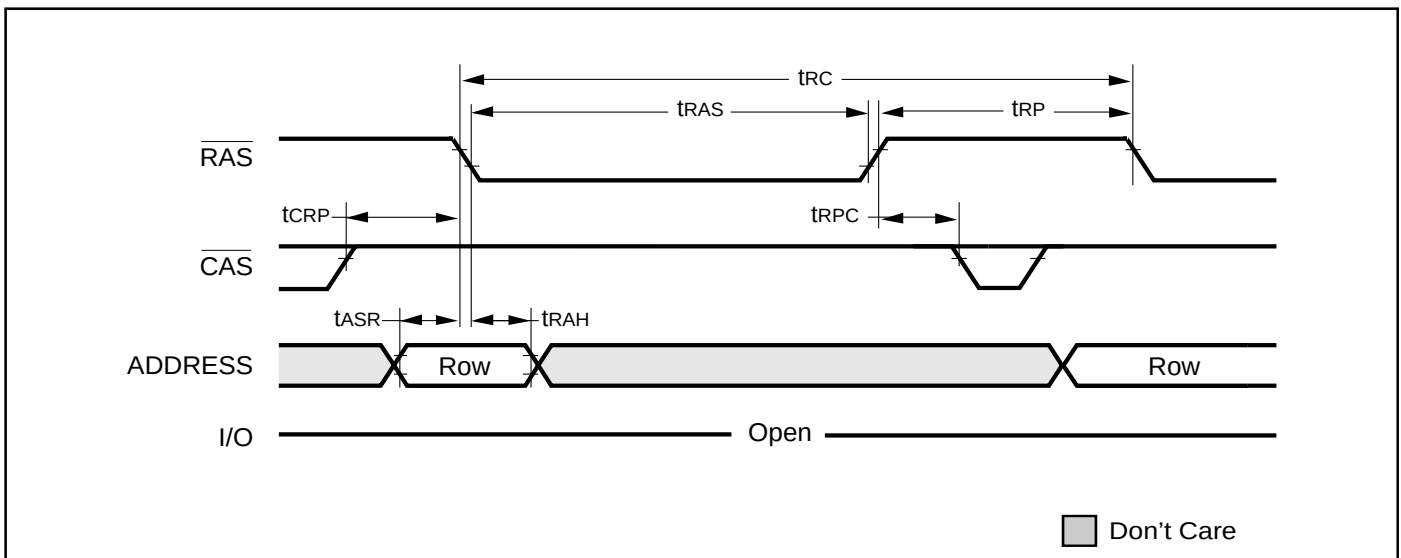
[illegible]

AC WAVEFORMS

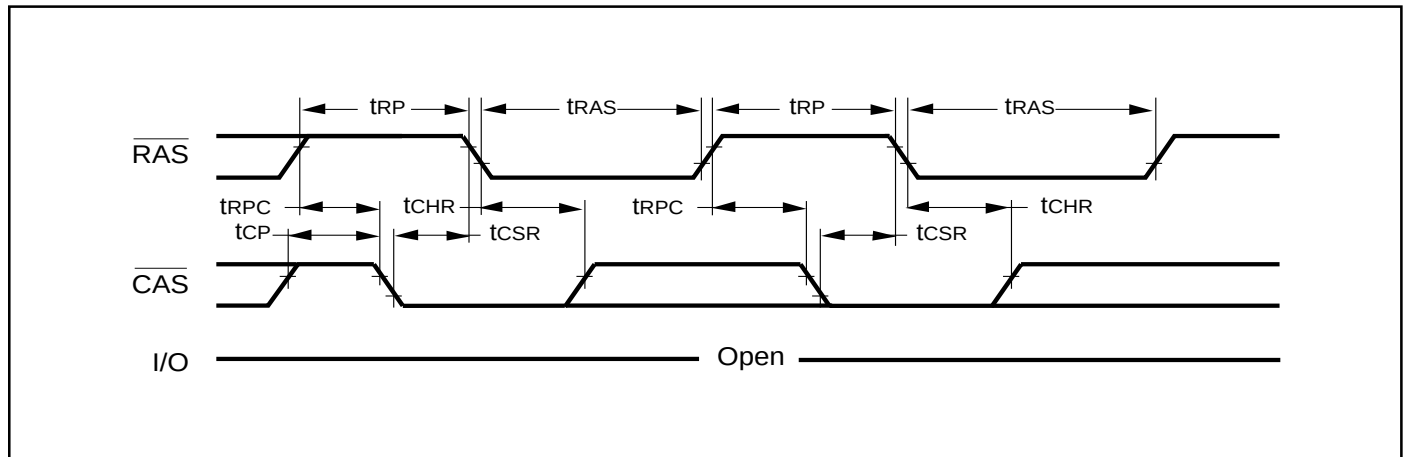
READ CYCLE (With $\overline{WE}$ -Controlled Disable)



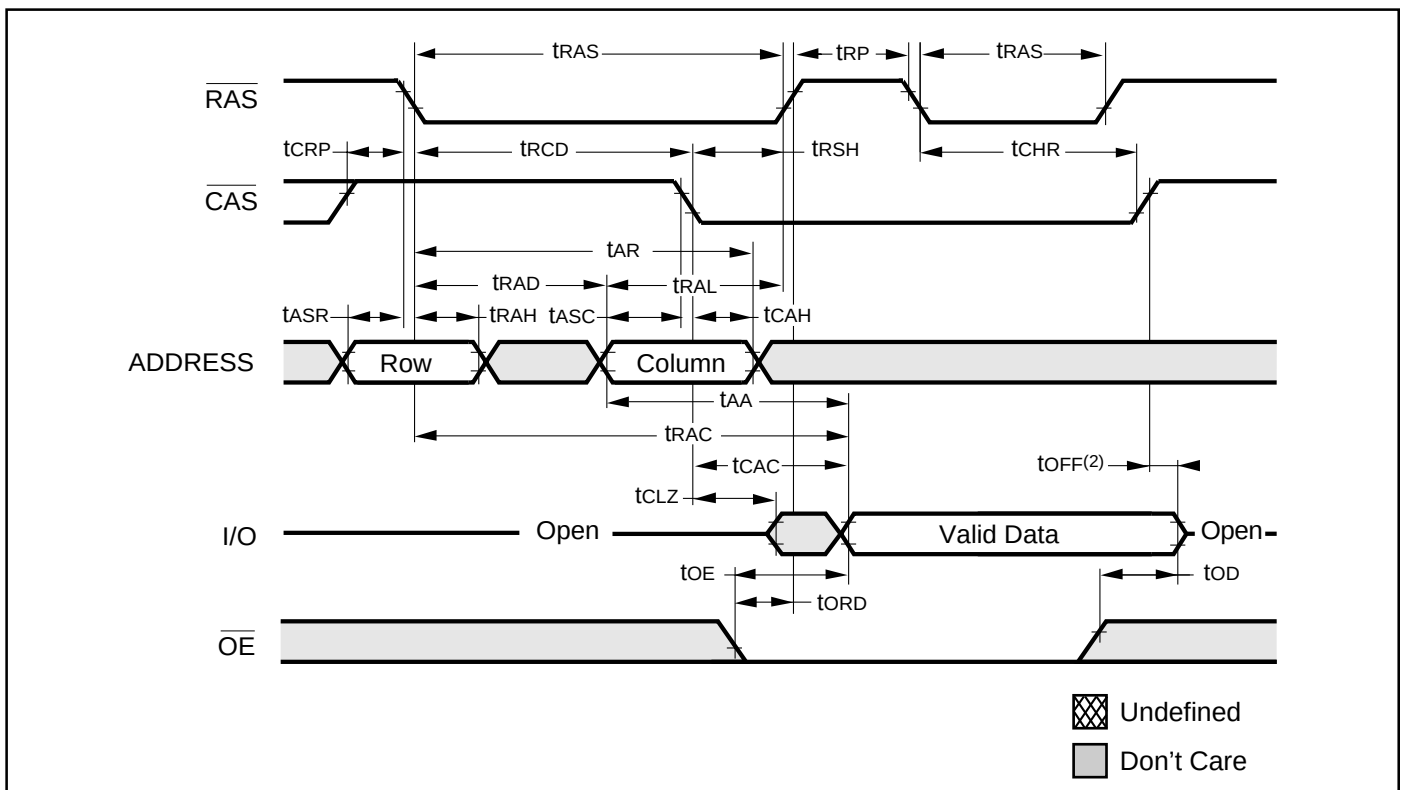
$\overline{RAS}$ -ONLY REFRESH CYCLE ($\overline{OE}$, $\overline{WE}$ = DON'T CARE)



$\overline{\text{CBR}}$ REFRESH CYCLE (Addresses; $\overline{\text{WE}}$, $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE⁽¹⁾ ($\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)



Notes:

1. A Hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
2. t_{OFF} is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

ORDERING INFORMATION

IS41C8512

Commercial Range: 0°C to 70°C

Speed (ns)	Order Part No.	Package
35	IS41C8512-35K	400mil SOJ
	IS41C8512-35T	400mil TSOP-2
50	IS41C8512-50K	400mil SOJ
	IS41C8512-50T	400mil TSOP-2
60	IS41C8512-60K	400mil SOJ
	IS41C8512-60T	400mil TSOP-2

ORDERING INFORMATION:

IS41LV8512

Commercial Range: 0°C to 70°C

Speed (ns)	Order Part No.	Package
35	IS41LV8512-35K	400mil SOJ
	IS41LV8512-35T	400mil TSOP-2
50	IS41LV8512-50K	400mil SOJ
	IS41LV8512-50T	400mil TSOP-2
60	IS41LV8512-60K	400mil SOJ
	IS41LV8512-60T	400mil TSOP-2

Industrial Range: -40°C to 85°C

Speed (ns)	Order Part No.	Package
35	IS41C8512-35KI	400mil SOJ
	IS41C8512-35TI	400mil TSOP-2
50	IS41C8512-50KI	400mil SOJ
	IS41C8512-50TI	400mil TSOP-2
60	IS41C8512-60KI	400mil SOJ
	IS41C8512-60TI	400mil TSOP-2

Industrial Range: -40°C to 85°C

Speed (ns)	Order Part No.	Package
35	IS41LV8512-35K	400mil SOJ
	IS41LV8512-35T	400mil TSOP-2
50	IS41LV8512-50KI	400mil SOJ
	IS41LV8512-50TI	400mil TSOP-2
60	IS41LV8512-60KI	400mil SOJ
	IS41LV8512-60TI	400mil TSOP-2



Integrated Circuit Solution Inc.

HEADQUARTER:

NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.

TEL: 886-3-5780333

Fax: 886-3-5783000

BRANCH OFFICE:

7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.

TEL: 886-2-26962140

FAX: 886-2-26962252

<http://www.icsi.com.tw>