

KK74HC4053A

Analog Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

The KK74HC4053A utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

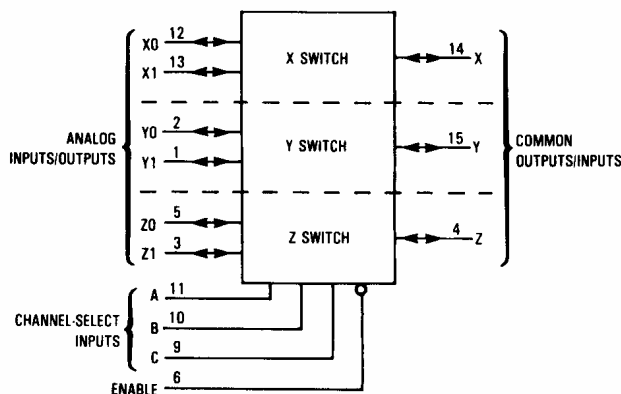
The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

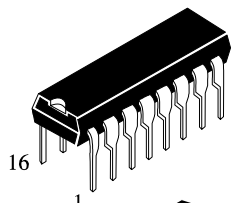
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC}-V_{EE}$)=2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC}-GND$)=2.0 to 6.0 V
- Low Noise

LOGIC DIAGRAM

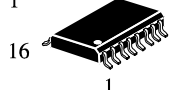
Triple Single-Pole, Double-Position
Plus Common Off



PIN 16 = V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND



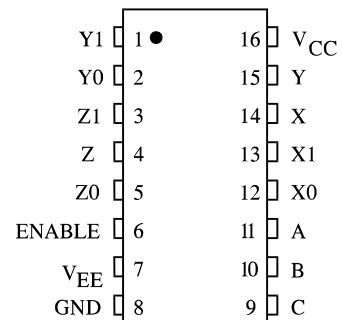
N SUFFIX
PLASTIC



DW SUFFIX
SOIC

ORDERING INFORMATION
 KK74HC4053AN Plastic
 KK74HC4053ADW SOIC
 $T_A = -55^\circ$ to 125° C for all packages

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs				ON Channels		
Enable	Select					
	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	None		

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	-0.5 to +7.0 -0.5 to +14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +0.5	V
V_{IS}	Analog Input Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
V_{IN}	Digital Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
I	DC Input Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Positive Supply Voltage (Referenced to GND) (Referenced to V _{EE})	2.0 2.0	6.0 12.0	V	
V _{EE}	Negative DC Supply Voltage (Referenced to GND)	- 6.0	GND	V	
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V	
V _{IN}	Digital Input Voltage (Referenced to GND)	GND	V _{CC}	V	
V _{IO} [*]	Static or Dynamic Voltage Across Switch	-	1.2	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Channel Select or Enable Inputs)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 0 0	1000 500 400	ns

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i. e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range indicated in the Recommended Operating Conditions..

Unused digital input pins must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) $V_{EE}=GND$,
Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{ON} = \text{Per Spec}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs	$R_{ON} = \text{Per Spec}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I_{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{IN}=V_{CC}$ or GND, $V_{EE}=-6.0$ V	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND Enable = V_{CC} or GND $V_{IS} = V_{CC}$ or GND $V_{IO}= 0$ V $V_{EE} = GND$ $V_{EE} = -6.0$	6.0 6.0	2 8	20 80	40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					25 °C to -55°C	≤85 °C	≤125 °C	
R_{ON}	Maximum “ON” Resistance	$V_{IN}=V_{IL}$ or V_{IH}	4.5	0.0	190	240	280	Ω
		$V_{IS} = V_{CC}$ or V_{EE}	4.5	-4.5	120	150	170	
		$I_S \leq 2.0$ mA(Figure 1)	6.0	-6.0	100	125	140	
		$V_{IN}=V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq 2.0$ mA(Figure 1)	4.5 4.5 6.0	0.0 -4.5 -6.0	150 100 80	190 125 100	230 140 115	
ΔR_{ON}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	$V_{IN}=V_{IL}$ or V_{IH}	4.5	0.0	30	35	40	Ω
		$V_{IS} = 1/2 (V_{CC}- V_{EE})$	4.5	-4.5	12	15	18	
		$I_S \leq 2.0$ mA	6.0	-6.0	10	12	14	
I_{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	$V_{IN}=V_{IL}$ or V_{IH} $V_{IO} = V_{CC}- V_{EE}$ Switch Off (Figure 2)	6.0	-6.0	0.1	0.5	1.0	μA
	Maximum Off- Channel Leakage Current, Common Channel	$V_{IN}=V_{IL}$ or V_{IH} $V_{IO}= V_{CC}- V_{EE}$ Switch Off (Figure 3)	6.0	-6.0	0.1	1.0	2.0	
I_{ON}	Maximum On- Channel Leakage Current, Channel to Channel	$V_{IN}=V_{IL}$ or V_{IH} Switch to Switch = $V_{CC}- V_{EE}$ (Figure 5)	6.0	-6.0	0.1	1.0	2.0	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter		V _{CC}	Guaranteed Limit			Unit
			V	25 °C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figures 8 and 9)		2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay , Analog Input to Analog Output (Figures 10 and 11)		2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay , Enable to Analog Output (Figures 12 and 13)		2.0 4.5 6.0	290 58 49	364 73 62	430 86 73	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay , Enable to Analog Output (Figures 12 and 13)		2.0 4.5 6.0	345 69 59	435 87 74	515 103 87	ns
C _{IN}	Maximum Input Capacitance, Channel-Select or Enable Inputs		-	10	10	10	pF
C _{I/O}	Maximum Capacitance Analog I/O Common O/I Feedthrough	All Switches Off	-	35	35	35	pF
			-	50	50	50	
			-	1.0	1.0	1.0	

C _{PD}	Power Dissipation Capacitance (Per Package) (Figure 15)	Typical @25°C,V _{CC} =5.0 V, V _{EE} =0 V	pF
	Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}	45	

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Limit*	Unit
					25 °C	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f _{in} =1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads -3 dB R _L =50 Ω, C _L =10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	120 120 120	MHz
-	Off-Channel Feedthrough Isolation (Figure 6)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L =600 Ω, C _L =50 pF f _{in} = 1.0 MHz, R _L =50 Ω, C _L =10 pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-50 -50 -50 -40 -40 -40	dB
-	Feedthrough Noise, Channel Select Input to Common O/I (Figure 7)	V _{IN} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A Enable = GND R _L =600 Ω, C _L =50 pF R _L =10 Ω, C _L =10 pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	25 105 135 35 145 190	mVpp
-	Crosstalk Between Any Two Switches (Figure 14)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L =600 Ω, C _L =50 pF f _{in} = 1 MHz, R _L =50 Ω, C _L =10 pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-50 -50 -50 -60 -60 -60	dB
THD	Total Harmonic Distortion (Figure 16)	f _{in} = 1 kHz, R _L =10 kΩ, C _L =50 pF THD = THD _{Measured} - THD _{Source} V _{IS} =4.0 V _{pp} sine wave V _{IS} =8.0 V _{pp} sine wave V _{IS} =11.0 V _{pp} sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.08 0.05	%

* Limits not tested. Determined by design and verified by qualification.

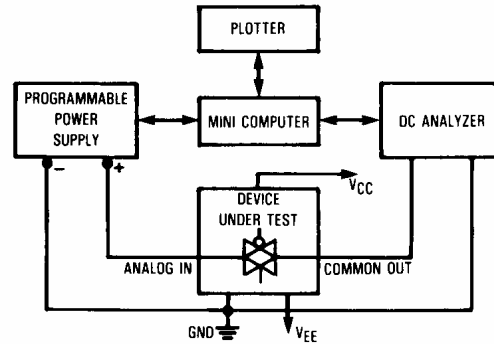


Figure 1. On Resistance Test Set-Up

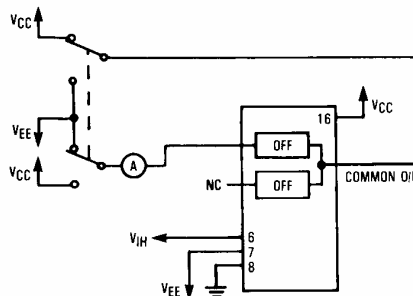


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

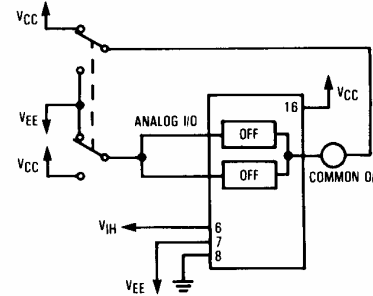


Figure 3. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

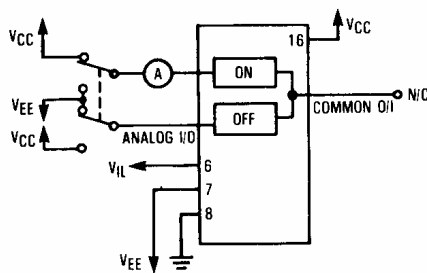
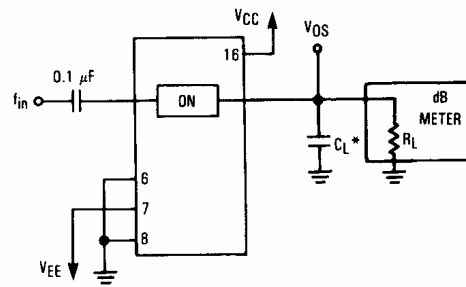
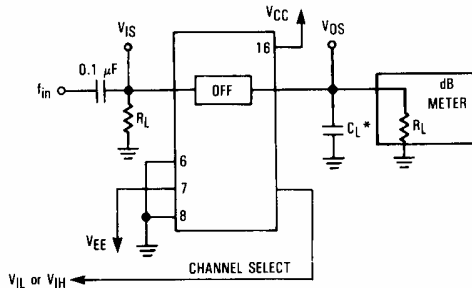


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



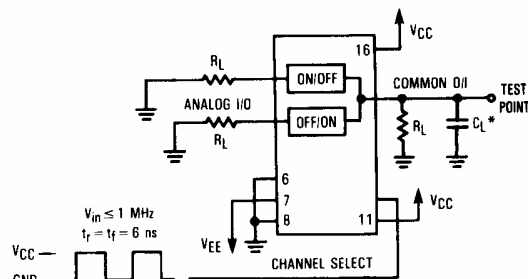
* Includes all probe and jig capacitance.

Figure 5. Maximum On Channel Bandwidth, Test Set-Up



* Includes all probe and jig capacitance.

Figure 6. Off Channel Feedthrough Isolation, Test Set-Up



* Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

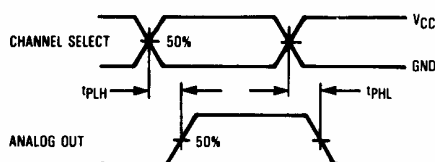
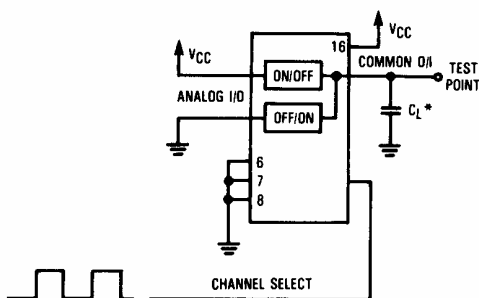


Figure 8. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 9. Test Set-Up, Channel Select to Analog Out

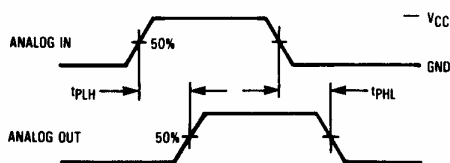
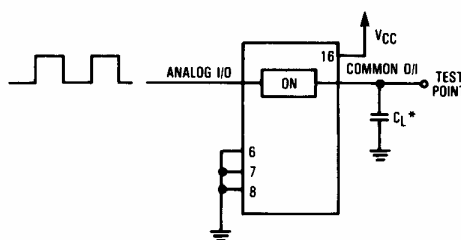


Figure 10. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 11. Test Set-Up, Analog In to Analog Out

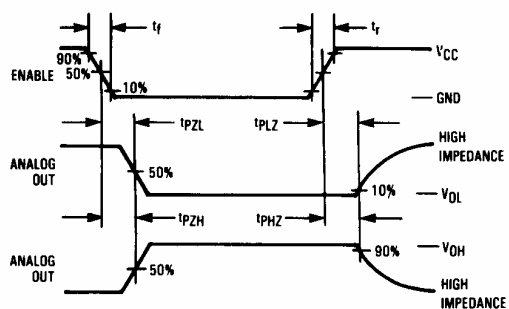


Figure 12. Switching Waveforms

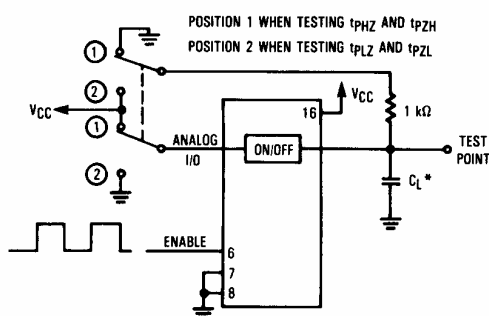
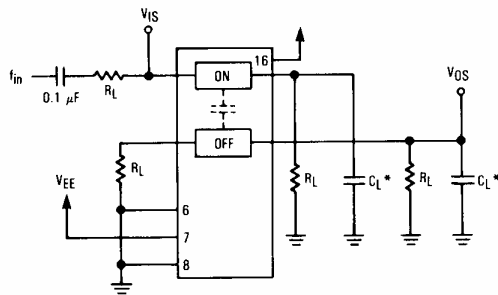


Figure 13. Test Set-Up, Enable to Analog Out



* Includes all probe and jig capacitance.

Figure 14. Crosstalk Between Any Two Switches, Test Set-Up_p

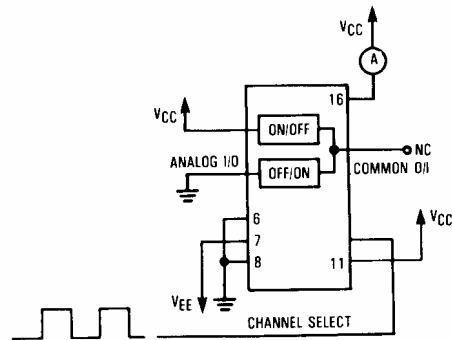


Figure 15. Power Dissipation Capacitance, Test Set-Up_p

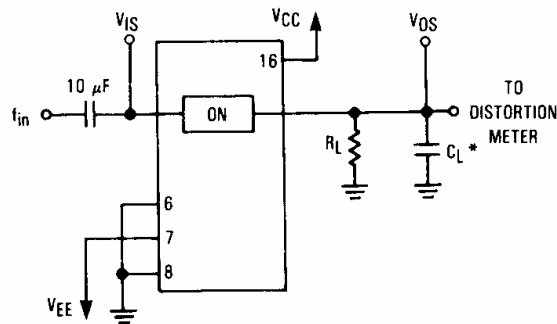
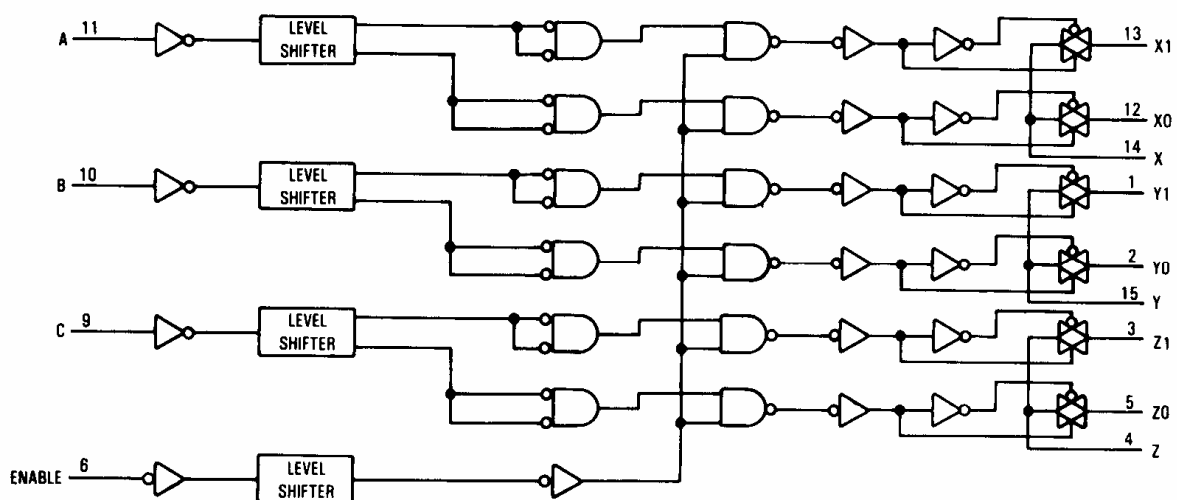
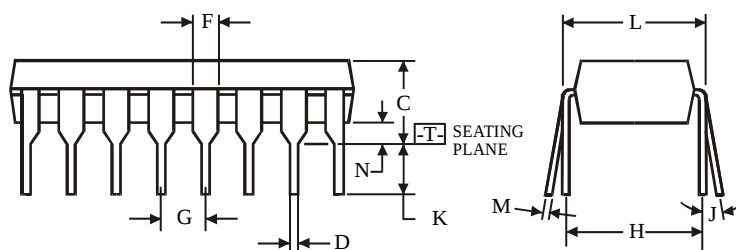
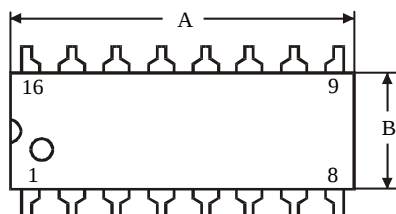
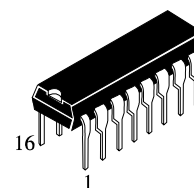


Figure 16. Total Harmonic Distortion, Test Set-Up_p

EXPANDED LOGIC DIAGRAM



N SUFFIX PLASTIC DIP (MS - 001BB)



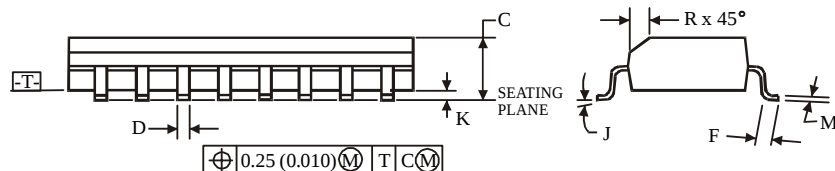
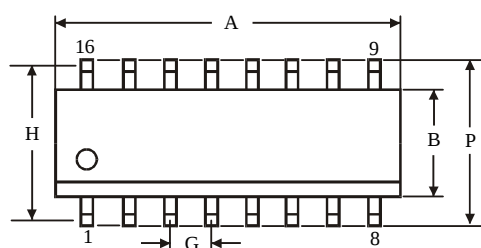
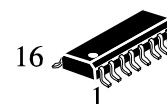
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Dimension, mm		
Symbol	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

D SUFFIX SOIC (MS - 012AC)



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side
for A; for B - 0.25 mm (0.010) per side.

Dimension, mm		
Symbol	MIN	MAX
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5