

Features

- Pin- and function-compatible with CY7C1020CV33
- Temperature Ranges
 - Commercial: 0 °C to 70 °C
 - Industrial: -40 °C to 85 °C
 - Automotive: -40 °C to 125 °C
- High speed
 - $t_{AA} = 10$ ns
- CMOS for optimum speed/power
- Low active power
 - 325 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II package

Functional Description

The CY7C1020CV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

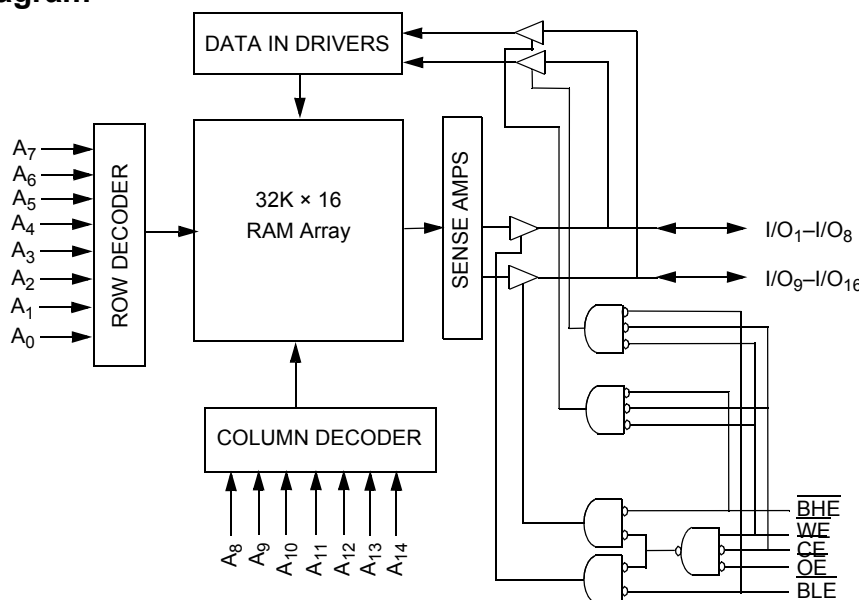
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₁ through I/O₈), is written into the location specified on the address pins (A₀ through A₁₄). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₄).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₁ to I/O₈. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₉ to I/O₁₆. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₁ through I/O₁₆) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ($\overline{CE}$ LOW, and WE LOW).

The CY7C1020CV33 is available in standard 44-pin TSOP Type II package.

Logic Block Diagram



Contents

Selection Guide	3	Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)	8
Pin Configuration	3	Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)	9
Pin Definitions	4	Truth Table	9
Maximum Ratings	5	Ordering Information	10
Operating Range	5	Ordering Code Definitions	10
Electrical Characteristics	5	Package Diagrams	10
Capacitance	5	Acronyms	11
Thermal Resistance	5	Document Conventions	11
AC Test Loads and Waveforms	6	Units of Measure	11
Switching Characteristics	6	Document History Page	12
Switching Waveforms	7	Sales, Solutions, and Legal Information	13
Read Cycle No. 1	7	Worldwide Sales and Design Support	13
Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)	7	Products	13
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)	8	PSoC Solutions	13

Selection Guide

		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial/Industrial	90	85	80	mA
	Automotive	—	—	85	mA
Maximum CMOS Standby Current	Commercial/Industrial	5	5	5	mA
	Automotive	—	—	10	mA

Pin Configuration ^[1]

TSOP II
Top View

NC	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₁	7	38	I/O ₁₆
I/O ₂	8	37	I/O ₁₅
I/O ₃	9	36	I/O ₁₄
I/O ₄	10	35	I/O ₁₃
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₅	13	32	I/O ₁₂
I/O ₆	14	31	I/O ₁₁
I/O ₇	15	30	I/O ₁₀
I/O ₈	16	29	I/O ₉
WE	17	28	NC
A ₄	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Note

1. NC pins are not connected on the die.

Pin Definitions

Pin Name	TSOP - Pin Number	I/O Type	Description
A ₀ –A ₁₄	5, 4, 3, 2, 18, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19	Input	Address Inputs used to select one of the address locations.
I/O ₁ –I/O ₁₆	7-10, 13-16, 29-32, 35-38	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	1, 22, 23, 28	No Connect	No Connects. Not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	Input/Control	Byte Write Select Inputs, active LOW. $\overline{\text{BHE}}$ controls I/O ₁₆ –I/O ₉ , $\overline{\text{BLE}}$ controls I/O ₈ –I/O ₁ .
$\overline{\text{OE}}$	41	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply inputs to the device.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} to relative GND^[2] -0.5 V to +4.6 V

DC voltage applied to outputs in high Z State^[2] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage > 2001 V (per MIL-STD-883, method 3015)

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%
Industrial	-40 °C to +85 °C	3.3 V ± 10%
Automotive	-40 °C to +125 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = -4.0 mA		2.4	—	2.4	—	2.4	—	V
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 8.0 mA		—	0.4	—	0.4	—	0.4	V
V _{IH}	Input HIGH voltage			2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage ^[2]			-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	Commercial/ Industrial	-1	+1	-1	+1	-1	+1	μA
			Automotive	—	—	—	—	-20	+20	μA
I _{OZ}	Output leakage current	GND ≤ V _I ≤ V _{CC} , Output Disabled	Commercial/ Industrial	-1	+1	-1	+1	-1	+1	μA
			Automotive	—	—	—	—	-20	+20	μA
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Commercial/ Industrial	—	90	—	85	—	80	mA
			Automotive	—	—	—	—	—	85	mA
I _{SB1}	Automatic CE power-down current —TTL Inputs	Max V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Commercial/ Industrial	—	15	—	15	—	15	mA
			Automotive	—	—	—	—	—	20	mA
I _{SB2}	Automatic CE power-down current —CMOS inputs	Max V _{CC} , CE ≥ V _{CC} - 0.3 V, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	Commercial/ Industrial	—	5	—	5	—	5	mA
			Automotive	—	—	—	—	—	10	mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

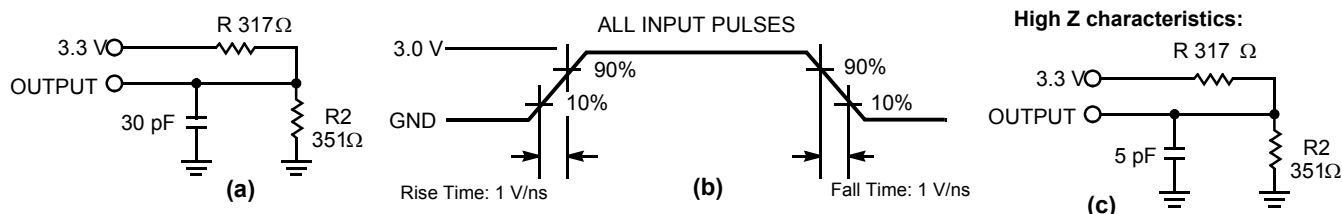
Thermal Resistance^[3]

Parameter	Description	Test Conditions	44-pin TSOP-II	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	76.92	°C/W
Θ_{JC}	Thermal resistance (Junction to Case)		15.86	°C/W

Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 0.5 \text{ V}$ for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[4]



Switching Characteristics

Over the Operating Range^[4]

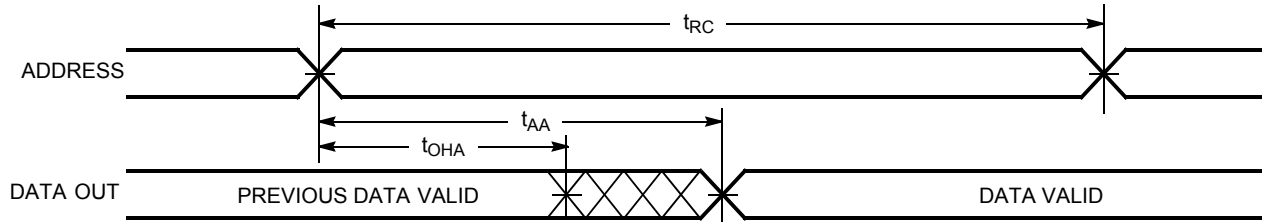
Parameter	Description	−10		−12		−15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t _{RC}	Read cycle time	10	–	12	–	15	–	ns
t _{AA}	Address to data valid	–	10	–	12	–	15	ns
t _{OHA}	Data hold from address change	3	–	3	–	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	10	–	12	–	15	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	5	–	6	–	7	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to low Z ^[5]	0	–	0	–	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to high Z ^[5, 6]	–	5	–	6	–	7	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to low Z ^[5]	3	–	3	–	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to high Z ^[5, 6]	–	5	–	6	–	7	ns
t _{PU} ^[7]	$\overline{\text{CE}}$ LOW to power-up	0	–	0	–	0	–	ns
t _{PD} ^[7]	$\overline{\text{CE}}$ HIGH to power-down	–	10	–	12	–	15	ns
t _{DBE}	Byte enable to data valid	–	5	–	6	–	7	ns
t _{LZBE}	Byte enable to low Z	0	–	0	–	0	–	ns
t _{HZBE}	Byte disable to high Z	–	5	–	6	–	7	ns
Write Cycle ^[8]								
t _{WC}	Write cycle time	10	–	12	–	15	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	8	–	9	–	10	–	ns
t _{AW}	Address set-up to write end	7	–	8	–	10	–	ns
t _{HA}	Address hold from write end	0	–	0	–	0	–	ns
t _{SA}	Address set-up to write start	0	–	0	–	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	7	–	8	–	10	–	ns
t _{SD}	Data set-up to write end	5	–	6	–	8	–	ns
t _{HD}	Data hold from write end	0	–	0	–	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to low Z ^[5]	3	–	3	–	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to high Z ^[5, 6]	–	5	–	6	–	7	ns
t _{BW}	Byte enable to end of write	7	–	8	–	9	–	ns

Notes

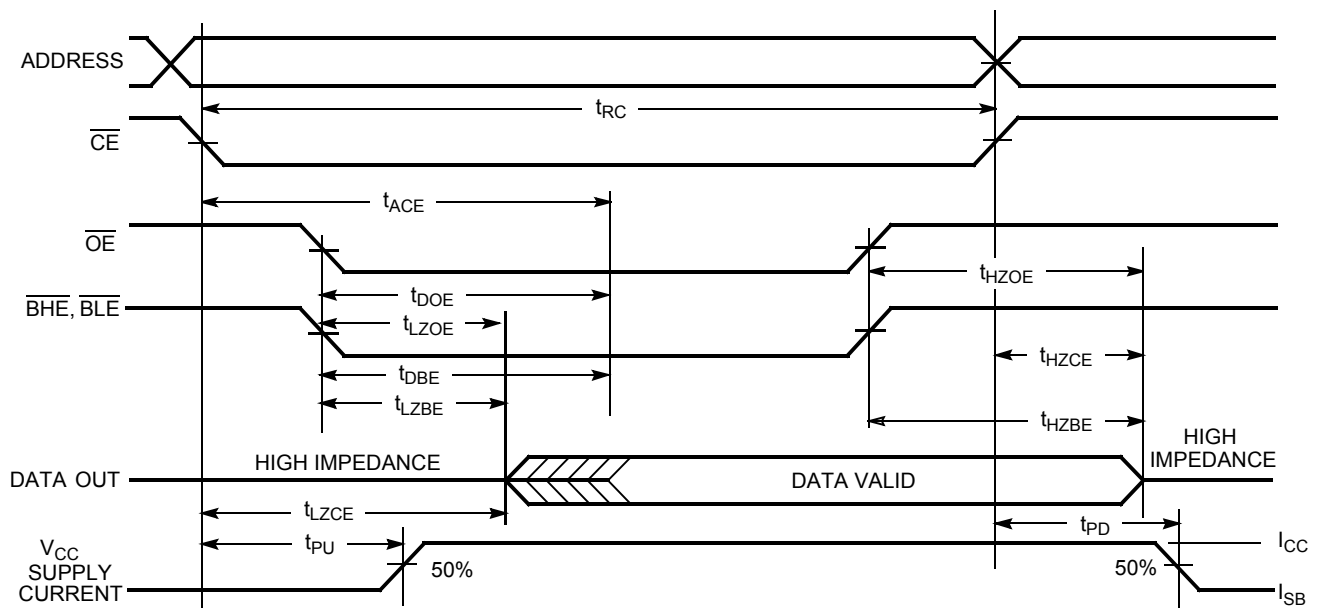
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle No. 1^[9, 10]



Read Cycle No. 2 ($\overline{OE}$ Controlled)^[10, 11]

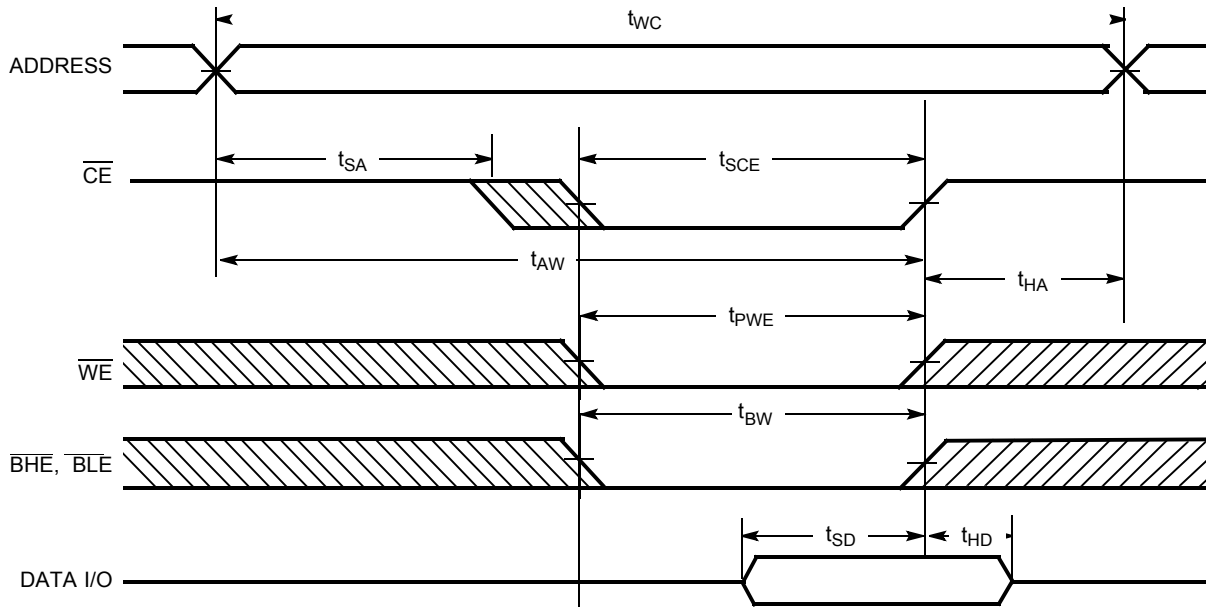


Notes

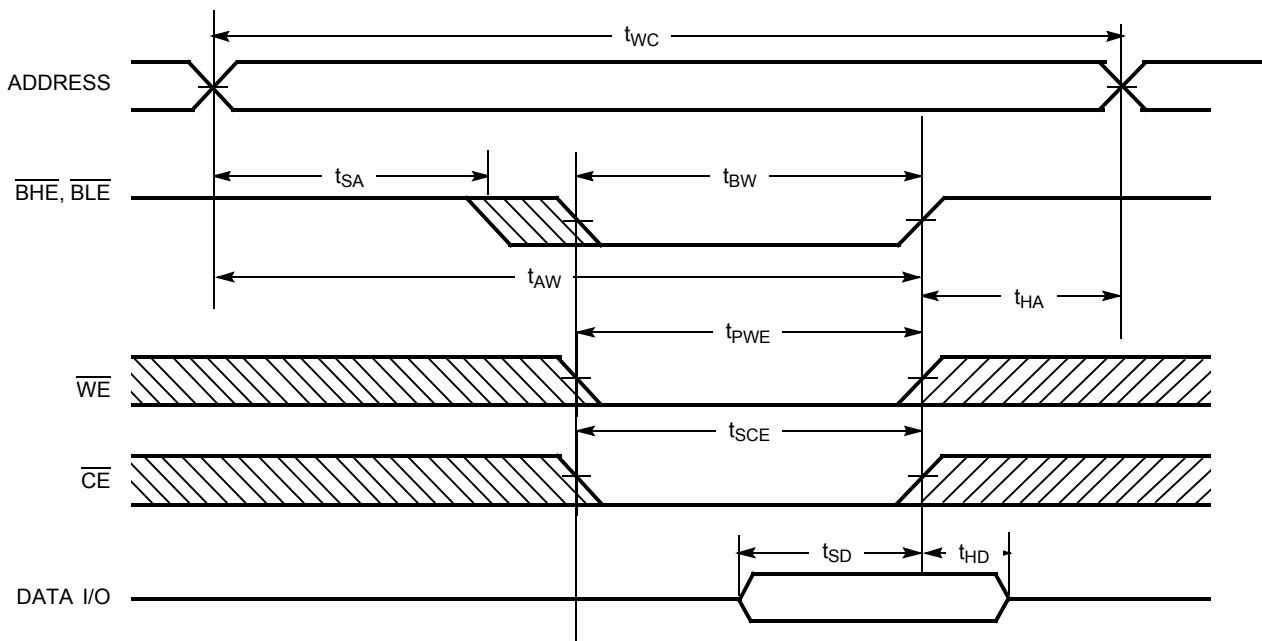
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL} .
10. $\overline{WE}$ is HIGH for Read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[12, 13]

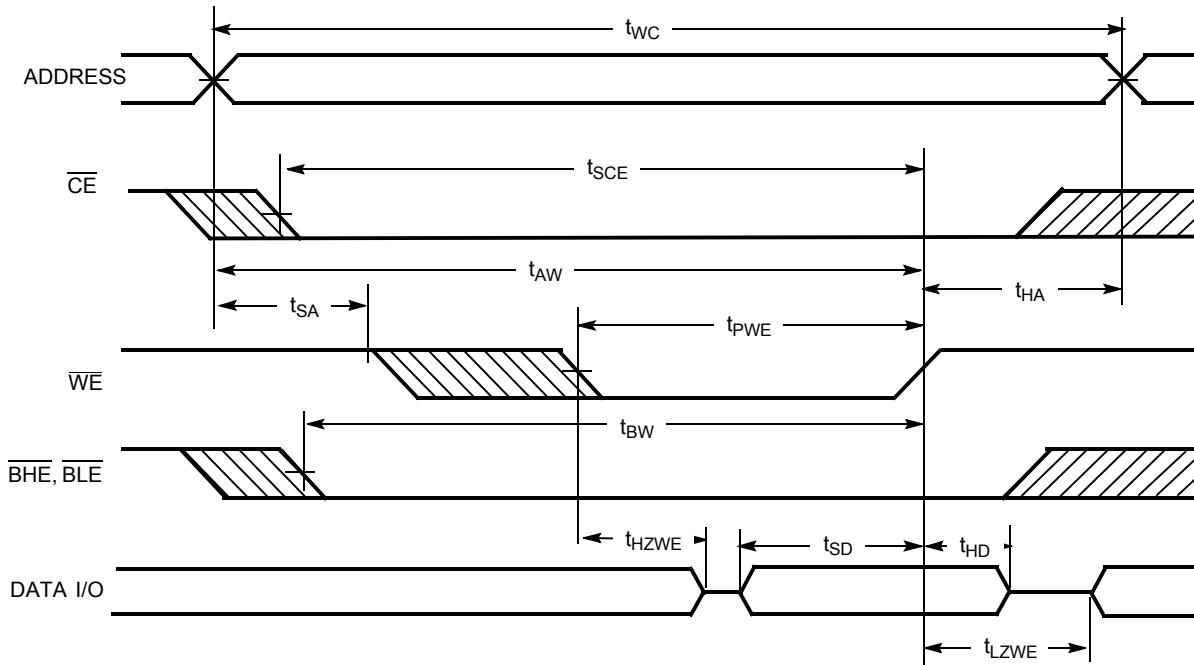


Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes

12. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)

Truth Table

CE	OE	WE	BLE	BHE	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read—All bits	Active (I_{CC})
			L	H	Data out	High Z	Read—Lower bits only	Active (I_{CC})
			H	L	High Z	Data out	Read—Upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write—All bits	Active (I_{CC})
			L	H	Data in	High Z	Write—Lower bits only	Active (I_{CC})
			H	L	High Z	Data in	Write—Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1020CV33-15ZSX E	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1020CV33-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

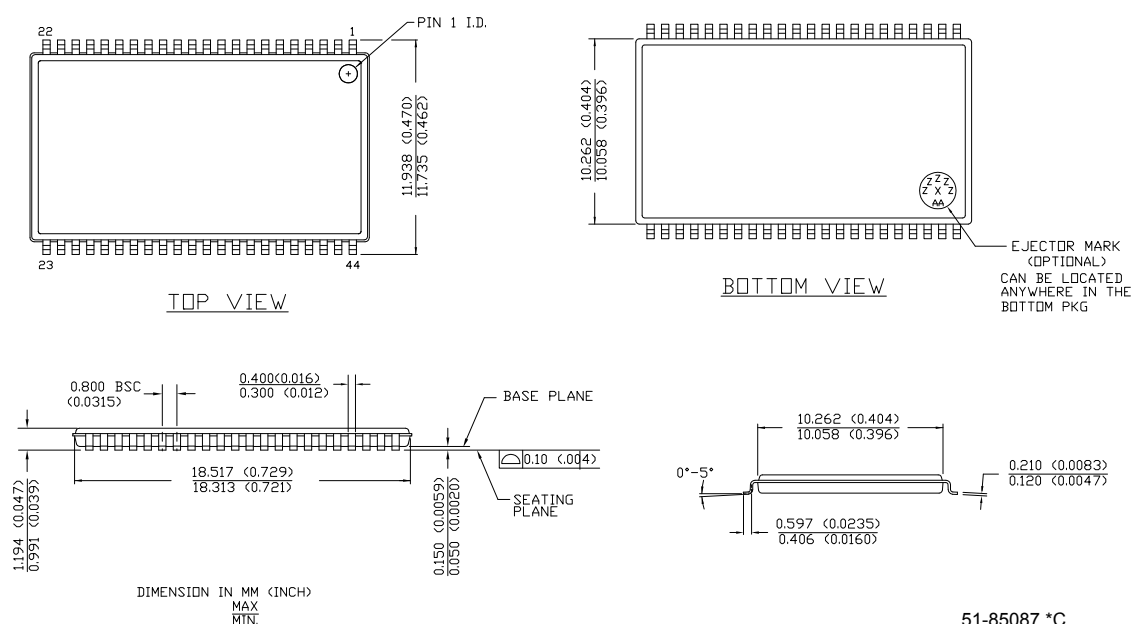
Ordering Code Definitions

CY7C 1020 C V33 - 15 ZSX E X

X = T or Blank
T = Tape and Reel; Blank = Tube
Temperature Range:
E = Automotive
Package Type:
ZSX = 44-pin TSOP Type II (Pb-free)
Speed Grade = 15 ns
V33 = 3.3 V
Process Technology = 0.16 μ m
1020 = Part Identifier
CY7C = Cypress SRAMs

Package Diagrams

Figure 1. 44-pin TSOP II, 51-85087



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

Document History Page

Document Title: CY7C1020CV33 512 K (32 K × 16) Static RAM Document Number: 38-05133				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109428	12/16/01	HGK	New Data Sheet
*A	115045	05/30/02	HGK	I _{CC} and I _{SB1} data modified
*B	117615	08/14/02	DFP	Pin 1= NC Pin 18 = A4; remove SOJ package option; remove 8ns option.
*C	262949	See ECN	RKF	Added Automotive Specs to Data sheet
*D	334398	See ECN	SYT	Added Lead-Free Product Information
*E	493543	See ECN	NXR	Added note #1 on page #1 Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table
*F	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagram
*G	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions .
*H	3100106	12/02/2010	PRAS	Added Acronyms and Units of Measure . Minor edits and updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

[psoc.cypress.com/solutions](#)
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2001-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.