

74ABT16952

16-Bit Registered Transceiver with TRI-STATE® Outputs

General Description

The 74ABT16952 is a 16-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The output pins are guaranteed to source 32 mA (24 mA mil.) and to sink 64 mA (48 mA mil.).

Features

- Separate clock, clock enable and TRI-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Commercial	Package Number	Package Description
74ABT16952CSSC (Note 1)	MS56A	56-Lead (0.300" Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT16952CMTD (Notes 1, 2)	MTD56	56-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

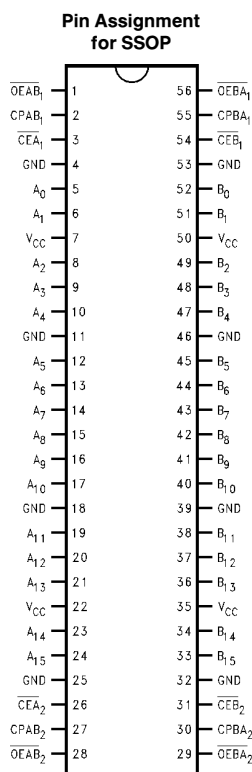
Note 1: Devices also available in 13" reel. Use suffix = SSCX and MTDX.

Note 2: Contact factory for package availability.

Pin Descriptions

Pin Names	Description
A ₀ –A ₁₆	Data Register A Inputs/ B-Register TRI-STATE Outputs
B ₀ –B ₁₆	Data Register B Inputs/ A-Register TRI-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
CEA _n , CEB _n	Clock Enable
OEAB _n , OEBA _n	Output Enable Inputs

Connection Diagram



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Pin Descriptions (Continued)

Output Control

$\overline{OE}$	Internal Q	Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	Enable Outputs

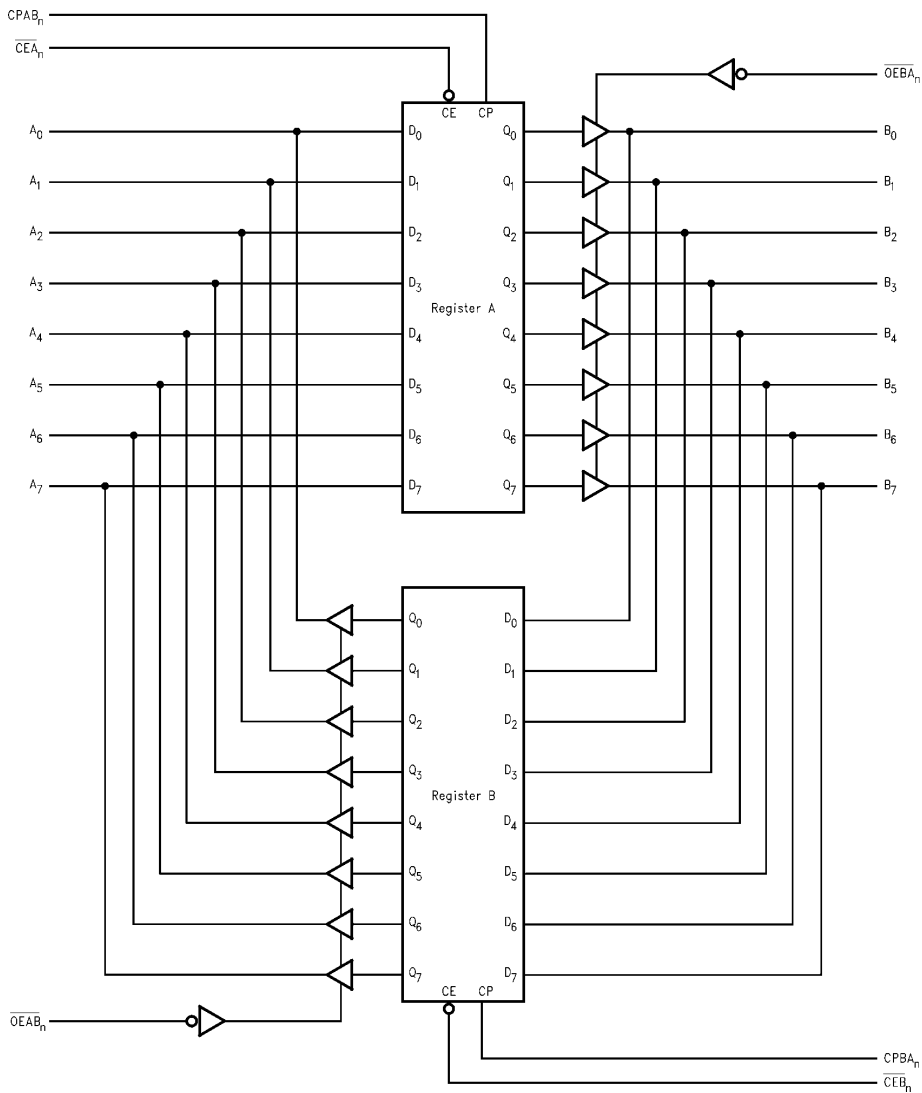
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Z = HIGH Impedance
/ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	/	L	L	Load Data
H	/	L	H	Load Data

Block Diagram



n for either byte 1 or byte 2

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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the HIGH State	−0.5V to +5.5V −0.5V to V _{CC}

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	−40°C to +85°C
Supply Voltage Commercial	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT16952			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage 74ABT 74ABT	2.5 2.0					I _{OH} = −3 mA (A _n , B _n) I _{OH} = −32 mA (A _n , B _n)
V _{OL}	Output LOW Voltage 74ABT			0.55			I _{OL} = 64 mA (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 2) V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			−5	μA	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 2) V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			50	μA	0V–5.5V	V _{OUT} = 2.7V (A _n , B _n); OEA or OEB = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V _{OUT} = 0.5V (A _n , B _n); OEA or OEB = 2.0V
I _{OS}	Output Short-Circuit Current	−100	−275		mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			100	μA	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			1.0	mA	Max	Outputs TRI-STATE; All Others GND
I _{CCT}	Additional I _{CC} /Input			2.5	mA	Max	V _I = V _{CC} − 2.1V; All Others at V _{CC} or GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT16952			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{CCD}	Dynamic I _{CC} No Load (Note 2)		0.18		mA/MHz	Max	Outputs Open OE _A or OE _B = GND, Non-I/O = GND or V _{CC} One Bit toggling, 50% duty cycle (Note 1)

Note 1: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT		74ABT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
f _{max}	Max Clock Frequency	200		200		MHz
t _{PLH} t _{PHL}	Propagation Delay CPAB _n or CPBA _n to A _n or B _n	1.5 1.5	5.3 5.3	1.5 1.5	5.3 5.3	ns
t _{PZH} t _{PZL}	Output Enable Time OEAB _n or OEBA _n to A _n or B _n	1.5 1.5	5.5 5.5	1.5 1.5	5.5 5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEAB _n or OEBA _n to A _n or B _n	1.5 1.5	6.0 6.0	1.5 1.5	6.0 6.0	ns

AC Operating Requirements

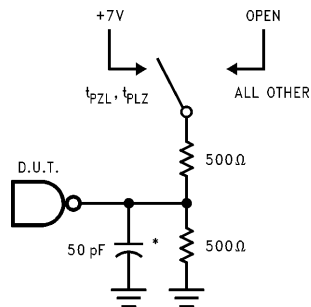
Symbol	Parameter	74ABT		74ABT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW A _n or B _n to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	2.5 2.5		2.5 2.5		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW A _n or B _n to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	1.5 1.5		1.5 1.5		ns
t _s (H) t _s (L)	Setup Time, HIGH or LOW $\overline{\text{CEA}}_n$ or $\overline{\text{CEB}}_n$ to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	2.5 2.5		2.5 2.5		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW $\overline{\text{CEA}}_n$ or $\overline{\text{CEB}}_n$ to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	1.5 1.5		1.5 1.5		ns
t _w (H) t _w (L)	Pulse Width, HIGH or LOW to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	3.0 3.0		3.0 3.0		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (Non I/O Pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

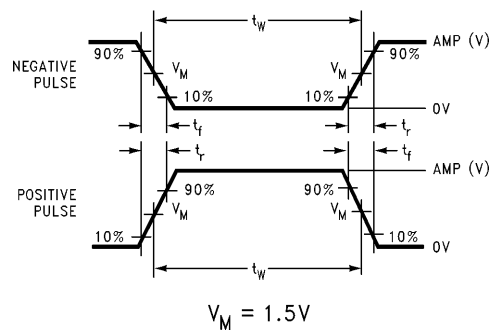
AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

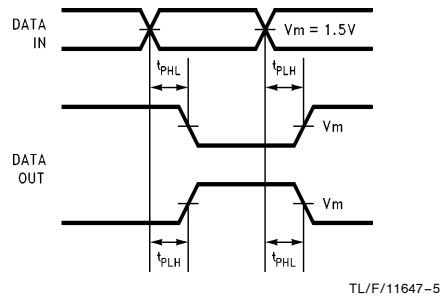


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FIGURE 2a. Test Input Signal Levels

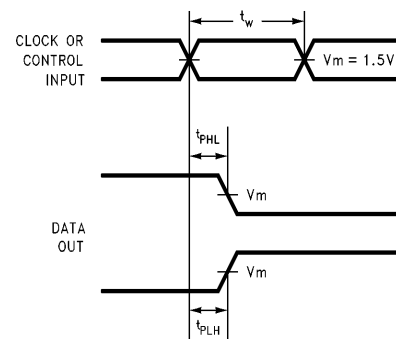
Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Input Signal Requirements



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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



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FIGURE 4. Propagation Delay, Pulse Width Waveforms

AC Loading (Continued)

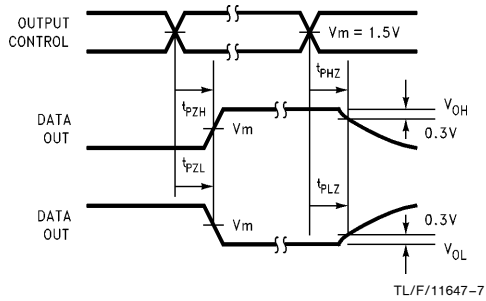


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

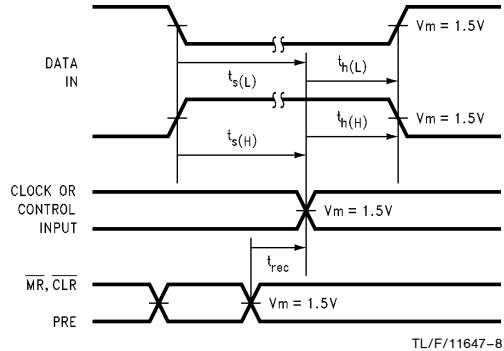
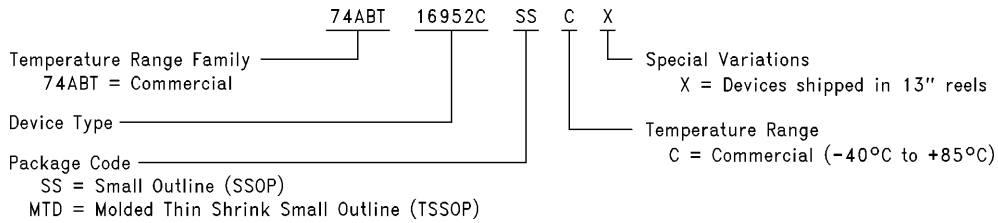


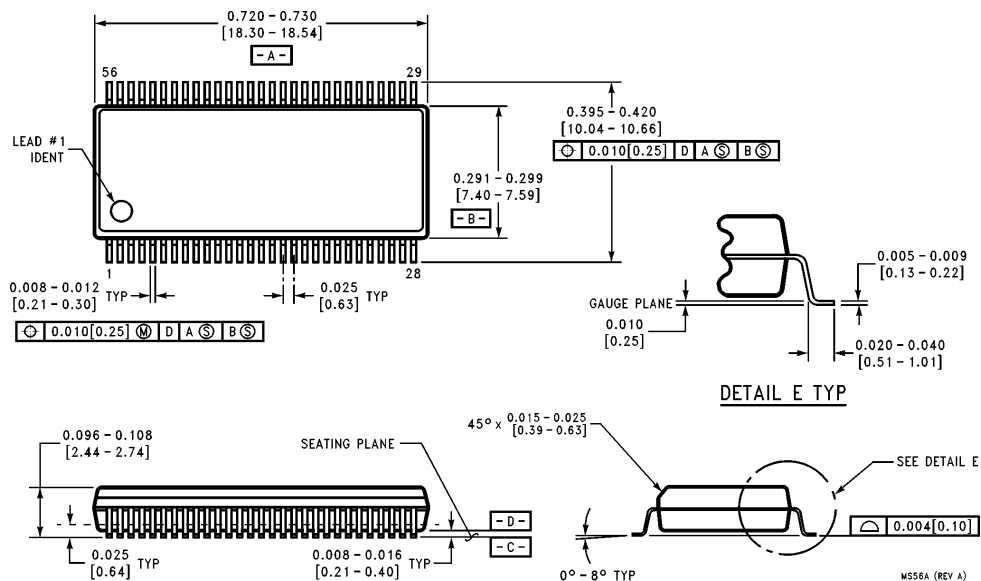
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

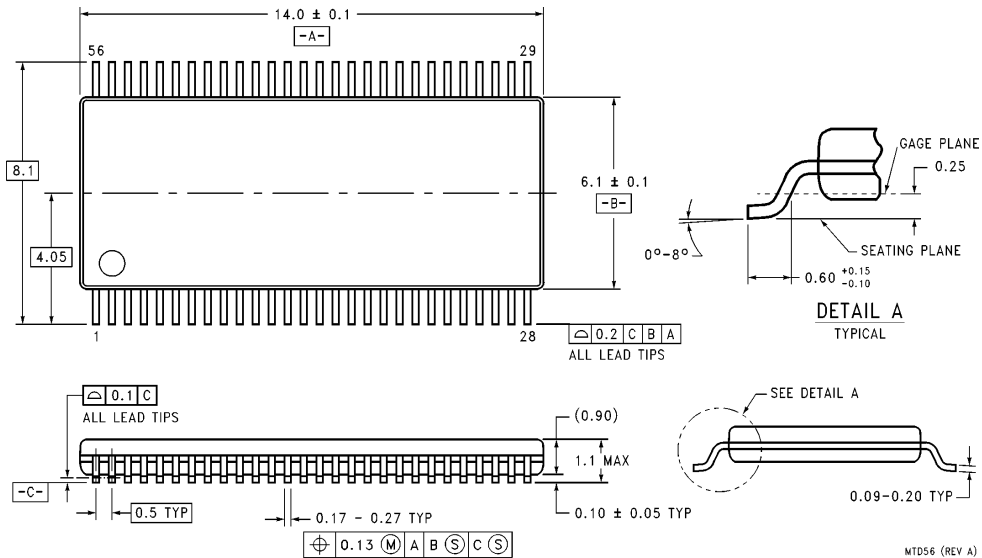


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Physical Dimensions inches (millimeters) unless otherwise noted

**56-Lead SSOP (0.300" Wide) (SS)
74ABT16952CSSC or 74ABT16952CSSCX
NS Package Number MS56A**

Physical Dimensions millimeters (Continued)



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
74ABT16952CMTD
NS Package Number MTD56

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