

# CY7C1049CV33 4-Mbit (512 K × 8) Static RAM

#### Features

- Temperature ranges
  Commercial: 0 °C to 70 °C
- High speed □ t<sub>AA</sub> = 8 ns
- Low active power 360 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- **Easy** memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features

#### **Functional Description**

The CY7C1049CV33 is a high performance CMOS Static RAM organized as 524,288 words by eight bits. Easy <u>memory</u> expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

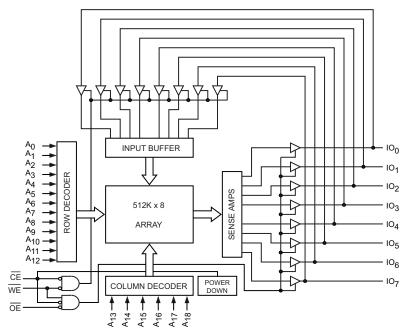
<u>Rea</u>ding from the device is <u>ac</u>complished by taking Chip Enable  $(\overline{CE})$  and Output Enable  $(\overline{OE})$  LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins  $(I/O_0 \text{ through } I/O_7)$  are placed in a high impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1049CV33 is available in standard 44-pin TSOP II package with center power and ground (revolutionary) pinout.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

#### Logic Block Diagram





## CY7C1049CV33

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#### **Selection Guide**

Description	-8	Unit
Maximum Access Time	8	ns
Maximum Operating Current	100	mA
Maximum CMOS Standby Current	10	mA

## **Pin Configuration**

Figure 1.	44-pin	TSOP	ll (Top	View)
-----------	--------	------	---------	-------

	-		
NC	1	44	⊐ NC
NC	2	43	
A <sub>0</sub> E	3	42	NC
A <sub>1</sub> E	4	41	□ A <sub>18</sub>
A <sub>2</sub> [	5	40	$\Box A_{17}$
A <sub>3</sub>	6	39	$\Box A_{16}$
$A_4$	7	38	$\Box A_{15}$
CE L	8	37	] OE
I/O <sub>0</sub>	9	36	I/O7
1/0 <sub>1</sub> [	10	35	□ I/O <sub>6</sub>
V <sub>CC</sub> E	11	34	□ V <sub>SS</sub>
V <sub>SS</sub>	12	33	
I/O <sub>2</sub>	13	32	_ I/O <sub>5</sub>
<u>I/O</u> 3 [	14	31	□ I/O <sub>4</sub>
WE [	15	30	A <sub>14</sub>
A <sub>5</sub> L	16	29	A <sub>13</sub>
A <sub>6</sub> L	17	28	A <sub>12</sub>
A7 [	18	27	A <sub>11</sub>
A <sub>8</sub>	19	26	$A_{10}$
	20	25	
	21	24	
NC 🗆	22	23	

## **Pin Definitions**

Pin Name	44-pin TSOP II Pin Number	I/O Type	Description	
A <sub>0</sub> -A <sub>18</sub>	3–7, 16–20, 26–30, 38–41	Input	Address inputs used to select one of the address locations.	
1/0 <sub>0</sub> –1/0 <sub>7</sub>	9, 10, 13, 14, 31, 32, 35, 36	Input/Output	<b>Bidirectional data I/O lines.</b> Used as input or output lines depending on operation.	
NC <sup>[1]</sup>	1, 2, 21, 22, 23, 24, 25, 42, 43, 44	No Connect	No connects. This pin is not connected to the die.	
WE	15	Input/Control	Write Enable input, active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.	
CE	8	Input/Control	Chip Enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.	
OE	37	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.	
V <sub>SS</sub> , GND	12, 34	Ground	Ground for the device. Should be connected to ground of the system.	
V <sub>CC</sub>	11, 33	Power Supply	Power supply inputs to the device.	



### **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	–65 °C to +150 °C
Ambient Temperature with	
Power Applied	. –55 °C to +125 °C
Supply Voltage on V <sub>CC</sub> to Relative GND <sup>[2</sup>	<sup>1</sup> _0.5 V to +4.6 VDC

#### **Electrical Characteristics**

Over the Operating Range

voltage Applied to Outputs	
in High Z State <sup>[2]</sup>	–0.5 V to $V_{CC}$ + 0.5 V
Input Voltage <sup>[2]</sup>	–0.5 V to V <sub>CC</sub> + 0.5 V
Current into Outputs (LOW)	

#### **Operating Range**

Valtaria Analia data Ordaria

Range	Range Ambient Temperature	
Commercial	0 °C to +70 °C	$3.3~V\pm0.3~V$

Parameter	Description Test Conditions	-8		Unit	
	Description	Test Conditions	Min	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min; I <sub>OH</sub> = -4.0 mA	2.4	-	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min; I <sub>OL</sub> = 8.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	$GND \leq V_1 \leq V_C$	–1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	$V_{CC}$ = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	-	100	mA
I <sub>SB1</sub>	Automatic CE Power Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \ge V_{IH}$ , $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ , f = f <sub>MAX</sub>	-	40	mA
I <sub>SB2</sub>	Automatic CE Power Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \ge V_{CC} - 0.3$ V, $V_{IN} \ge V_{CC} - 0.3$ V, or $V_{IN} \le 0.3$ V, f = 0	-	10	mA

#### Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

#### **Thermal Resistance**

Tested initially and after any design or process changes that may affect these parameters.

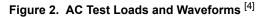
Parameter <sup>[3]</sup>	Description	Test Conditions	44-pin TSOP-II	Unit
$\Theta_{JA}$	(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring	41.66	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)	thermal impedance, per EIA / JESD51.	10.56	°C/W

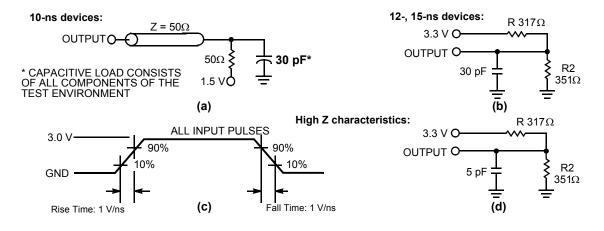
Notes

V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.5 V for pulse durations of less than 20 ns.
 Tested initially and after any design or process changes that may affect these parameters.









Note

AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in Figure 2 (a). All other speeds are tested using the Thevenin load shown in Figure 2 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (d).



### **AC Switching Characteristics**

Over the Operating Range [5]

			-8	
Parameter	Description	Min	Max	Unit
Read Cycle		•		
t <sub>power</sub> [6]	V <sub>CC</sub> (typical) to the first access	100	-	μS
t <sub>RC</sub>	Read Cycle Time	8	-	ns
t <sub>AA</sub>	Address to Data Valid	-	8	ns
t <sub>OHA</sub>	Data Hold from Address Change	3	-	ns
t <sub>ACE</sub>	CE LOW to Data Valid	-	8	ns
t <sub>DOE</sub>	OE LOW to Data Valid	-	5	ns
t <sub>LZOE</sub>	OE LOW to Low Z	0	-	ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[7, 8]</sup>	-	4	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[8]</sup>	3	-	ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[7, 8]</sup>	-	4	ns
t <sub>PU</sub>	CE LOW to Power Up	0	-	ns
t <sub>PD</sub>	CE HIGH to Power Down	-	8	ns
Write Cycle <sup>[9, 10]</sup>				
t <sub>WC</sub>	Write Cycle Time	8	-	ns
t <sub>SCE</sub>	CE LOW to Write End	6	-	ns
t <sub>AW</sub>	Address Setup to Write End	6	-	ns
t <sub>HA</sub>	Address Hold from Write End	0	-	ns
t <sub>SA</sub>	Address Setup to Write Start	0	-	ns
t <sub>PWE</sub>	WE Pulse Width	6	-	ns
t <sub>SD</sub>	Data Setup to Write End		-	ns
t <sub>HD</sub>	Data Hold from Write End	0	-	ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[8]</sup>	3	-	ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[7, 8]</sup>	-	4	ns

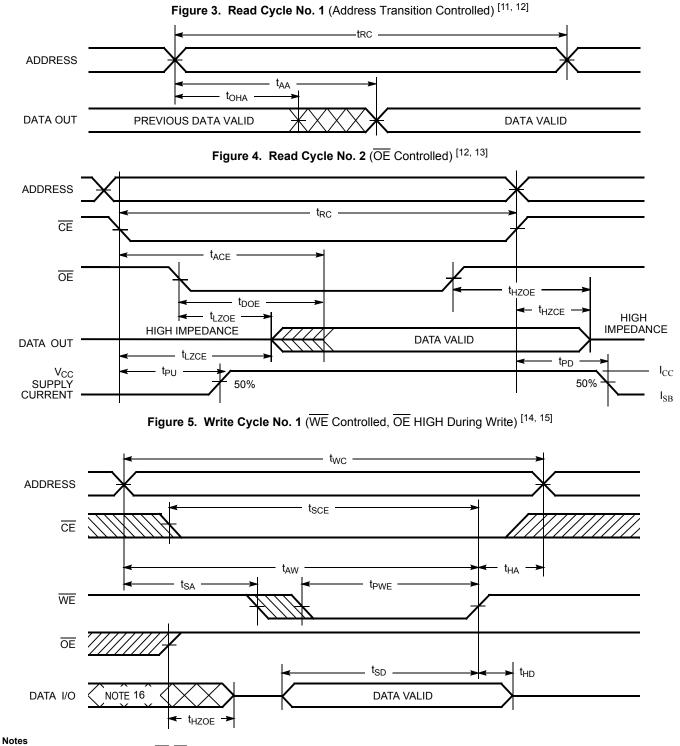
Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

fest conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
 t<sub>POWER</sub> gives the minimum amount of time that the power supply should be at stable, typical V<sub>CC</sub> values until the first memory access can be performed.
 t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
 At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>.
 The internal Write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data <u>set</u>up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
 The minimum Write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



#### Switching Waveforms



- 13. Address valid before or similar to  $\overline{CE}$  transition LOW.
- 14. Data I/O is high impedance if  $\overline{OE} = V_{IL}$ 15. If  $\overline{OE}$  goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.
- 16. During this period, the I/Os are in output state. Do not apply input signals.



#### Switching Waveforms (continued)

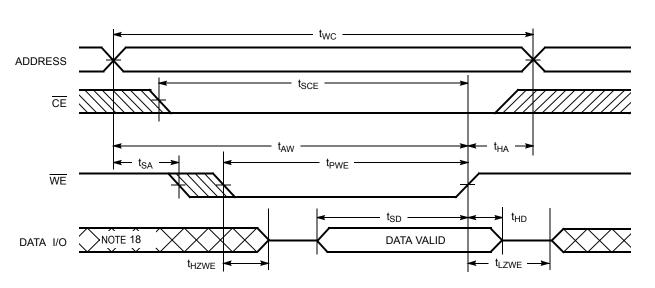


Figure 6. Write Cycle No. 2 (WE Controlled, OE LOW) <sup>[17]</sup>

#### **Truth Table**

CE	OE	WE	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
Н	Х	Х	High Z	Power Down	Standby (I <sub>SB</sub> )
L	L	Н	Data Out	Read	Active (I <sub>CC</sub> )
L	Х	L	Data In	Write	Active (I <sub>CC</sub> )
L	Н	Н	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

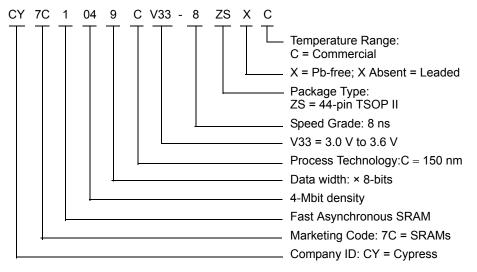
 $\begin{array}{l} \textbf{Notes} \\ \textbf{17. If CE goes HIGH simultaneously with } \overline{\text{WE HIGH}}, \text{ the output remains in high impedance state.} \\ \textbf{18. During this period, the I/Os are in output state. Do not apply input signals.} \end{array}$ 



#### **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
8	CY7C1049CV33-8ZSXC	51-85087	44-pin TSOP II (Pb-free)	Commercial

#### **Ordering Code Definitions**





### Package Diagram

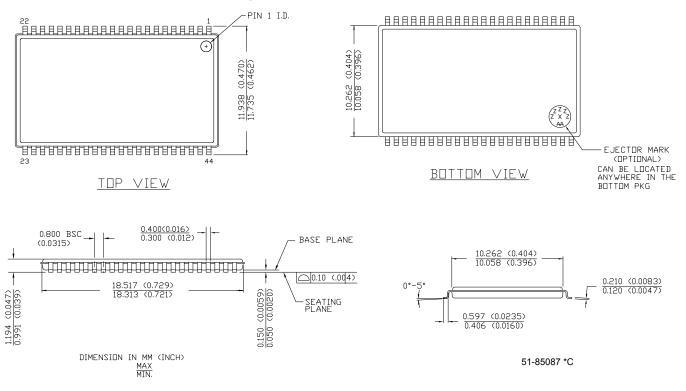


Figure 7. 44-pin TSOP II, 51-85087



### Acronyms

Acronym	Description		
CMOS	complementary metal oxide semiconductor		
CE	Chip Enable		
OE	Output Enable		
RAM	Random Access Memory		
I/O	Input/Output		
SOJ	small outline J-lead		
TTL	transistor-transistor logic		
TSOP	thin small outline package		
WE	Write Enable		

### **Document Conventions**

#### Units of Measure

Symbol	Unit of Measure
Ω	ohms
ns	nano seconds
V	Volts
μs	micro seconds
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
%	percent
mW	milli Watts
W	Watts
°C	degree Celcius



## **Document History Page**

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	112569	HGK	03/06/02	New data sheet
*A	114091	DFP	04/25/02	Changed Tpower unit from ns to μs
*B	116479	CEA	09/16/02	Add applications foot note to data sheet, page 1.
*C	262949	RKF	See ECN	Added Automotive-E Specs Added $\Theta_{JA}$ and $\Theta_{JC}$ values on Page #3.
*D	300091	RKF	See ECN	Added -20-ns Speed bin
*E	344595	SYT	See ECN	Added Pb-free package on page #8 Removed shading for CY7C1049CV33-15ZSXE in the ordering Information on page 9
*F	2615344	VKN/PYRS	12/03/08	Added Automotive-A information Removed 8 ns and 20 ns speed bins, Changed t <sub>POWER</sub> spec from 1 μs to 100 μs, Updated Ordering Information table.
*G	2841563	NXR/	01/07/2010	Added CY7C1049CV33-10VXA to Ordering Info table.
*H	2898958	AJU	03/25/10	Removed inactive parts from the ordering informaiton table. Updated package diagrams.
*	2954734	AJU	06/30/2010	New Part Number added CY7C1049CV33-10ZXC to Ordering Info table.
*J	3072834	PRAS	11/12/2010	Removed obsolete parts and updated package diagram.
*K	3185812	PRAS	03/02/2011	Updated Features. Updated Functional Description. Updated Selection Guide (Added -8 ns speed grade devices and removed -10 ns, -12 ns, and -15 ns speed grade devices). Removed Figure 36-pin SOJ (Top View) in Pin Configuration. Updated Electrical Characteristics (Added -8 ns speed grade devices and removed -10 ns, -12 ns, and -15 ns speed grade devices). Deleted 36-pin SOJ column in Thermal Resistance. Updated AC Switching Characteristics (Added -8 ns speed grade devices and removed -10 ns, -12 ns, and -15 ns speed grade devices). Added Units of Measure. Dislodged Automotive information to 001-67511. Removed SOJ package related information in all instances in the document.



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