NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD16502

CCD DRIVER CMOS IC

The μPD16502 is a vertical drive interface for CCD area image sensor incorporating a level conversion circuit and three-level output function.

Using the CMOS process provides a low power consumption and a optimum transmission delay and low output ON resistance to drive the CCD image sensor.

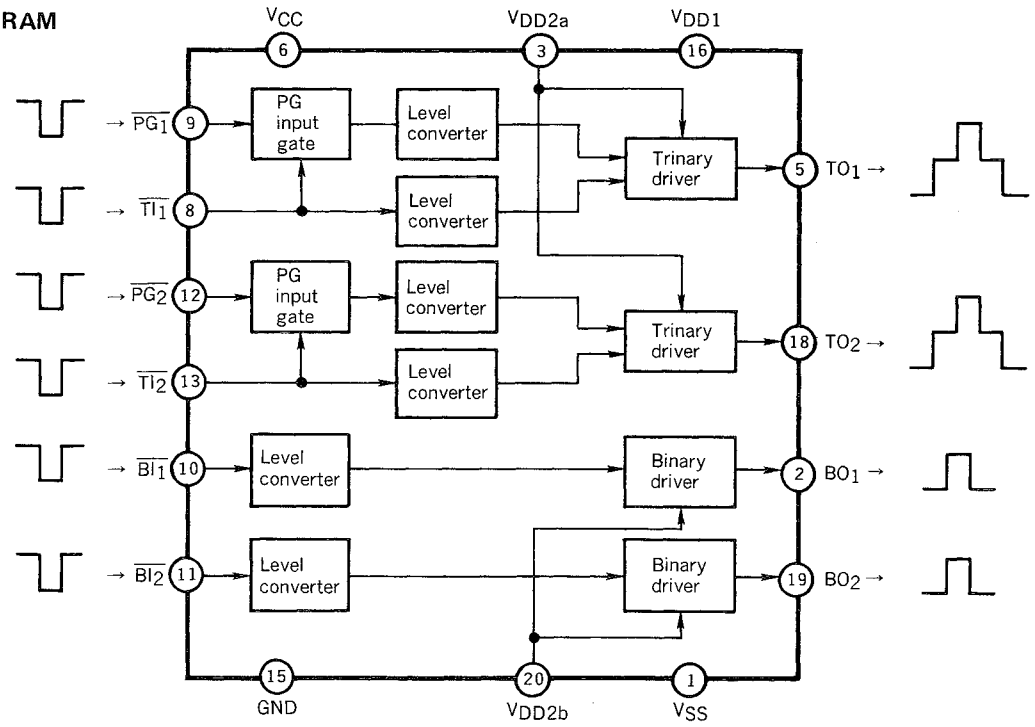
FEATURES

- Low power consumption: 6.0 mA TYP.
- Low output ON resistance: 18 Ω TYP.
- High withstand voltage: 25 V MAX.
- Complete one-chip vertical drive interface circuit capable of connection with the clock generator (CMOS IC)
  Middle level power V_{DD2a} and V_{DD2b} can be set with separate voltage.

ORDERING INFORMATION

Order name	Package
μPD16502GS	20-pin plastic SOP (300 mil)

BLOCK DIAGRAM



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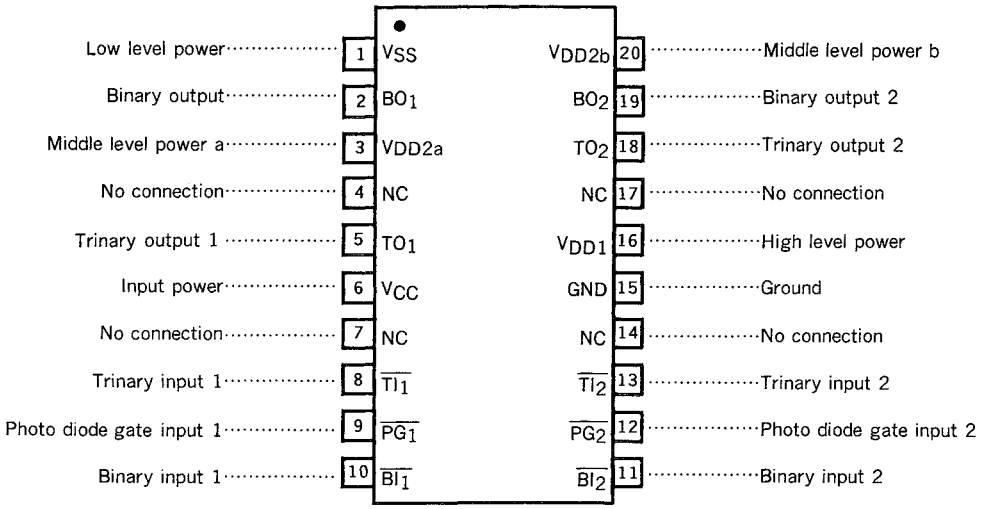
TERMINAL CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, GND = 0 V)

Power Withstand Voltage 1	$V_{DD1} - V_{SS}$	25	V
Power Withstand Voltage 2	$V_{DD2} - V_{SS}$	17	V
Power Withstand Voltage 3	V_{CC} – GND	7	V
Low Level Power Withstand Voltage	V_{SS} – GND	–10	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
I/O Clamp Diode Current	I_{IC}, I_{OC}	±10	mA
Maximum DC Load Current	I_{ODC}	±3	mA
Maximum Load Capacitance	C_L	30 000	pF/pin
Allowable Loss	P_D	200	mW
Storage Temperature	T_{stg}	–60 to +150	°C

Note: Use voltage $V_{DD2} < V_{CC}$

RECOMMENDED OPERATING CONDITIONS

(If no special specifications are stated grounding is 0 V, T_a ranges from −10 to +60 °C.)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Voltage Across the Power 1 and Power 2 Supply	$V_{DD1} - V_{DD2}$	6.5 to 15.5	V
Voltage Across the Power 2 and Low Level Power Supply	$V_{DD2} - V_{SS}$	7.0 to 10.0	V
Power 2 Supply	V_{DD2}	0.0 to 4.0	V
Power 3 Supply	V_{CC}	4.75 to 5.25	V
High Level Input Voltage	V_{IH}*	3.5 to V_{CC}	V
Low Level Input Voltage	V_{IL}*	0.0 to 1.0	V
Operating Temperature	T_{opt}	−10 to +60	°C

* V_{CC} = 5.0 V

DC CHARACTERISTIC

(If there is no specification, V_{dd1} is 14.5 V, V_{dd2} is 1 V, V_{CC} is 5 V, grounding is 0 V, V_{SS} is −6 V, and T_a ranges from −10 to +60 °C.)

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High Level Output Voltage (High level)	V_{OH} (H)	V_I = GND, V_{CC} I_O = −1 mA	V_{DD1} −0.1		V_{DD1}	V
High Level Output Voltage (Middle level)	V_{OH} (M)	V_I = GND, V_{CC} I_O = −1 mA	V_{DD2} −0.1		V_{DD2}	V
Low Level Output Voltage (Low level)	V_{OL} (L)	V_I = GND, V_{CC} I_O = 1 mA	V_{SS} +0.1		V_{SS}	V
Input Current	I_I	V_I = GND, V_{CC}			1.0	μA
Output on Resistance (High level)	R_{ON} (H)	I_O = −50 mA		18	30	Ω
Output on Resistance (Middle level)	R_{ON} (M)	I_O = −50 mA		18	30	Ω
Output on Resistance (Low level)	R_{ON} (L)	I_O = 50 mA		18	30	Ω
Static Current Consumption	$I_{CC} + I_{DD1} + I_{DD2}$	V_I = GND, V_{CC}		10^{-4}	100	μA

AC CHARACTERISTIC

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmission Delay Time	t_{PLH}, t_{PHL}	No load. See Figure 1.		100	200	ns
Transmission Delay Time	t_{PLH}, t_{PHL}	Middle level ⇄ High level		200	400	ns
Rising and Falling Time	t_{TLH}, t_{THL}	Load circuit. See Figure 2.		200	300	ns
Current Consumption	I_{dyn} (I_{CC} + I_{DD1} + I_{DD2} + I_{SS})	Input pulse timing is Figure 3.		6.0	10	mA
	I_{CC}			0.02	0.2	mA
	I_{DD1} + I_{DD2}			3.8	5.0	mA
	I_{SS}		−5.0	−3.8		mA

Fig. 1 Transmission Delay Time

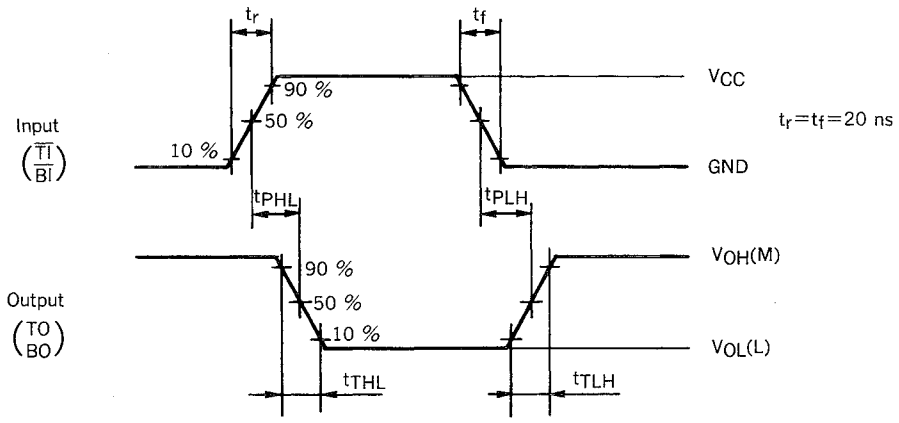


Fig. 2 Output Load Circuit

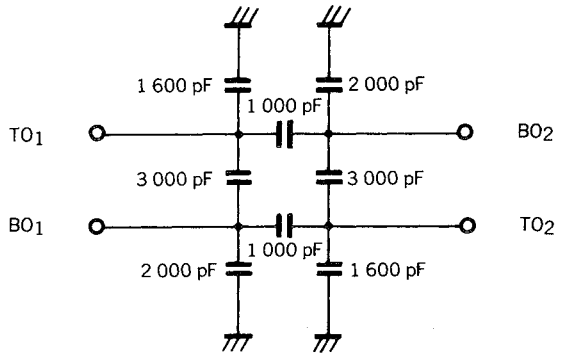
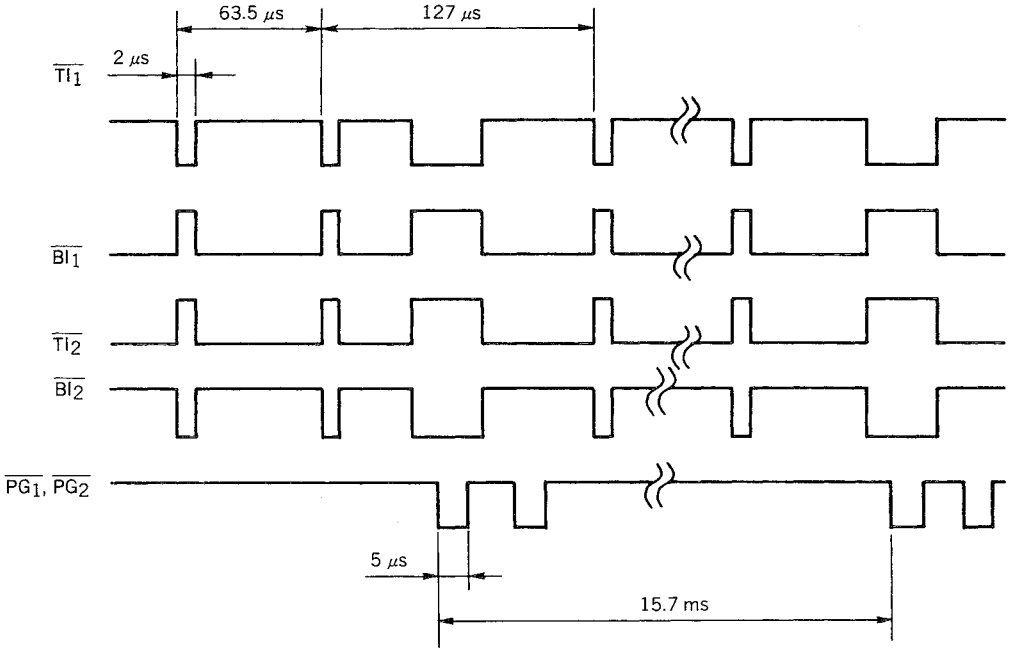
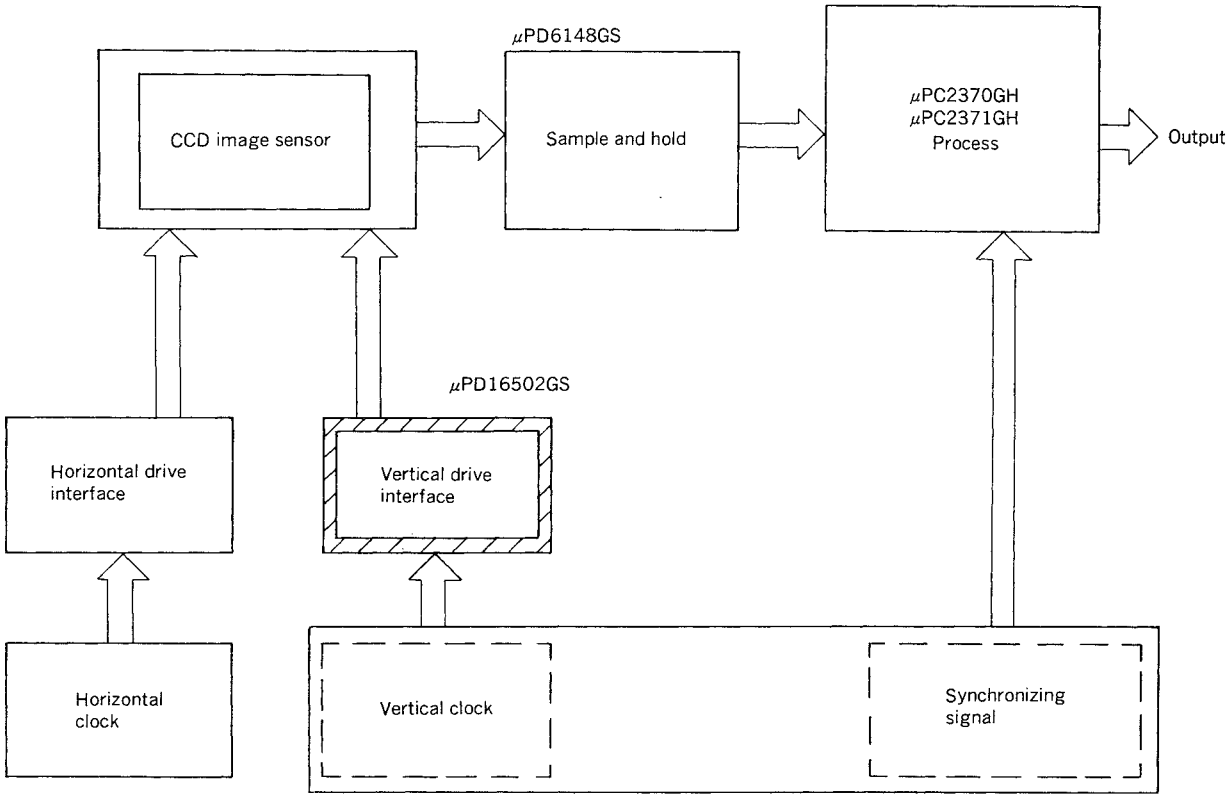


Fig. 3 Input Pulse Timing Diagram

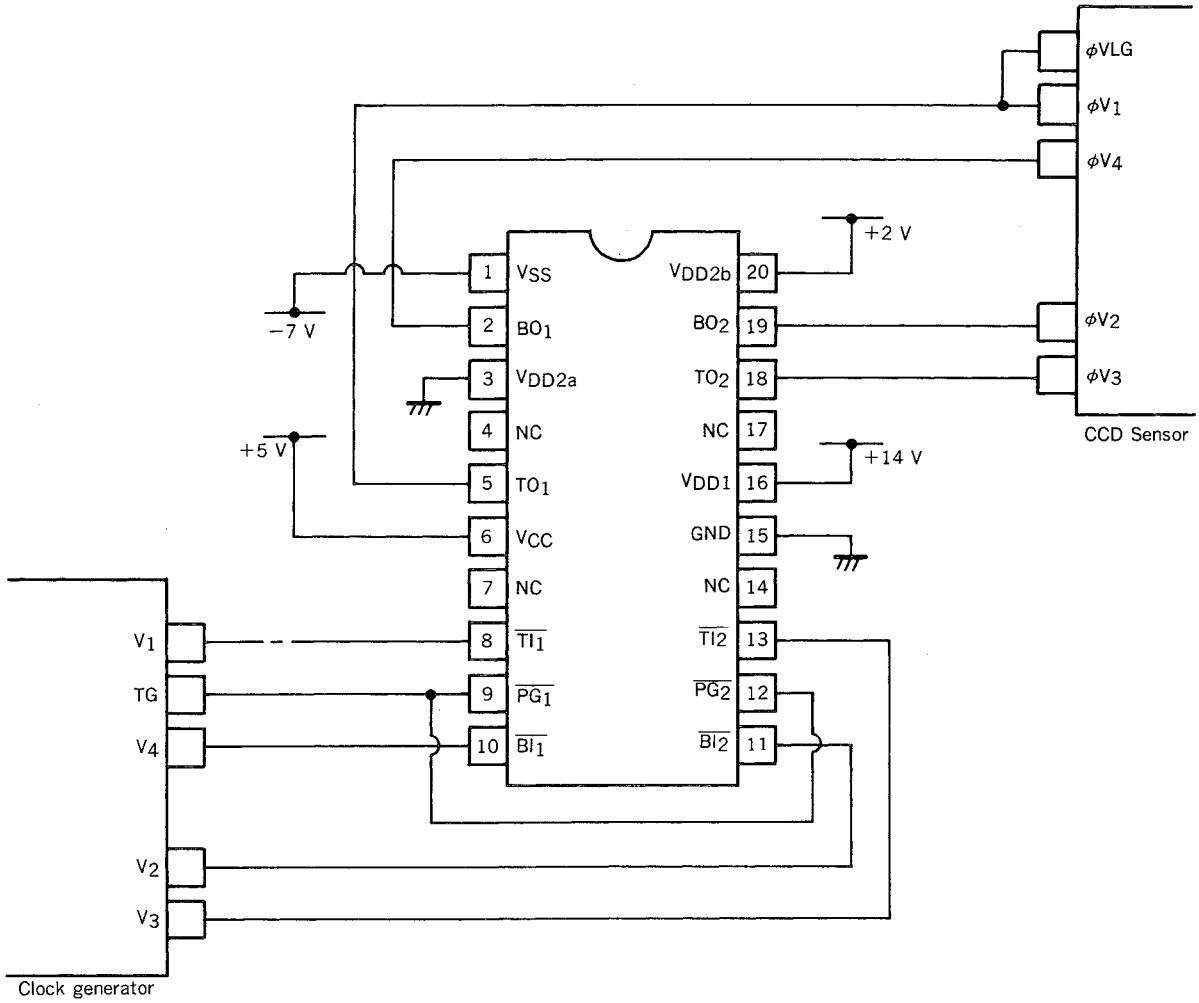


APPLICATION CIRCUIT EXAMPLE

CCD Camera Drive Block Diagram



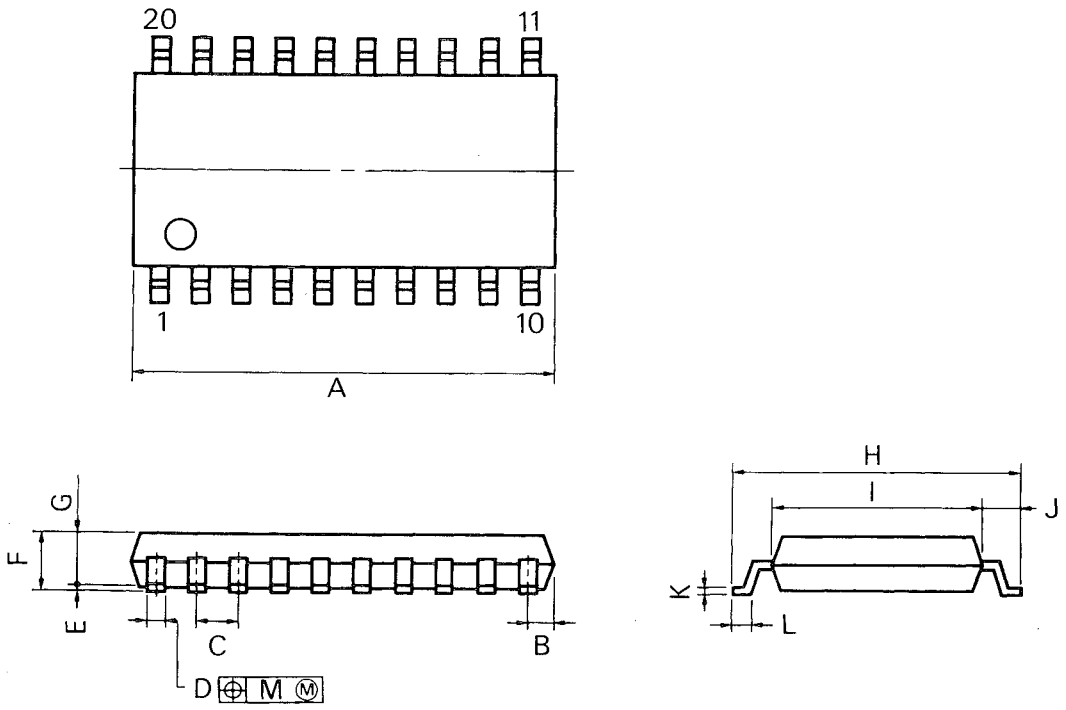
SAMPLE APPLICATION CIRCUIT



Note 1. Turn on the power V_{DD1} before V_{CC} and V_{DD2}

2. PG_1 (terminal 9) and PG_2 (terminal 12) are able to input both common signal and different signal.

20PIN PLASTIC SOP (300 mil)



P20GM-50-300B,C-1

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.