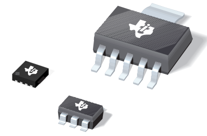


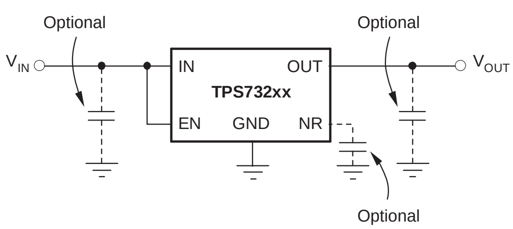
Cap-Free, NMOS, 250mA Low Dropout Regulator with Reverse Current Protection

FEATURES

- **Stable with No Output Capacitor or Any Value or Type of Capacitor**
- **Input Voltage Range: 1.7V to 5.5V**
- **Ultralow Dropout Voltage: 40mV Typ at 250mA**
- **Excellent Load Transient Response—with or without Optional Output Capacitor**
- **New NMOS Topology Provides Low Reverse Leakage Current**
- **Low Noise: 30μV_{RMS} Typ (10kHz to 100kHz)**
- **0.5% Initial Accuracy**
- **1% Overall Accuracy (Line, Load, and Temperature)**
- **Less Than 1μA Max I_Q in Shutdown Mode**
- **Thermal Shutdown and Specified Min/Max Current Limit Protection**
- **Available in Multiple Output Voltage Versions**
  - **Fixed Outputs of 1.20V to 5.0V**
  - **Adjustable Outputs from 1.20V to 5.5V**
  - **Custom Outputs Available**

APPLICATIONS

- **Portable/Battery-Powered Equipment**
- **Post-Regulation for Switching Supplies**
- **Noise-Sensitive Circuitry such as VCOs**
- **Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors**



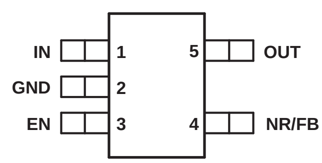
Typical Application Circuit for Fixed-Voltage Versions

DESCRIPTION

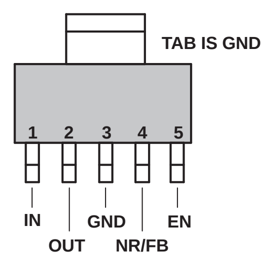
The TPS732xx family of low-dropout (LDO) voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS732xx uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1μA and ideal for portable applications. The extremely low output noise (30μV_{RMS} with 0.1μF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

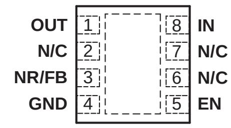
**DBV PACKAGE
SOT23
(TOP VIEW)**



**DCQ PACKAGE
SOT223
(TOP VIEW)**



**DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

PRODUCT	V_{OUT}[2]
TPS732***xxyyyz***	**XX** is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable[3]). **YYY** is package designator. **Z** is package quantity.

(1) For the most current specification and package information, refer to the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.
(2) Output voltages from 1.2V to 4.5V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 1.2V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted[1]

	TPS732xx	UNIT
V_{IN} range	–0.3 to 6.0	V
V_{EN} range	–0.3 to 6.0	V
V_{OUT} range	–0.3 to 5.5	V
V_{NR}, V_{FB} range	–0.3 to 6.0	V
Peak output current	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation	See Dissipation Ratings Table	
Junction temperature range, T_J	–55 to +150	°C
Storage temperature range	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS[1]

BOARD	PACKAGE	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K[2]	DBV	64°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K[3]	DBV	64°C/W	180°C/W	5.6mW/°C	560mW	310mW	225mW
Low-K[2]	DCQ	15°C/W	53°C/W	18.9mW/°C	1.89W	1.04W	0.76W
High-K[3][4]	DRB	1.2°C/W	40°C/W	25.0mW/°C	2.50W	1.38W	1.0W

(1) See *Power Dissipation* in the ***Applications*** section for more information related to thermal design.
(2) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch x 3 inch, two-layer board with 2-ounce copper traces on top of the board.
(3) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.
(4) Based on preliminary thermal simulations.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(nom)}$ + 0.5V(1), I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1μF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			1.7		5.5	V
V_{FB}	Internal reference (TPS73201)		T_J = +25°C	1.198	1.20	1.210	V
V_{OUT}	Output voltage range (TPS73201)(2)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)	Nominal	T_J = +25°C	–0.5		+0.5	%
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10 mA ≤ I_{OUT} ≤ 250mA	–1.0	±0.5	+1.0	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1mA ≤ I_{OUT} ≤ 250mA		0.002		%/mA
			10mA ≤ I_{OUT} ≤ 250mA		0.0005		
V_{DO}	Dropout voltage(3) ($V_{IN} = V_{OUT}$ (nom) – 0.1V)		I_{OUT} = 250mA		40	150	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	250	425	600	mA
I_{SC}	Short-circuit current		V_{OUT} = 0V		300		mA
I_{REV}	Reverse leakage current(4) (–I_{IN})		V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT} –40°C ≤ T_J ≤ +100°C		0.1	10	μA
I_{GND}	Ground pin current		I_{OUT} = 10mA (I_Q)		400	550	μA
			I_{OUT} = 250mA		650	950	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5		0.02	1	μA
I_{FB}	FB pin current (TPS73201)				0.1	0.3	μA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100Hz, I_{OUT} = 250 mA		58		dB
			f = 10kHz, I_{OUT} = 250 mA		37		
V_N	Output noise voltage BW = 10Hz – 100kHz		C_{OUT} = 10μF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10μF, C_{NR} = 0.01μF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3V, R_L = 30Ω C_{OUT} = 1 μF, C_{NR} = 0.01 μF		600		μs
V_{EN}(HI)	Enable high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	Enable low (shutdown)			0		0.5	V
I_{EN}(HI)	Enable pin current (enabled)		V_{EN} = 5.5V		0.02	0.1	μA
T_{SD}	Thermal shutdown temperature		Shutdown Temp increasing		+160		°C
			Reset Temp decreasing		+140		
T_J	Operating junction temperature			–40		+125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.7V, whichever is greater.
(2) TPS73201 is tested at V_{OUT} = 2.5V.
(3) V_{DO} is not measured for the TPS73214, TPS73215 or TPS73216 since minimum V_{IN} = 1.7V.
(4) Fixed-voltage versions only; refer to ***Applications*** section for more information.

FUNCTIONAL BLOCK DIAGRAMS

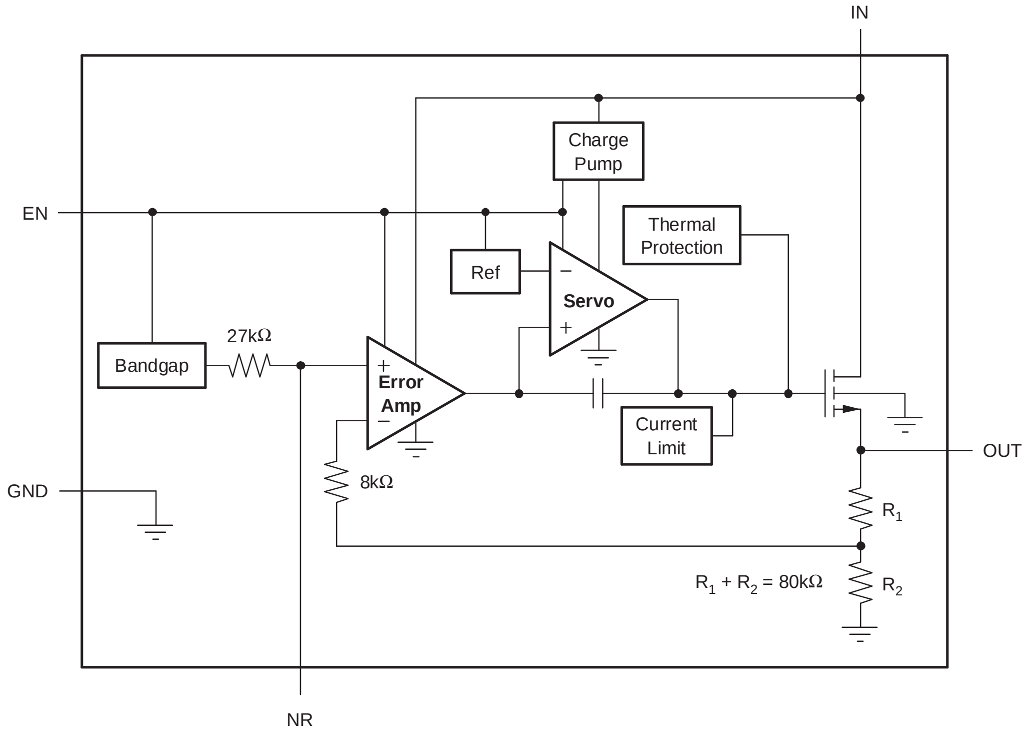


Figure 1. Fixed Voltage Version

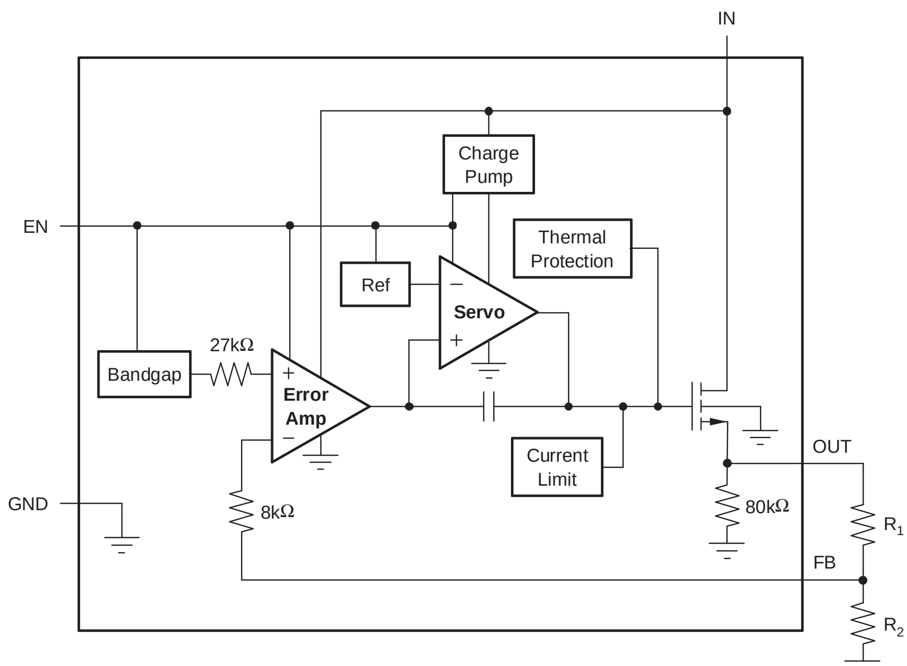


Figure 2. Adjustable Voltage Version

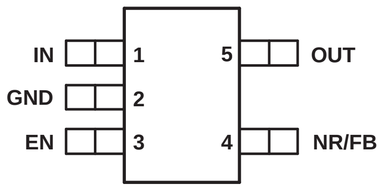
Table 1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ
5.0V	78.7kΩ	24.9kΩ

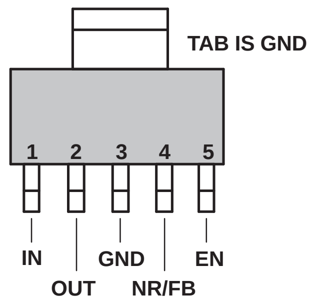
NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 \| R_2 \cong 19k\Omega$ for best accuracy.

PIN ASSIGNMENTS

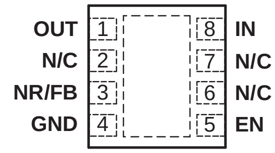
DBV PACKAGE
SOT23
(TOP VIEW)



DCQ PACKAGE
SOT223
(TOP VIEW)



DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL				
NAME	SOT23 (DBV) PIN NO.	SOT223 (DCQ) PIN NO.	3×3 SON (DRB) PIN NO.	DESCRIPTION
IN	1	1	8	Input supply
GND	2	3	4, Pad	Ground
EN	3	5	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the Shutdown section under Applications Information for more details. EN can be connected to IN if not used.
NR	4	4	3	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	4	3	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	2	1	Output of the Regulator. There are no output capacitor requirements for stability.

TYPICAL CHARACTERISTICS

For all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF, unless otherwise noted.

LOAD REGULATION

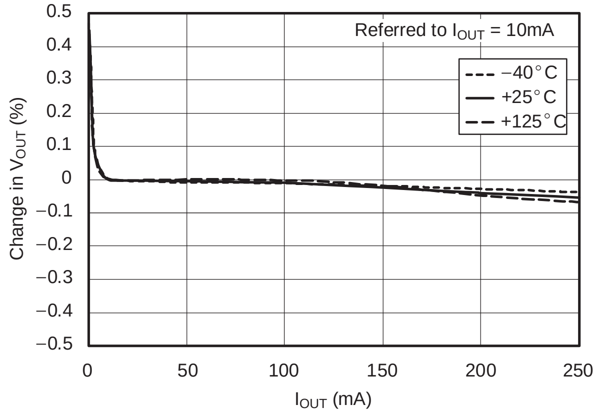


Figure 3.

LINE REGULATION

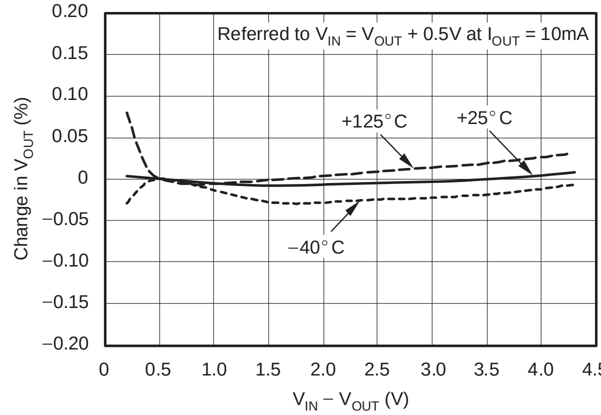


Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

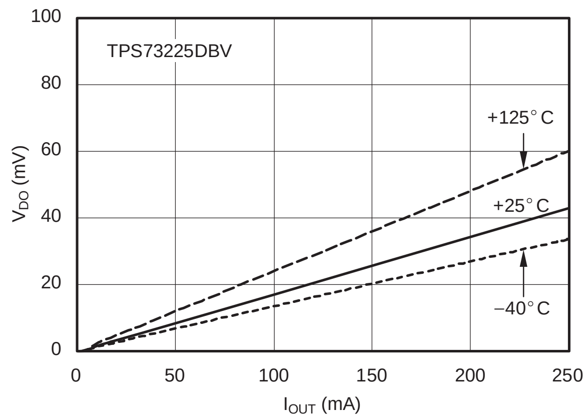


Figure 5.

DROPOUT VOLTAGE vs TEMPERATURE

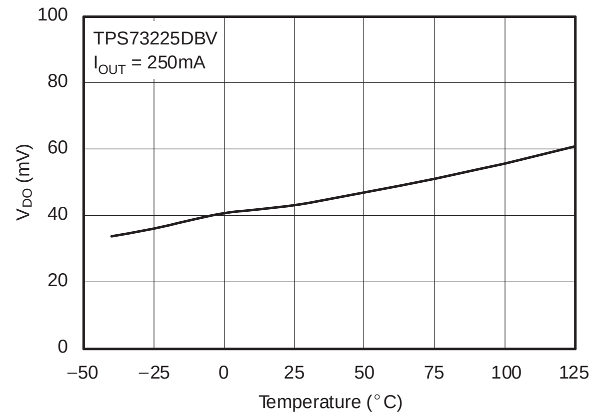


Figure 6.

OUTPUT VOLTAGE ACCURACY HISTOGRAM

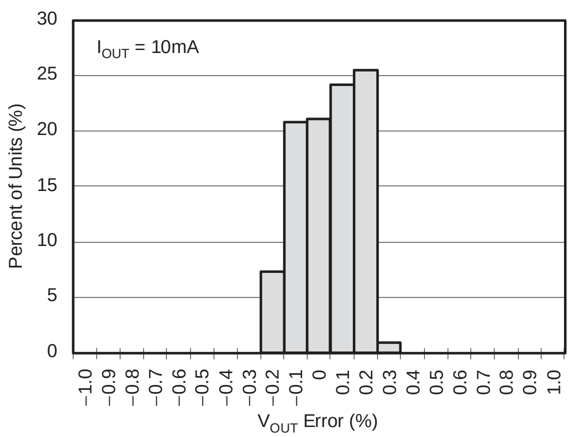


Figure 7.

OUTPUT VOLTAGE DRIFT HISTOGRAM

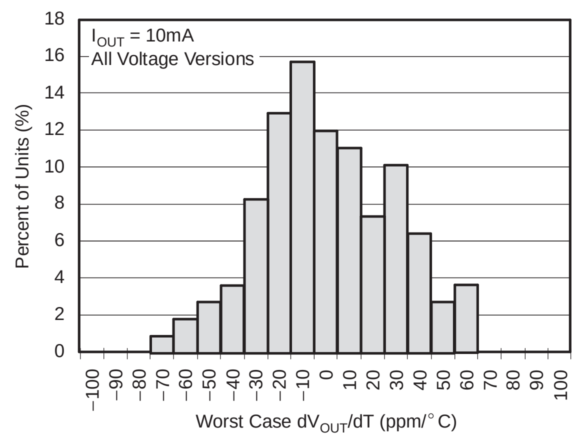


Figure 8.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF, unless otherwise noted.

GROUND PIN CURRENT vs OUTPUT CURRENT

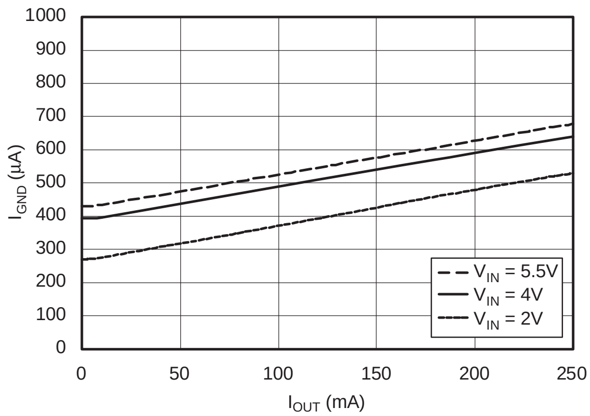


Figure 9.

GROUND PIN CURRENT vs TEMPERATURE

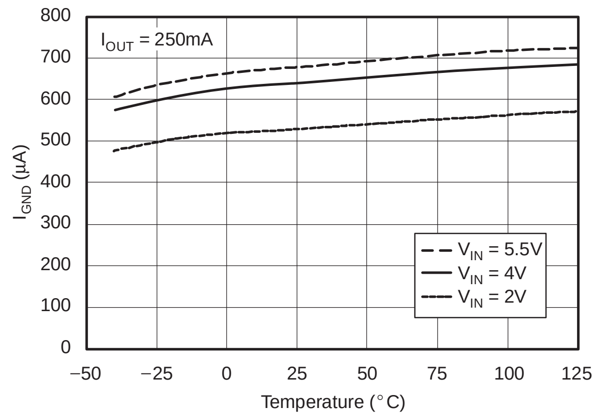


Figure 10.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

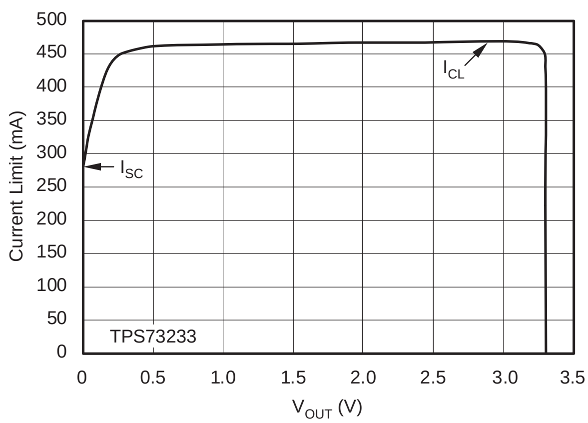


Figure 11.

GROUND PIN CURRENT IN SHUTDOWN vs TEMPERATURE

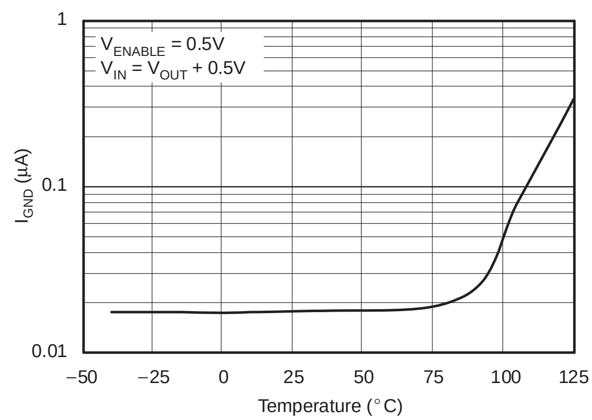


Figure 12.

CURRENT LIMIT vs V_{IN}

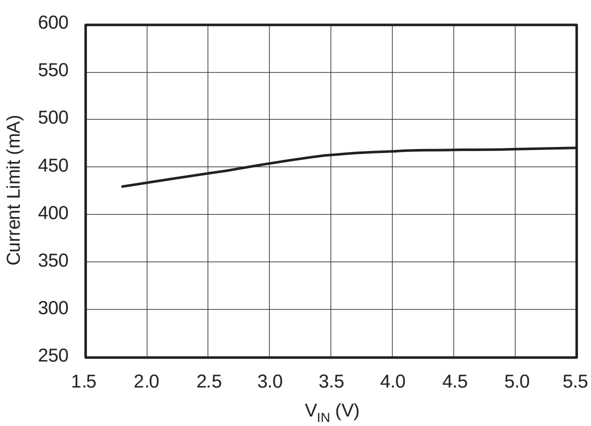


Figure 13.

CURRENT LIMIT vs TEMPERATURE

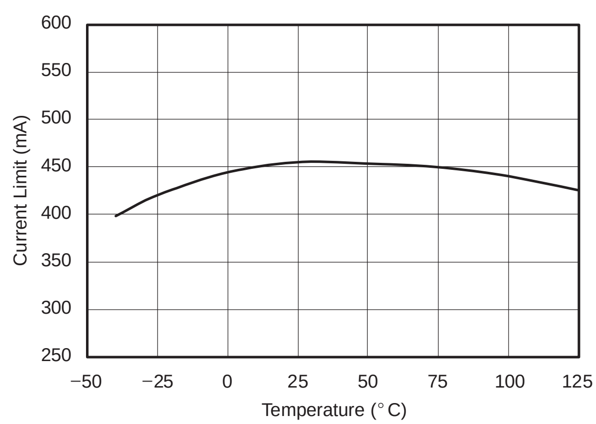


Figure 14.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF, unless otherwise noted.

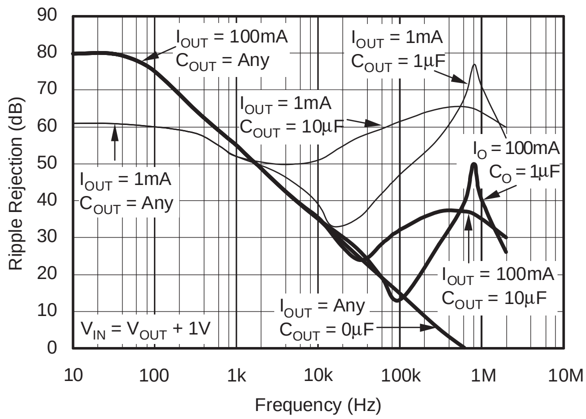


Figure 15.

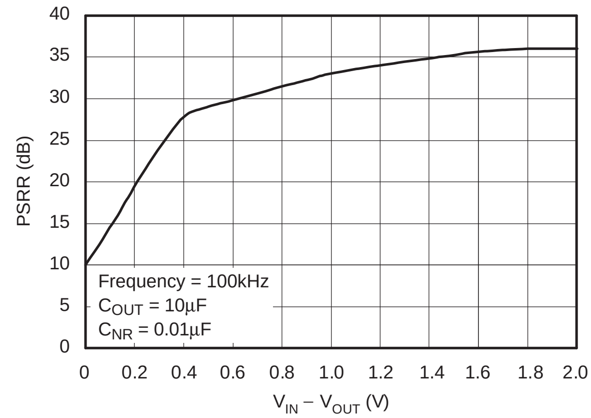


Figure 16.

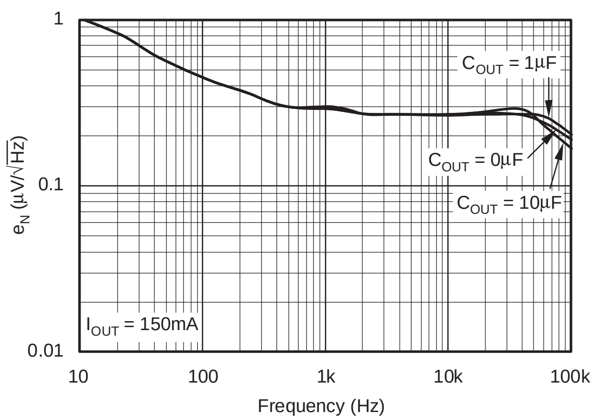


Figure 17.

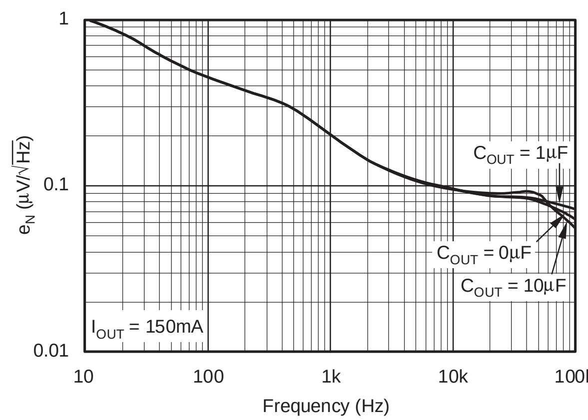


Figure 18.

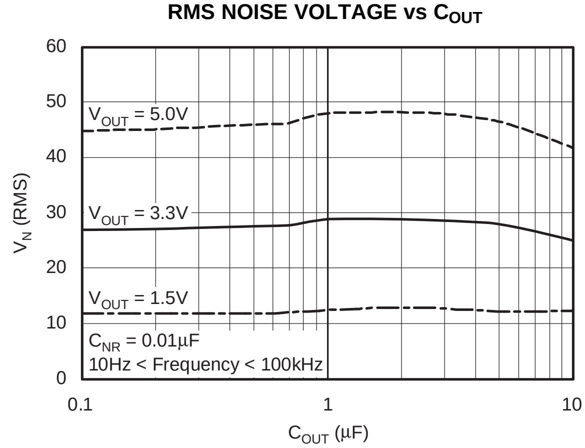


Figure 19.

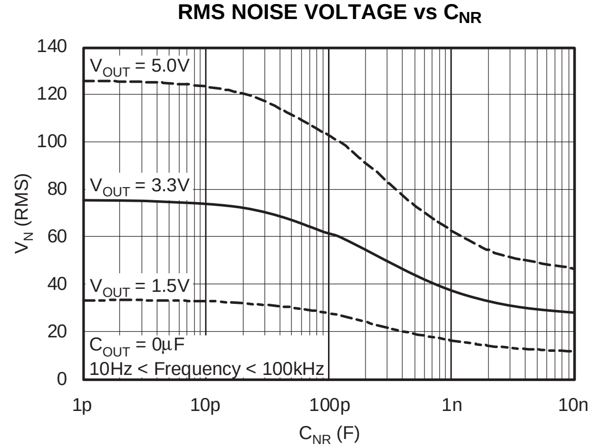


Figure 20.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF, unless otherwise noted.

TPS73233
LOAD TRANSIENT RESPONSE

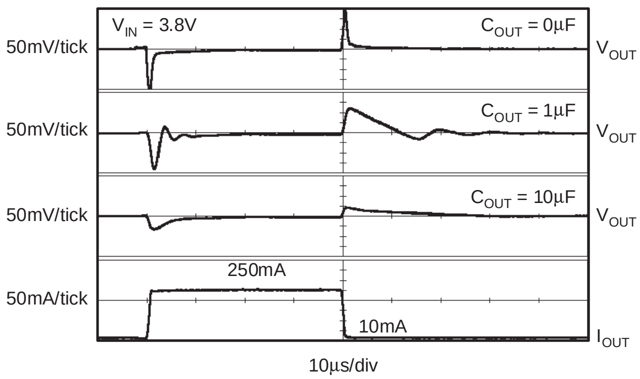


Figure 21.

TPS73233
LINE TRANSIENT RESPONSE

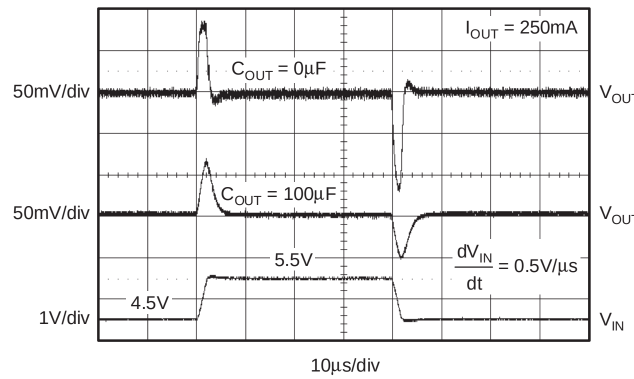


Figure 22.

TPS73233
TURN-ON RESPONSE

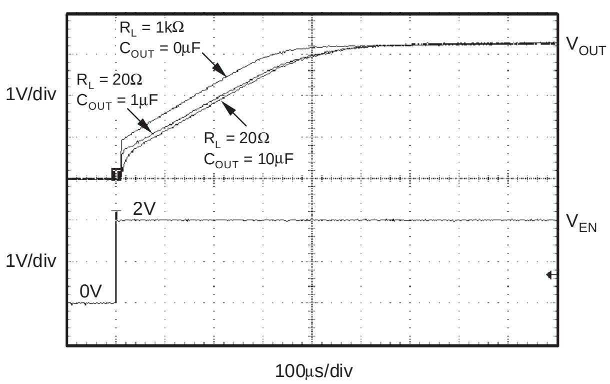


Figure 23.

TPS73233
TURN-OFF RESPONSE

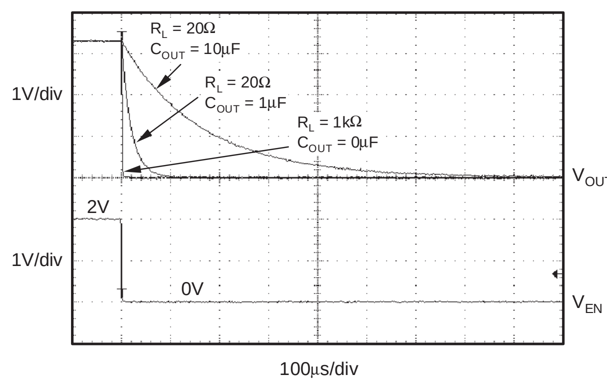


Figure 24.

TPS73233
POWER UP / POWER DOWN

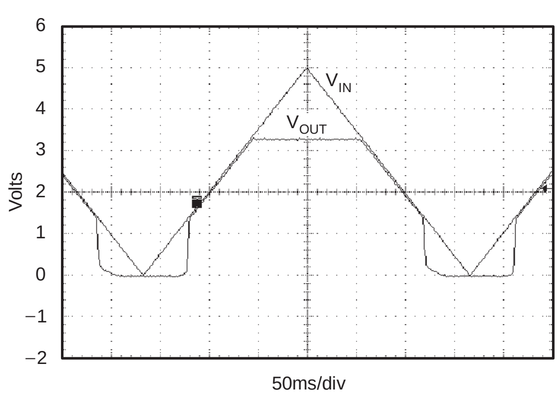


Figure 25.

I_{ENABLE} vs TEMPERATURE

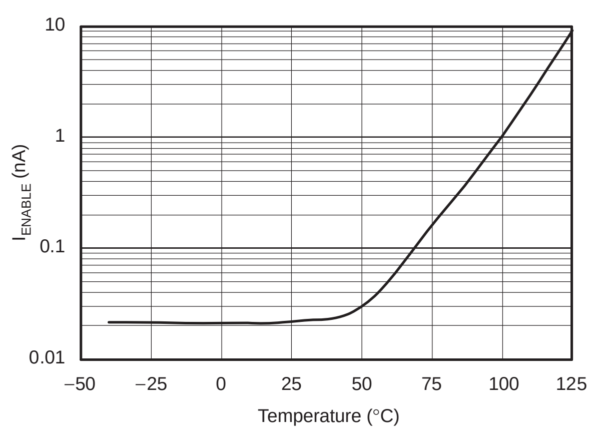


Figure 26.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25°C$, $V_{IN} = V_{OUT(nom)} + 0.5V$, $I_{OUT} = 10mA$, $V_{EN} = 1.7V$, and $C_{OUT} = 0.1\mu F$, unless otherwise noted.

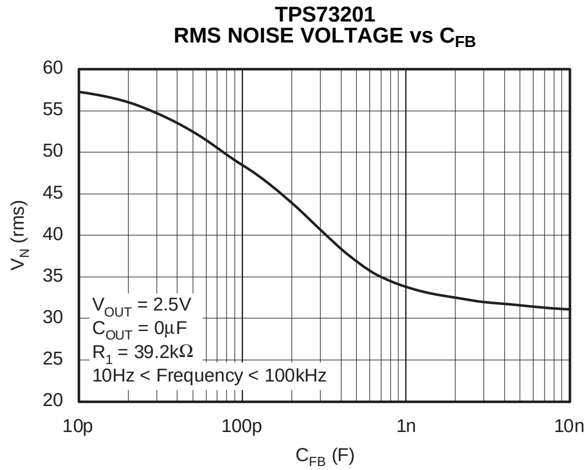


Figure 27.

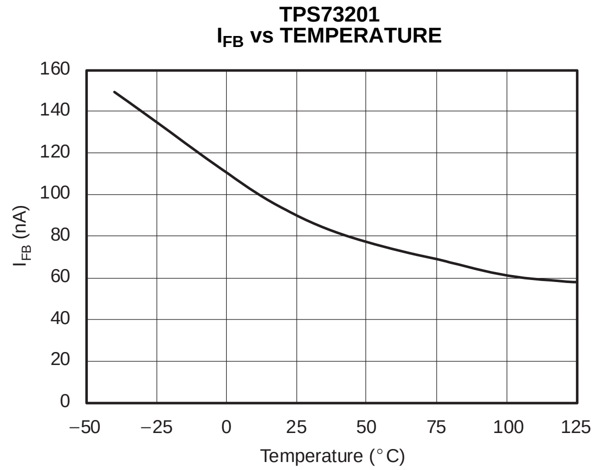


Figure 28.

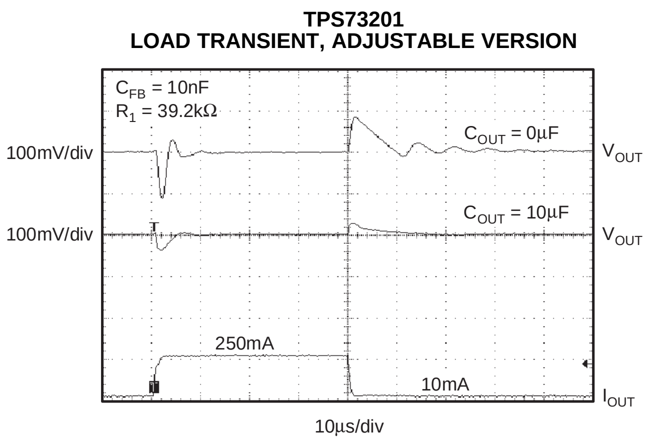


Figure 29.

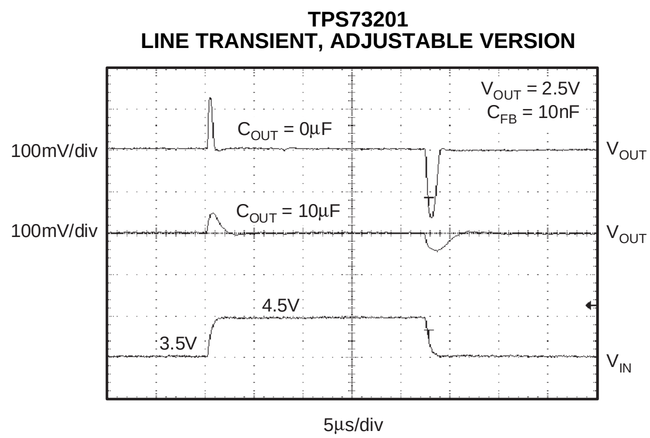


Figure 30.

APPLICATION INFORMATION

The TPS732xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 31 shows the basic circuit connections for the fixed voltage models. Figure 32 gives the connections for the adjustable output version (TPS73201).

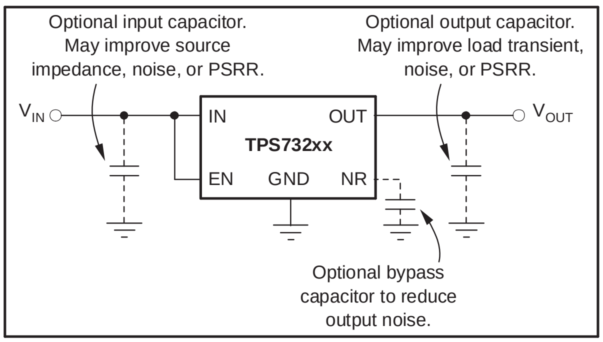


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

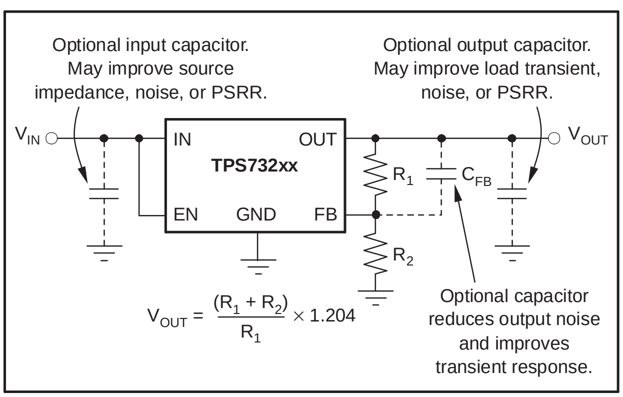


Figure 32. Typical Application Circuit for Adjustable-Voltage Versions

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 32. Sample resistor values for common output voltages are shown in Figure 2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately euqal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amp as the 27kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732xx does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where V_{IN} - V_{OUT} < 0.5V and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

OUTPUT NOISE

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732xx and it generates approximately 32µVRMS (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \qquad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \qquad (2)$$

for the case of no C_{NR}.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

The TPS73201 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the FB pin will reduce output noise and improve load transient performance.

The TPS732xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250µV of switching noise at ~2MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS732xx internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 11 in the Typical Characteristics section for a graph of I_{OUT} vs V_{OUT}.

SHUTDOWN

The Enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5V (max) turns the regulator off and drops the ground pin current to approximately 10nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN}. When a pull-up resistor is used, and operation down to 1.8V is required, use pull-up resistor values below 50 kΩ.

DROPOUT VOLTAGE

The TPS732xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS\text{-}ON}$ of the NMOS pass element.

For large step changes in load current, the TPS732xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} - V_{OUT} above this line insure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} - V_{OUT}) close to dc dropout levels], the TPS732xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the output pin to ground will reduce undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the adjust pin will also improve the transient response.

The TPS732xx does not have active pull-down when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

REVERSE CURRENT

The NMOS pass element of the TPS732xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see Figure 1 and Figure 2).

For the TPS73201, reverse current may flow when V_{FB} is more than 1.0V above V_{IN}.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS732xx into thermal shutdown will degrade device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Power Dissipation Ratings table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

Package Mounting

Solder pad footprint recommendations for the TPS732xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (AB-132), available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS73201DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73201DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73201DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73201DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73201DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73201DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73213DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73213DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73213DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73213DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73215DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73215DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73215DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73215DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73215DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73215DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73215DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73215DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73216DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS73216DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73216DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73216DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73218DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73218DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73218DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73218DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73218DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73218DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73218DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73218DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73225DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73225DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73225DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73225DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73225DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73225DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73225DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73225DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73230DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73230DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73230DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73230DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73230DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
TPS73230DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
TPS73230DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS73230DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
TPS73233DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73233DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73233DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73233DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73233DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73233DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73233DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73233DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73250DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73250DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73250DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73250DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS73250DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73250DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73250DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73250DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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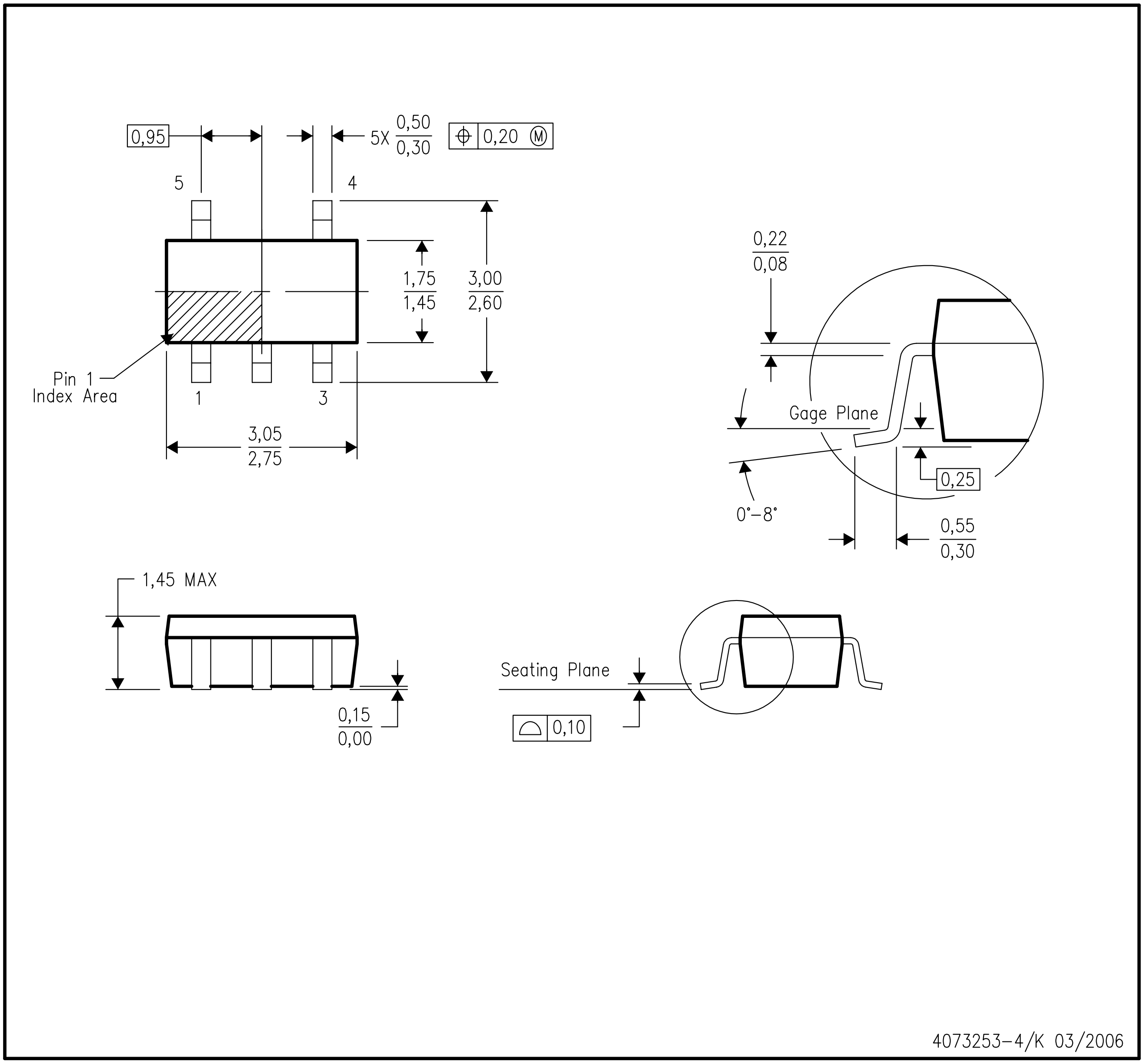
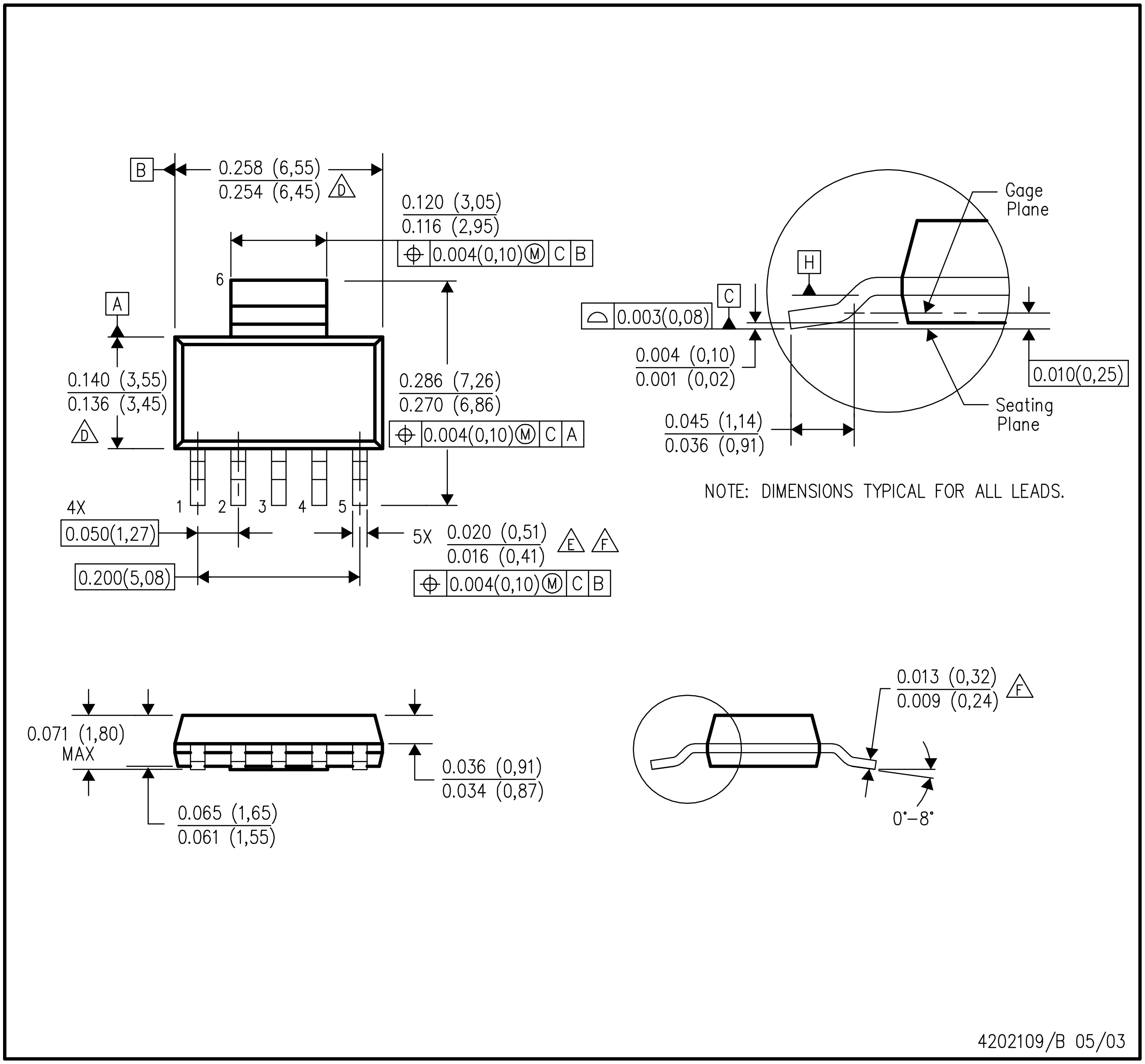
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DCQ (R–PDSO–G6) **PLASTIC SMALL–OUTLINE**



NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Controlling dimension in inches.

D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

E. Lead width dimension does not include dambar protrusion.

F. Lead width and thickness dimensions apply to solder plated leads.

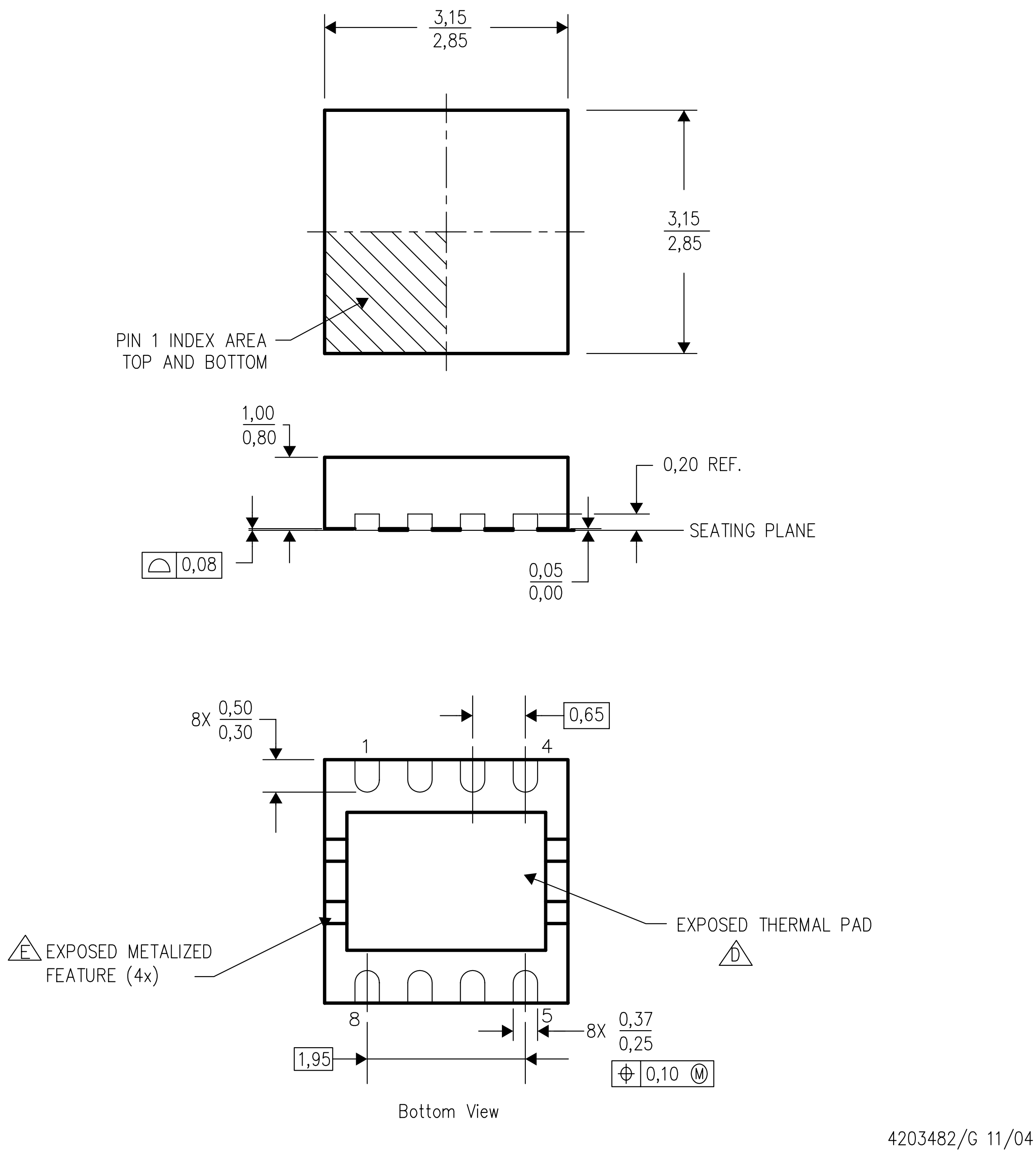
G. Interlead flash allow 0.008 inch max.

H. Gate burr/protrusion max. 0.006 inch.

I. Datums A and B are to be determined at Datum H.

J. Package dimensions per JEDEC outline drawing TO–261, issue B, dated Feb. 1999. This variation is not yet included.

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



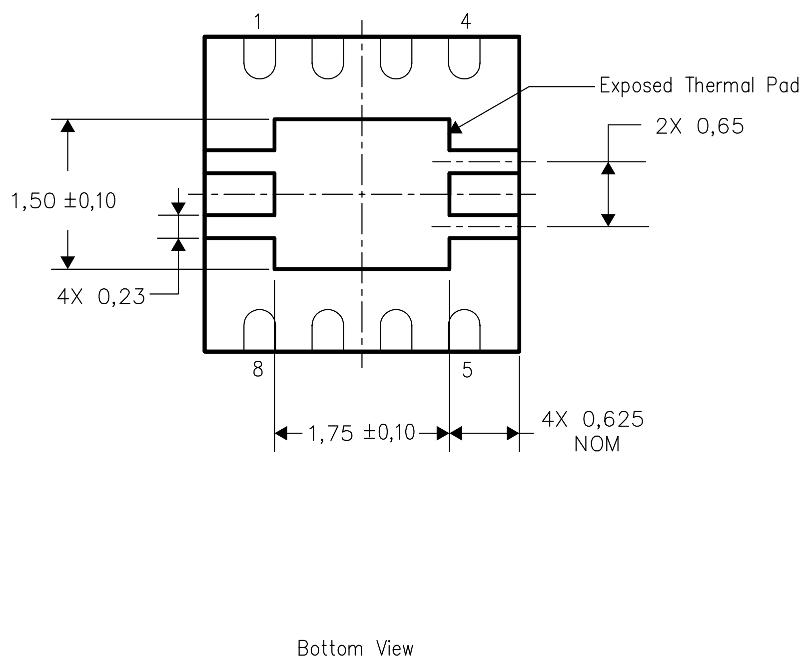
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

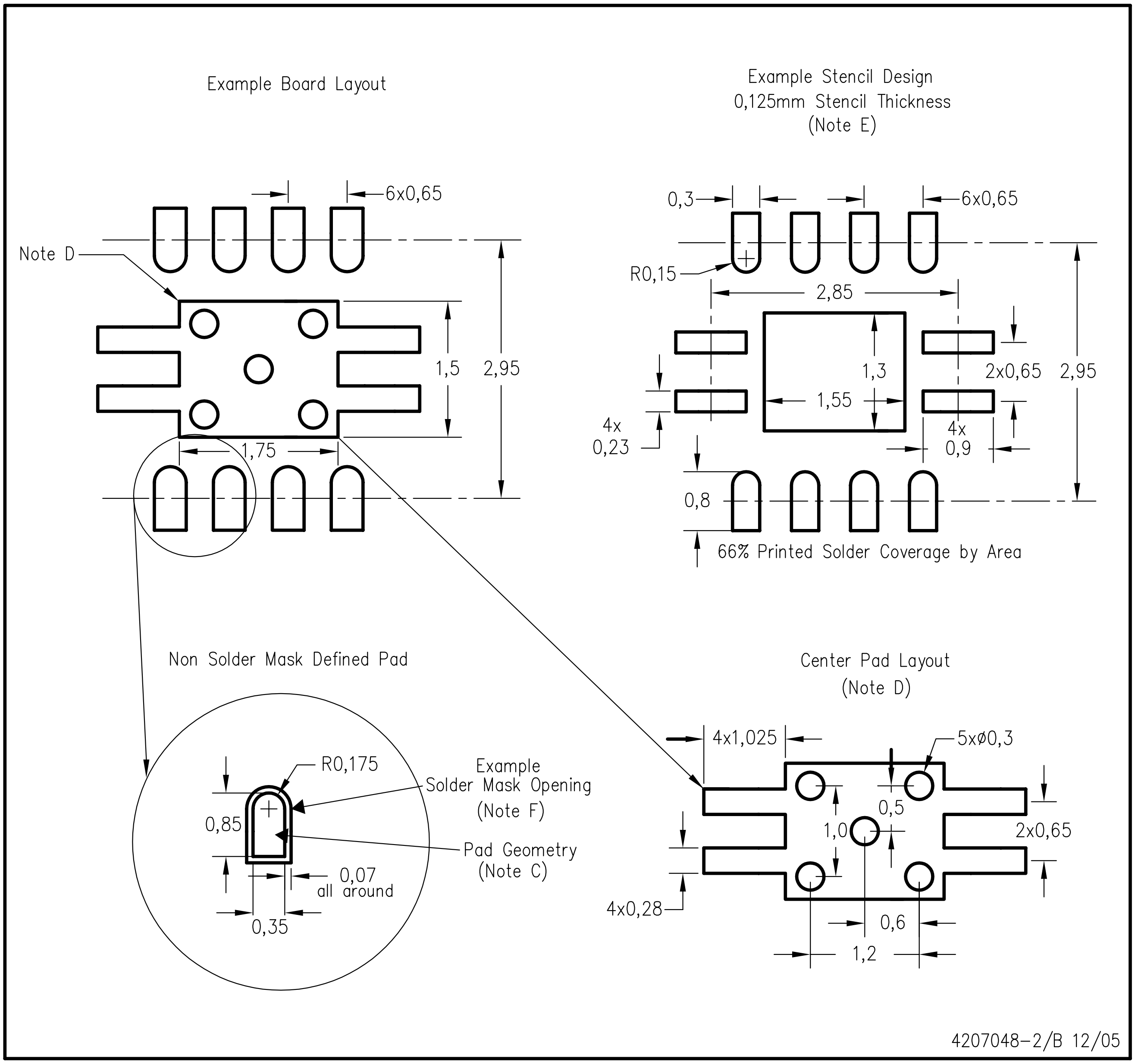
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRB (S-PDSO-N8)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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