National Semiconductor

ADVANCE INFORMATION
January 25, 2008

ADC12EU050
Ultra-Low Power, Octal, 12-bit, 40-50 MSPS Analog-to-Digital Converter

General Description

NOTE: This is Advance Information for a product currently in development. ALL specifications are design targets and are subject to change.

The ADC12EU050 is a 12-bit, ultra-low power, octal A/D converter for use in high performance analog to digital applications. The ADC12EU050 uses an innovative continuous time sigma delta architecture offering ultra low power consumption and an alias free sample bandwidth up to 25MHz. The input stage of each channel features a proprietary system to ensure instantaneous recovery from overdrive. Instant overload recovery (IOR) with no memory effect guarantees the elimination of phase errors resulting from out of range input signals. The ADC12EU050 reduces interconnection complexity by using programmable serialized outputs which offer the industry standard LVDS and SLVS modes. Power consumption of only 44mW per channel(@ 50MSPS) gives a total chip power consumption of 350mW. The ADC12EU050 can operate entirely from a 1.2V supply, although a separate output driver supply of up to 1.8V can be used. The device operates from -40 to +85 °C and is supplied in a 10 x 10 mm^2, 68 pin package.

Features

- CT∑ΔADC architecture with 40-50MSPS throughput
- Anti-alias filter free Nyquist sample range
- Unique Instant Overload Recovery (IOR)
- Wide 2.10 V_{PP} input range
- 1.2V supply voltage
- Integrated precision LC PLL
- Serial control via SPI compatible interface

Key Specifications

Resolution	12 Bits
Conversion Rate	40 to 50 MSPS
SNR	70 dBFS (typ) @ (f_{IN} = 3.5MHz)
THD	–70 dB (typ) @ (f_{IN} = 3.5MHz)
Power Consumption	44 mW/ch (typ) @ 50MSPS
	40 mW/ch (typ) @ 40MSPS
Total Active Power Consumption	350 mW (typ) @ 50MSPS (Equalizer off)
Inter-Channel Isolation	>110 dB @ (f_{IN} = 3.5MHz)
Operating Temp. Range	-40 to +85 °C

Applications

- Battery powered portable systems
- Medical imaging, ultrasound
- Industrial ultrasound, such as non-destructive testing
- Communications

ADC12EU050 Ultra-Low Power, Octal, 12-bit, 40-50 MSPS Analog-to-Digital Converter

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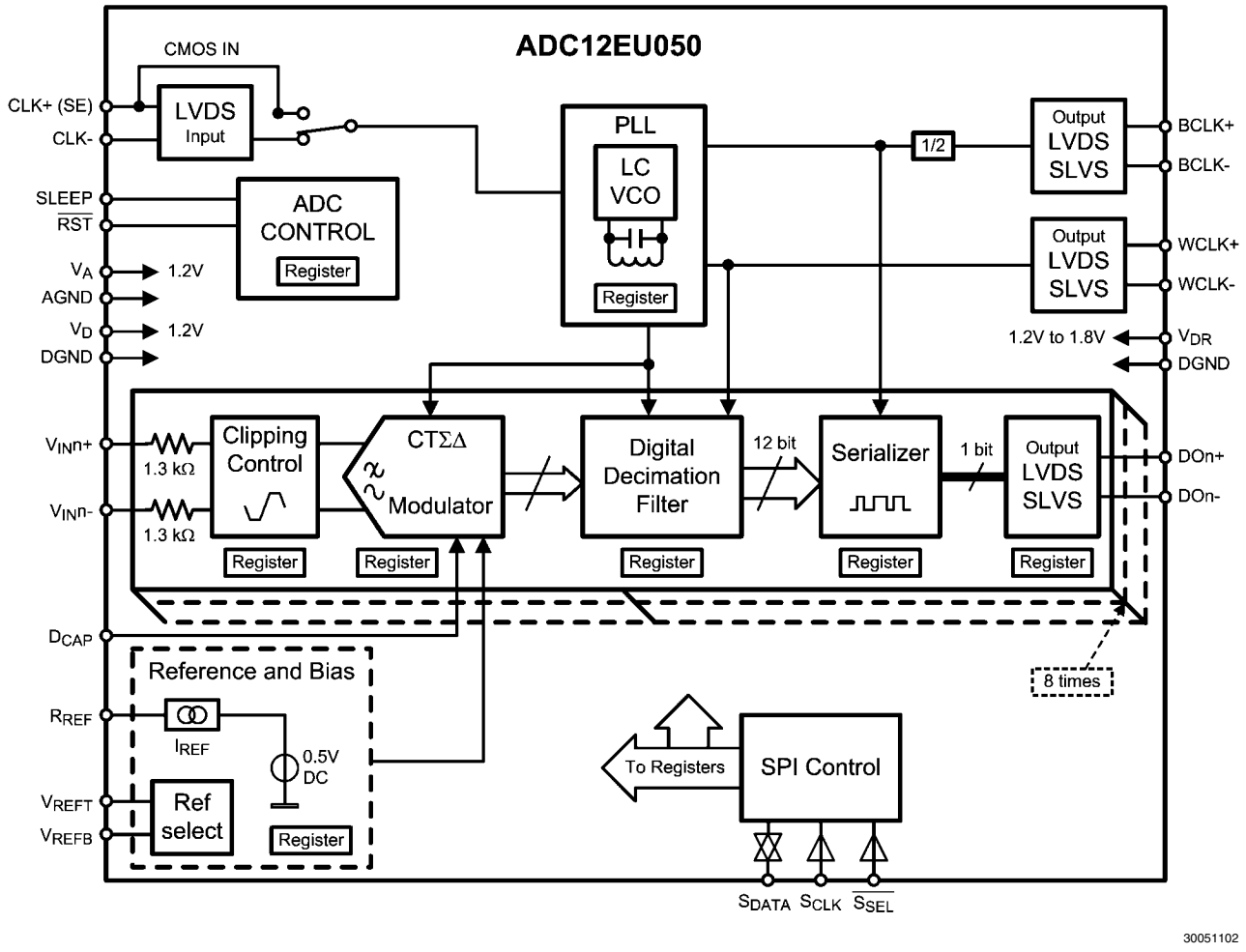
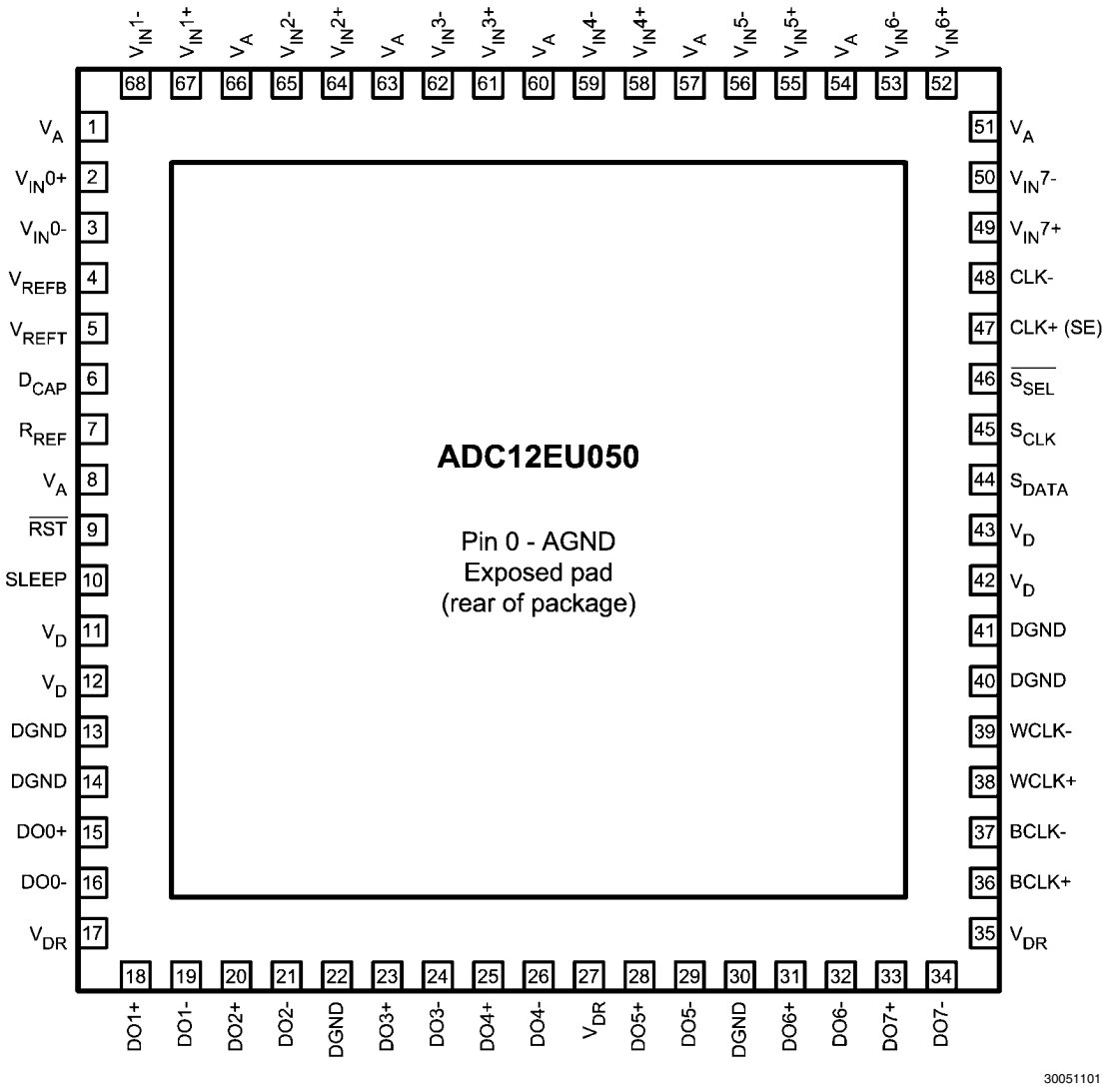
Block Diagram



Connection Diagram



30051101

Ordering Information

Industrial (−40°C ≤ T_A ≤ +85°C)	Package
ADC12EU050CILQ	68 Pin LLP

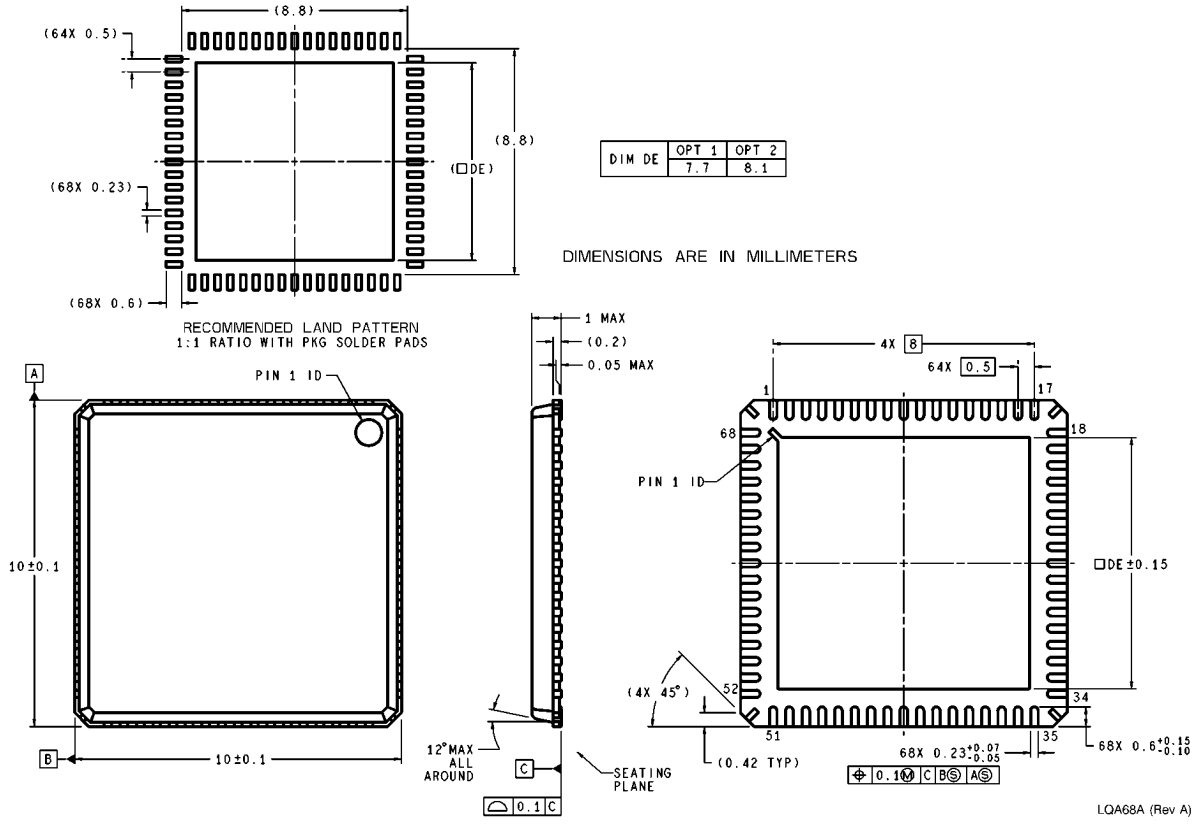
Note: The ADC12EU050 evaluation systems comprise a fully populated & tested device board (DUT), a data capture card with USB 2.0 interface, a SPI control daughter board, Merlin® time and frequency domain measurement software and 2 USB connection cables. The ADC12EU050 evaluation kit is not compatible with National Semiconductor's Wavevision capture board and software.

Pin Descriptions

Pin No.	Name	Type	Function and Connection
ANALOG I/O			
2 3 67 68 64 65 61 62 58 59 55 56 52 53 49 50	$V_{IN}0+$ $V_{IN}0-$ $V_{IN}1+$ $V_{IN}1-$ $V_{IN}2+$ $V_{IN}2-$ $V_{IN}3+$ $V_{IN}3-$ $V_{IN}4+$ $V_{IN}4-$ $V_{IN}5+$ $V_{IN}5-$ $V_{IN}6+$ $V_{IN}6-$ $V_{IN}7+$ $V_{IN}7-$	Input	Differential analog inputs to the ADC, for channels 0 to 7. The negative input pin may be connected to AGND or the inputs may be transformer coupled for single ended operation. A differential input is recommended for best performance.
4	V_{REFB}		Optional negative reference voltage to improve multi-channel ADC matching. If no reference is supplied, this pin must be connected to AGND.
5	V_{REFT}		Optional positive reference voltage to improve multi-channel ADC matching. If using the internal reference, this pin should be left unconnected. If using an external reference voltage, this pin should be connected to the positive reference voltage, which must lie in the range specified in the Electrical Characteristics table.
6	D_{CAP}	Input	This pin provides the capacitance for the low pass filter in the modulator's DAC. It must be connected to AGND through a minimum 100nF capacitor. It is possible to decrease the noise close to the carrier by increasing this capacitor, up to a maximum of 10µF.
7	R_{REF}	Input/Output	External bias reference resistor. This pin must always be connected to AGND through a resistor, whether the internal or an external reference voltage is used. The resistor value must be 10kΩ ±1%.
DIGITAL I/O			
9	$\overline{RST}$	Input	This pin is an active low reset for the entire ADC, both analog and digital components. The pin must be held low for 500ns then returned to high in order to ensure that the chip is reset correctly.
10	SLEEP	Input	Sleep mode. Toggling this pin to high will cause the ADC to enter the low power sleep mode. When the pin is returned to low, the chip will, after the specified time to exit sleep mode, return to normal operation.

Pin No.	Name	Type	Function and Connection
15 16 18 19 20 21 23 24 25 26 28 29 31 32 33 34	DO0+ DO0- DO1+ DO1- DO2+ DO2- DO3+ DO3- DO4+ DO4- DO5+ DO5- DO6+ DO6- DO7+ DO7-	Output	Differential Serial Outputs for channels 0 to 7. Each pair of outputs provides the serial output for the specific channel. The default output is LVDS format, but programming the appropriate control registers, the output format can be changed to SLVS. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100 ohm resistors.
36 37	BCLK+ BCLK-	Output	Bit clock. Differential output clock to be used for sampling the serial outputs. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100 ohm resistors.
38 39	WCLK+ WCLK-	Output	Word Clock. Differential output frame clock. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100 ohm resistors.
44	S_{DATA}	Input/Output	SPI data input and output. This pin is used to send and receive SPI address and data information. The direction of the pin is controlled internally by the ADC based on the SPI protocol.
45	S_{CLK}	Input	SPI clock. In order to use the SPI interface, a clock must be provided on this pin. The maximum frequency of operation for the serial interface is 1MHz.
46	$\overline{S_{SEL}}$	Input	SPI chip select. This active low pin is used to enable the serial interface.
47 48	CLK+ (SE) CLK-	Input	Differential Input Clock. The input clock must lie in the range of 40MHz to 50MHz. It is used by the PLL to generate the internal sampling clocks. A single ended clock can also be used, and should be connected to pin 47.
POWER SUPPLY			
1, 8, 51, 54, 57, 60, 63, 66	V_A	Power	Analog Power Supply. All pins should be connected to the same 1.2V supply, with voltage limits as in the Electrical Specification.
0	AGND	Ground	Analog Ground Return.
11, 12, 42, 43	V_D	Power	Digital Power Supply. Connect to 1.2V, with voltage limits as in the Electrical Specification.
13, 14, 22, 30, 40, 41	DGND	Ground	Digital and Output Driver Ground Return.
17, 27, 35	V_{DR}	Power	Output Driver Power Supply. Can be connected to 1.2V – 1.8V, depending on application requirements. Voltage limits are described in more detail in the Electrical Specification.

Physical Dimensions inches (millimeters) unless otherwise noted



TOP View.....SIDE View.....BOTTOM View
68-Lead LLP Package 10x10x1.0mm, 0.5mm Pitch
Ordering Numbers ADC12EU050CILQ
NS Package Number LQA68A

Notes

Notes

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