

TC74LVX138F, TC74LVX138FN, TC74LVX138FT

3-TO-8 LINE DECODER

The TC74LVX138 is a high speed CMOS 3-TO-8 LINE DECODER fabricated with silicon gate C²MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\overline{Y}0$ - $\overline{Y}7$) will go low.

When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

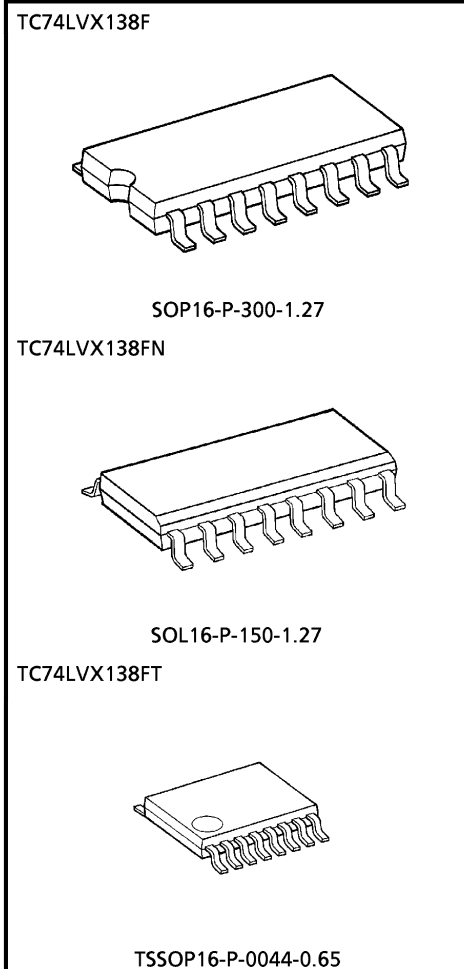
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage.

This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

- High speed : $t_{pd} = 5.5ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) ($T_a = 25^\circ C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
 $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \approx t_{pHL}$
- Low noise : $V_{OLP} = 0.5V$ (Max.)
- Pin and function compatible with 74HC138

(Note) The JEDEC SOP (FN) is not available in Japan.

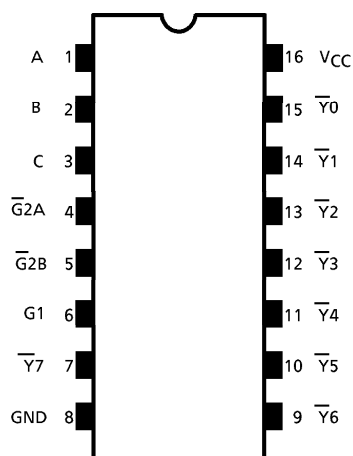


Weight
 SOP16-P-300-1.27 : 0.18g (Typ.)
 SOL16-P-150-1.27 : 0.12g (Typ.)
 TSSOP16-P-0044-0.65 : 0.06g (Typ.)

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PIN ASSIGNMENT



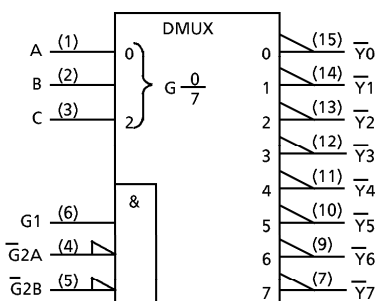
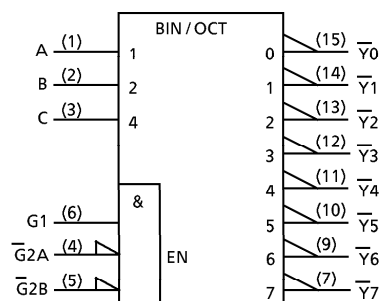
(TOP VIEW)

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
G1	G2A	G2B	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	Y0
H	L	L	L	L	H	H	L	H	H	H	H	H	H	Y1
H	L	L	L	H	L	H	H	L	H	H	H	H	H	Y2
H	L	L	L	H	H	H	H	H	L	H	H	H	H	Y3
H	L	L	H	L	L	H	H	H	H	L	H	H	H	Y4
H	L	L	H	L	H	H	H	H	H	H	L	H	H	Y5
H	L	L	H	H	L	H	H	H	H	H	H	L	H	Y6
H	L	L	H	H	H	H	H	H	H	H	H	H	L	Y7

X : Don't Care

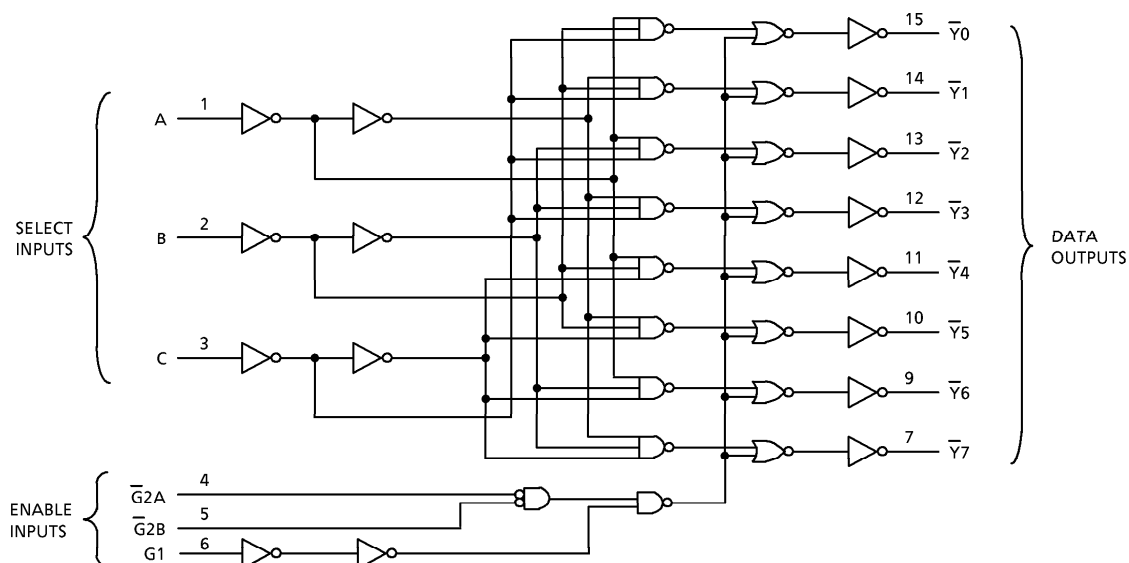
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM- BOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = - 40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	“H” Level	V _{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	“L” Level	V _{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 50μA	2.0	1.9	2.0	—	1.9	—	V
				I _{OH} = - 50μA	3.0	2.9	3.0	—	2.9	—	
				I _{OH} = - 4mA	3.0	2.58	—	—	2.48	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I _{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I _{OL} = 4mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current		I _{IN}	V _{IN} = 5.5V or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC characteristics (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM- BOL	TEST CONDITION			Ta = 25°C			Ta = - 40~85°C		UNIT
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, C- $\bar{Y}$)	t _{pLH}		2.7	15	—	7.1	13.8	1.0	16.5	ns
				50	—	9.6	17.3	1.0	20.0	
	t _{pHL}		3.3 ± 0.3	15	—	5.5	8.8	1.0	10.5	
				50	—	8.0	12.3	1.0	14.0	
Propagation Delay Time (G1- $\bar{Y}$)	t _{pLH}		2.7	15	—	8.7	16.3	1.0	19.5	ns
				50	—	11.2	19.8	1.0	23.0	
	t _{pHL}		3.3 ± 0.3	15	—	6.8	10.6	1.0	12.5	
				50	—	9.3	14.1	1.0	16.0	
Propagation Delay Time ($\bar{G}2$ - $\bar{Y}$)	t _{pLH}		2.7	15	—	8.8	16.0	1.0	18.5	ns
				50	—	11.3	19.5	1.0	22.0	
	t _{pHL}		3.3 ± 0.3	15	—	6.9	10.4	1.0	11.5	
				50	—	9.4	13.9	1.0	15.0	
Output To Output Skew	t _{osLH}	(Note 1)	2.7	50	—	—	2.5	—	2.5	ns
	t _{osHL}		3.3 ± 0.3	50	—	—	2.5	—	2.5	
Input Capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 3)			—	34	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

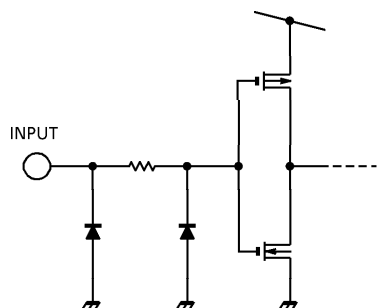
Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3\text{ns}$, C_L = 50pF)

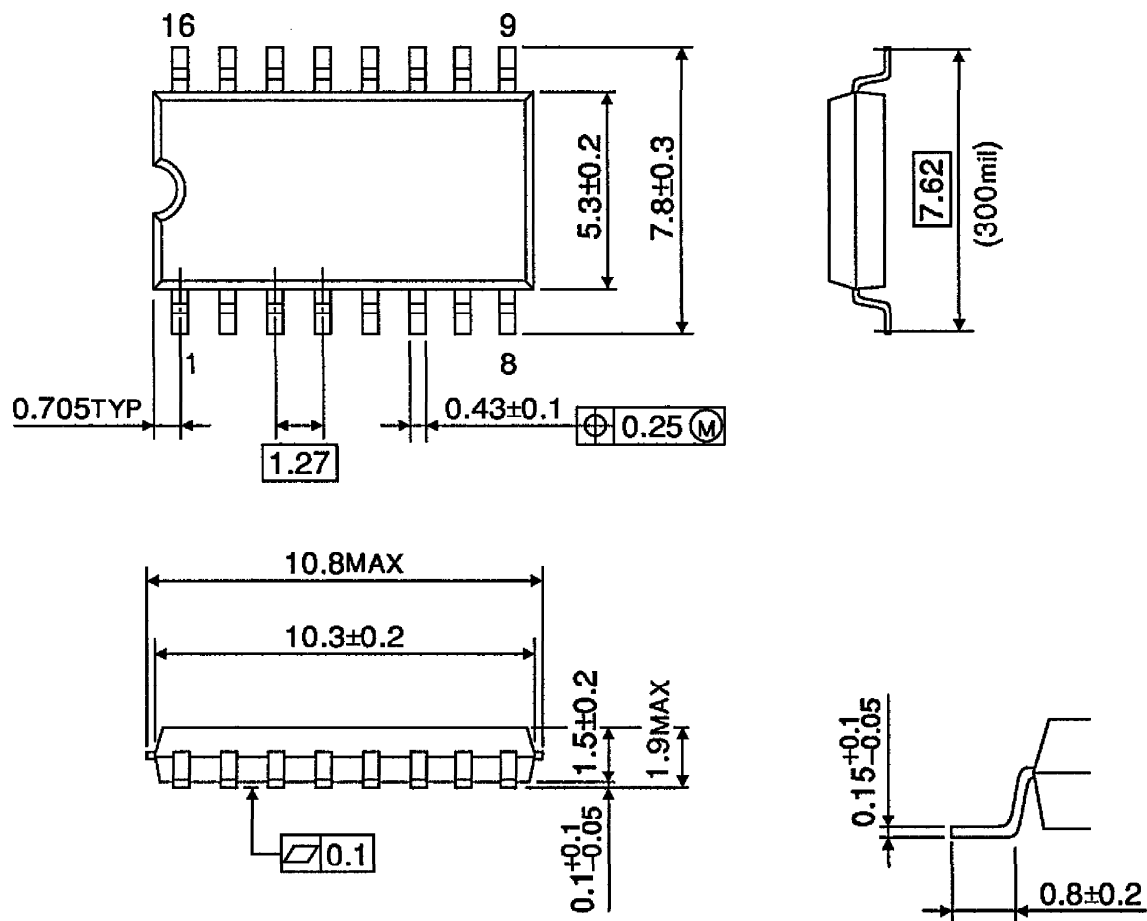
PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}		3.3	—	0.5	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}		3.3	—	-0.5	V
Minimum High Level Dynamic Input Voltage	V _{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SOP16-P-300-1.27

Unit : mm



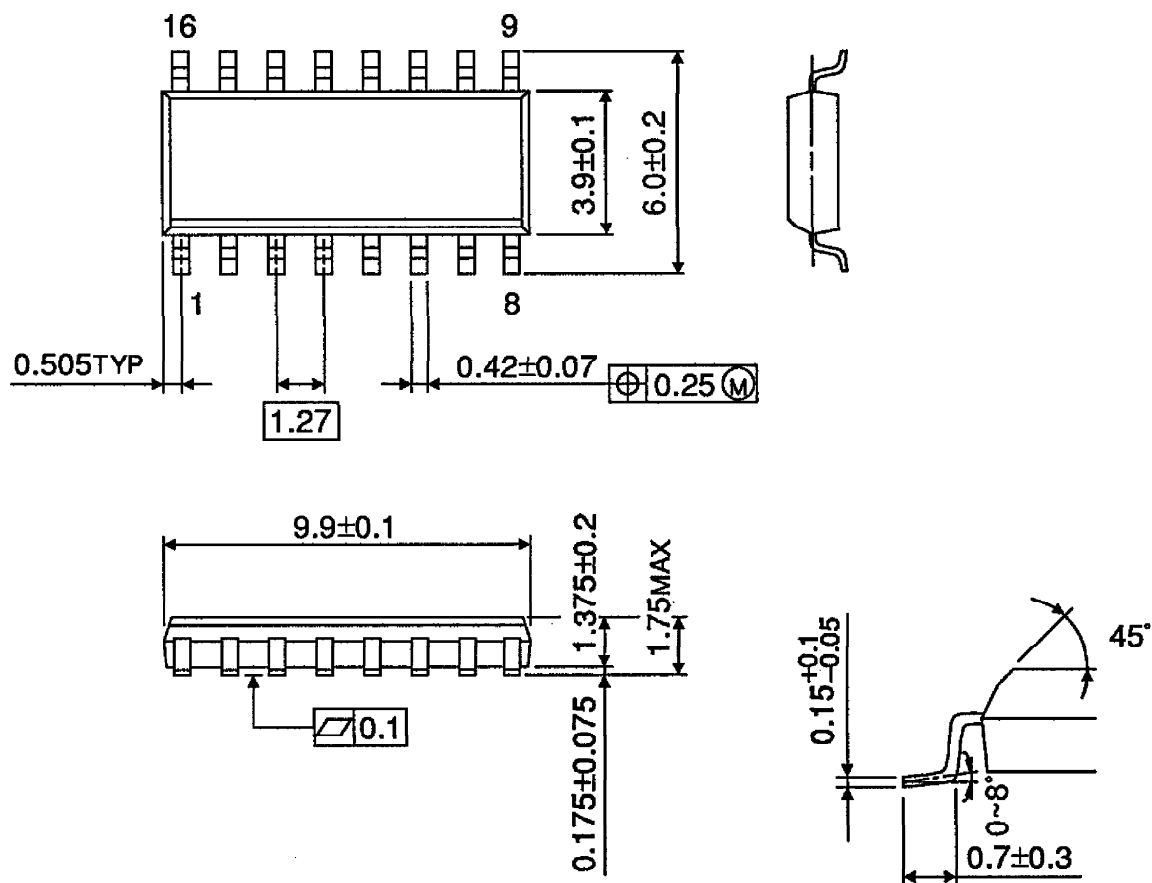
Weight : 0.18g (Typ.)

OUTLINE DRAWING

SOL16-P-150-1.27

Unit : mm

(Note) This package is not available in Japan.

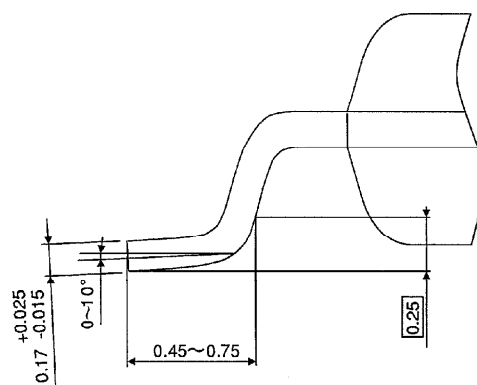
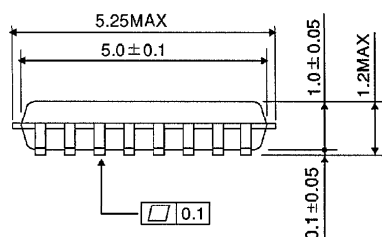
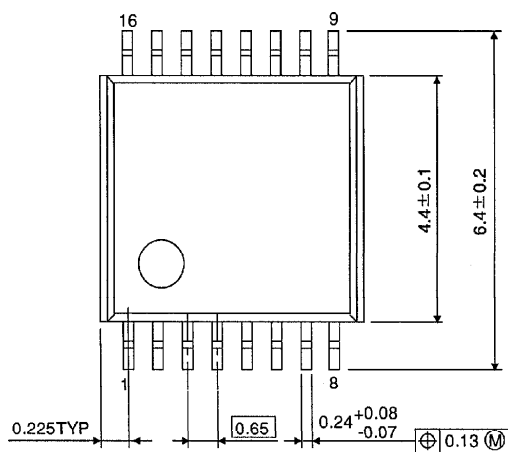


Weight : 0.12g (Typ.)

OUTLINE DRAWING

TSSOP16-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)