

## TC74LVX273F, TC74LVX273FT

### Octal D-Type Flip-Flop with Clear

The TC74LVX273F/ FT is a high-speed CMOS octal D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

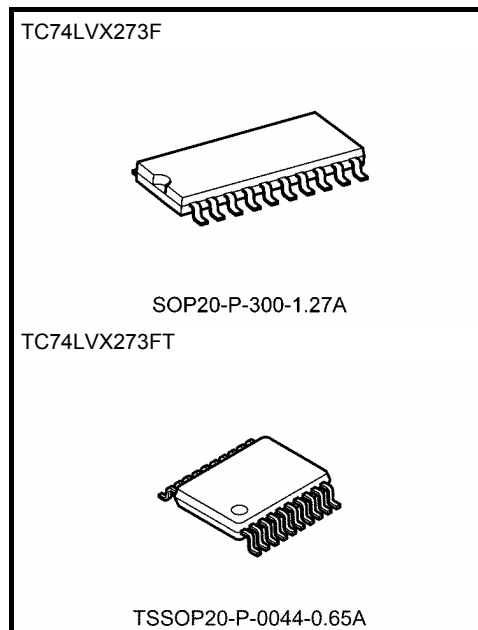
This device is suitable for low-voltage and battery operated systems.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. When the  $\overline{\text{CLR}}$  input is held low, the Q outputs are in the low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

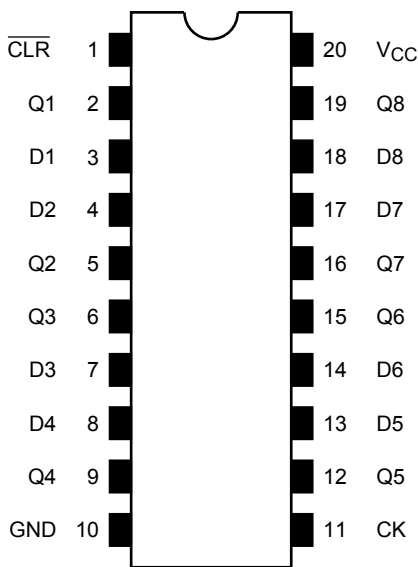
- High-speed:  $f_{\text{max}} = 150 \text{ MHz}$  (typ.) ( $V_{\text{CC}} = 3 \text{ V}$ )
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) ( $T_a = 25^\circ\text{C}$ )
- Input voltage level:  $V_{\text{IL}} = 0.8 \text{ V}$  (max) ( $V_{\text{CC}} = 3 \text{ V}$ )  
 $V_{\text{IH}} = 2.0 \text{ V}$  (min) ( $V_{\text{CC}} = 3 \text{ V}$ )
- Power-down protection provided on all inputs
- Balanced propagation delays:  $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Low noise:  $V_{\text{OLP}} = 0.8 \text{ V}$  (max)
- Pin and function compatible with 74HC273



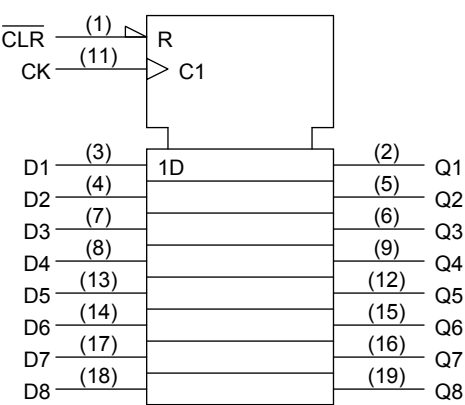
#### Weight

SOP20-P-300-1.27A	: 0.22 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol

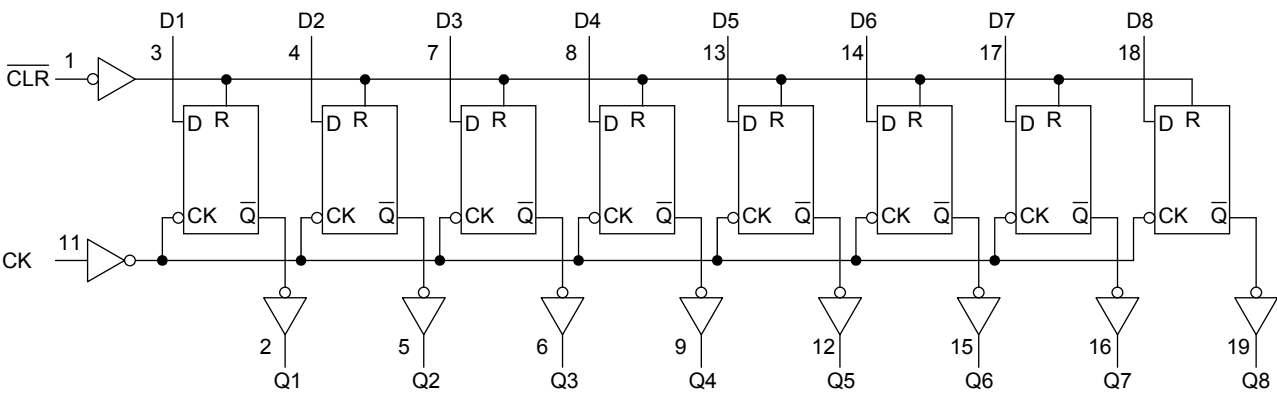


Truth Table

Inputs			Outputs	Function
CLR	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Q <sub>n</sub>	No change

X: Don't care

System Diagram



## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 3.6	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$dt/dv$	0 to 100	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

## DC Characteristics

Characteristics		Sym- bol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
					V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Input voltage	H-level	V <sub>IH</sub>	—	2.0	1.5	—	—	1.5	—	V	
				3.0	2.0	—	—	2.0	—		
				3.6	2.4	—	—	2.4	—		
	L-level	V <sub>IL</sub>	—	2.0	—	—	0.5	—	0.5		
				3.0	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	—	2.9	—	
				I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0	0.1	—	0.1	
				I <sub>OL</sub> = 50 μA	3.0	—	0	0.1	—	0.1	
				I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	3.6	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	—	—	4.0	—	40.0	μA	

Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			VCC (V)	Limit	Limit	
Minimum pulse width (CK)	tW (L)	—	2.7	8.0	9.5	ns
	tW (H)		3.3 ± 0.3	5.5	6.5	
Minimum pulse width ( $\overline{\text{CLR}}$ )	tW (L)	—	2.7	7.5	8.5	ns
			3.3 ± 0.3	5.0	6.0	
Minimum set-up time	ts	—	2.7	8.0	9.5	ns
			3.3 ± 0.3	5.5	6.5	
Minimum hold time	th	—	2.7	1.0	1.0	ns
			3.3 ± 0.3	1.0	1.0	
Minimum removal time ( $\overline{\text{CLR}}$ )	trem	—	2.7	4.0	4.0	ns
			3.3 ± 0.3	2.5	2.5	

**AC Characteristics (input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t <sub>pLH</sub>	—	2.7	15	—	9.0	16.9	1.0	20.5	ns
				50	—	11.5	20.4	1.0	24.0	
	t <sub>pHL</sub>		3.3 ± 0.3	15	—	7.1	11.0	1.0	13.0	
				50	—	9.6	14.5	1.0	16.5	
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	t <sub>pHL</sub>	—	2.7	15	—	9.3	17.6	1.0	20.5	ns
				50	—	11.8	21.1	1.0	24.0	
			3.3 ± 0.3	15	—	7.3	11.5	1.0	13.5	
				50	—	9.8	15.0	1.0	17.0	
Maximum clock frequency	f <sub>max</sub>	—	2.7	15	55	110	—	45	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	95	150	—	80	—	
				50	60	90	—	50	—	
Output to output skew	t <sub>osLH</sub>	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t <sub>osHL</sub>		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C <sub>IN</sub>	(Note 2)			—	4	10	—	10	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note 3)			—	31	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Note 2: Parameter guaranteed by design.

Note 3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

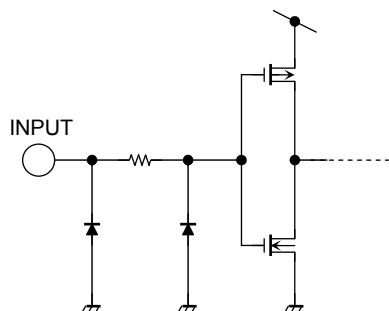
And the total C<sub>PD</sub> when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 22 + 9 \cdot n$$

## Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	—	3.3	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	—	3.3	-0.5	-0.8	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	—	3.3	—	0.8	V

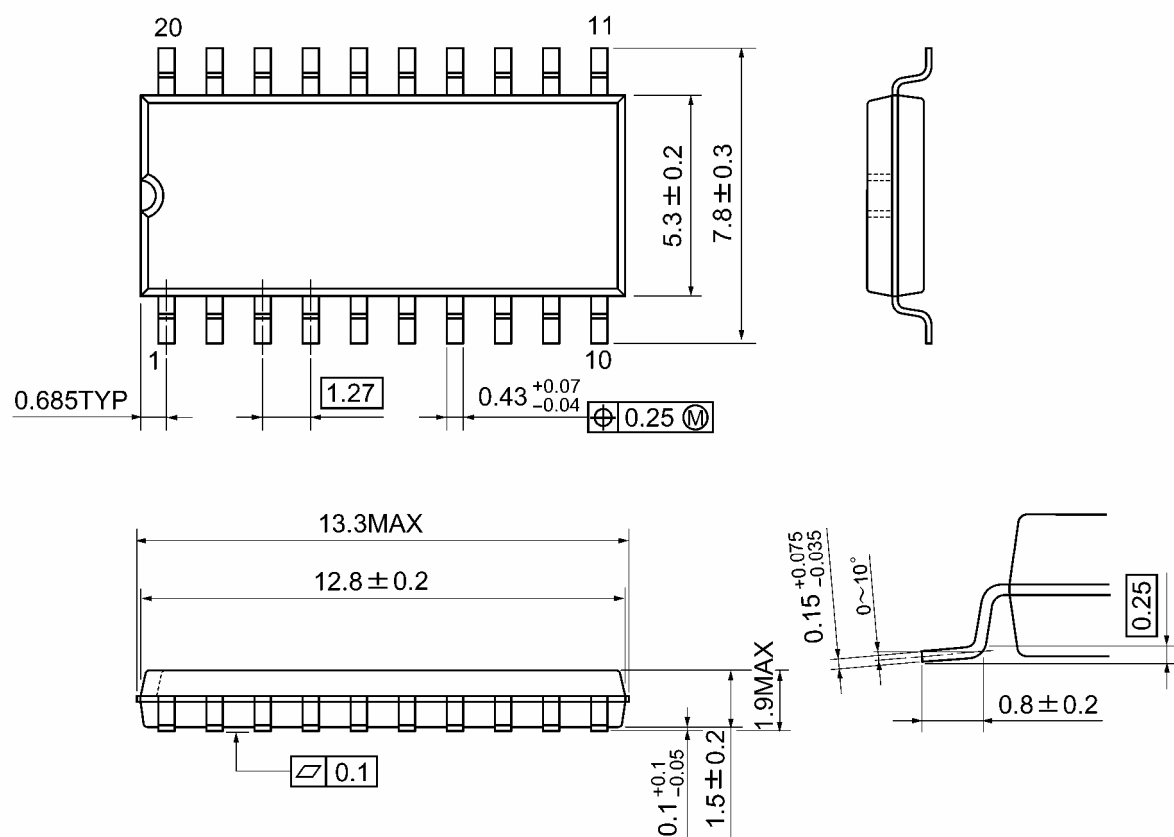
## Input Equivalent Circuit



## Package Dimensions

SOP20-P-300-1.27A

Unit: mm

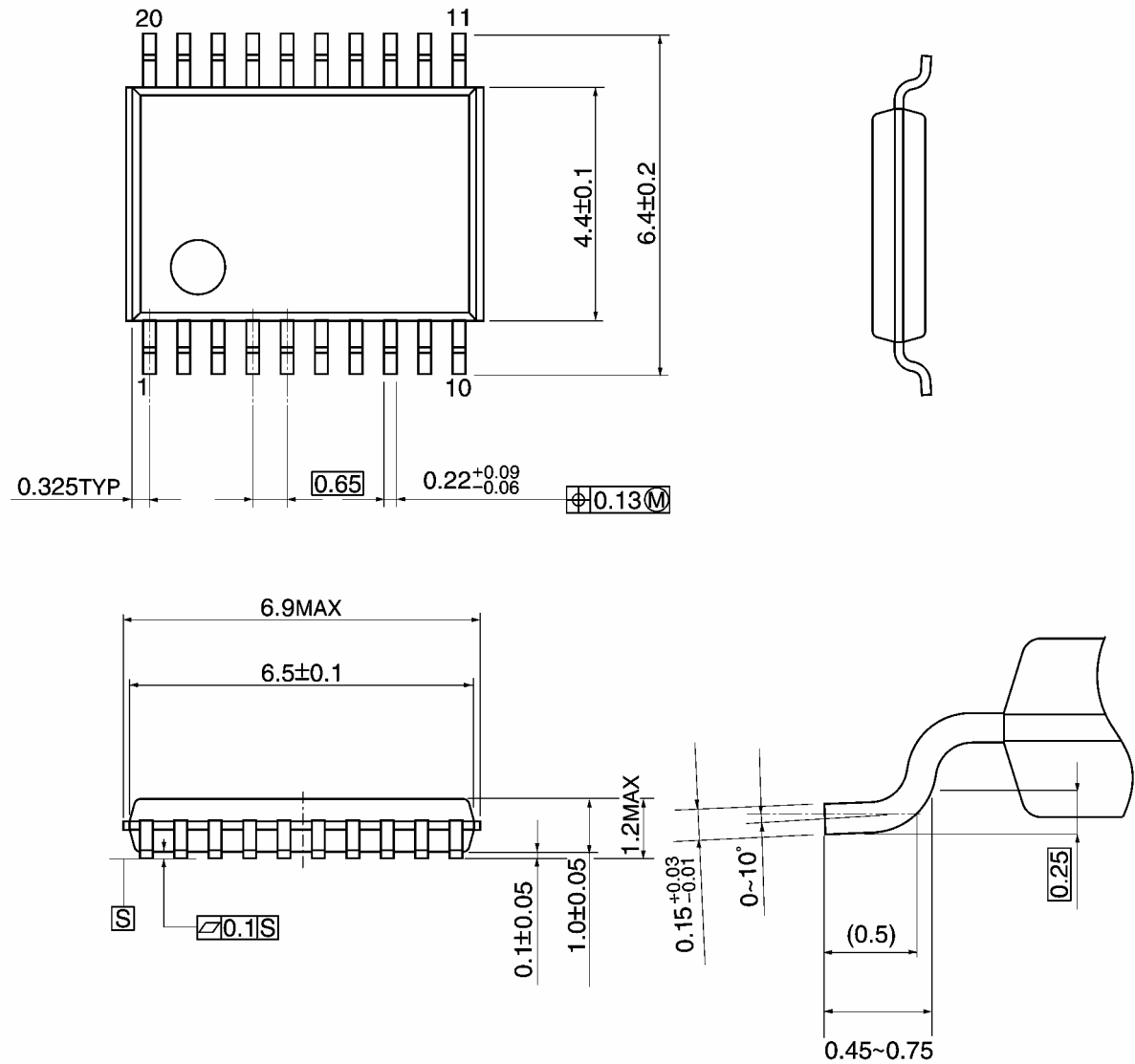


Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

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20070701-EN GENERAL

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