SY10/100EP451L

3.3V ECL 6-Bit Differential Register with Master Reset

General Description

The SY10/100EP451L is a 6-bit fully differential register with common clock and single-ended Master Reset (MR). It is ideal for very high frequency applications where a registered data path is necessary.

All inputs have an internal 75kΩ pull-down resistor. Differential inputs have an override clamp. Unused differential register inputs can be left open and will default LOW. When the differential inputs are forced to < V_{EE} +1.2V, the clamp will override and force the output to a default state.

The positive transition of CLK (pin 4) will latch the registers. Master Reset (MR) HIGH will asynchronously reset all registers forcing Q outputs to go LOW.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

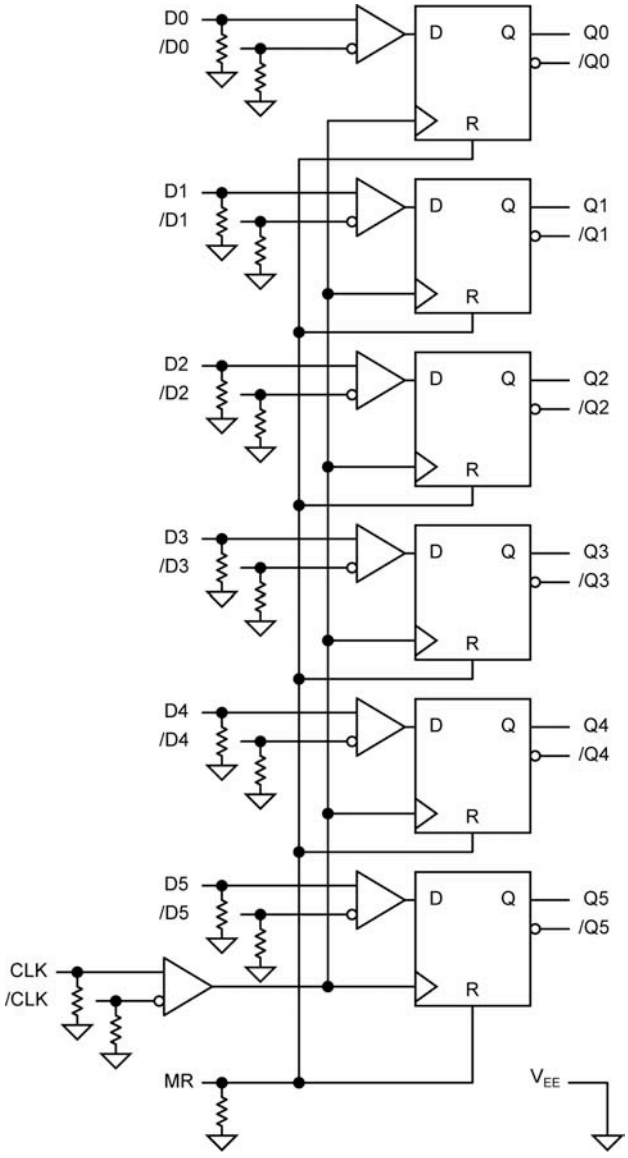
Features

- 450ps typical propagation delay
- Maximum frequency > 3.0GHz typical
- Asynchronous Master Reset
- 20ps skew within device, 35ps skew device-to-device
- PECL mode operating range:
  - V_{CC} = 3.0V to 3.6V with V_{EE} = 0V
- NECL mode operating range:
  - V_{CC} = 0V with V_{EE} = –3.0V to –3.6V
- Open input default state
- Safety clamp on inputs
- Available in 32-pin TQFP

Applications

- High Speed Logic
- Wireless Communication Systems
- Data Communication Systems

Logic Diagram



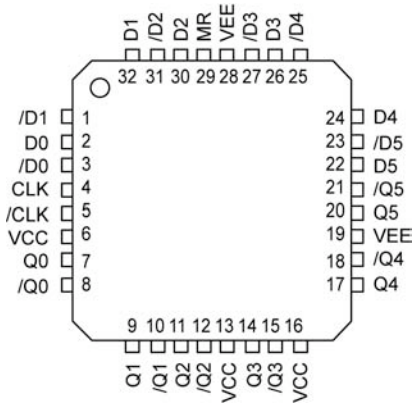
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EP451LTG	T32-1	Industrial	SY10EP451LTG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP451LTGTR[2]	T32-1	Industrial	SY10EP451LTG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP451LTG	T32-1	Industrial	SY100EP451LTG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP451LTGTR[2]	T32-1	Industrial	SY100EP451LTG with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin TQFP (T32-1)

hbwhelp@micrel.com or (408) 955-1690

Pin Description

Pin Number	Pin Name	Pin Function
2, 3	D0, /D0	ECL Differential Data Inputs: These input pairs are the different data signal inputs to the device. Each input pin is connected to a 75kΩ pull-down resistor. Due to an internal clamping circuit, D will default LOW and /D will default HIGH if left open.
32, 1	D1, /D1	
30, 31	D2, /D2	
26, 27	D3, /D3	
24, 25	D4, /D4	
22, 23	D5, /D5	
29	MR	ECL Master Reset Input pin. If input pin is left open, it will default to LOW.
4, 5	CLK, /CLK	ECL Differential Clock Input: This input pair is the clock signal input to the device. Each input pin is connected to a 75kΩ pull-down resistor. Due to an internal clamping circuit, CLK will default LOW and /CLK will default HIGH if left open.
7, 8	Q0, /Q0	ECL Differential Data Outputs: Q defaults to LOW and /Q defaults to HIGH if D inputs are left open. See “LVPECL Output Interface Applications” section for recommendations on terminations.
9, 10	Q1, /Q1	
11, 12	Q2, /Q2	
14, 15	Q3, /Q3	
17, 18	Q4, /Q4	
20, 21	Q5, /Q5	
6, 13, 16	VCC	Positive Supply: Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
19, 28	VEE	Negative Power Supply: V_{EE} must be tied to most negative supply.

Absolute Maximum Ratings[1]

Supply Voltage
- PECL Mode (V_{CC}) ..... +4V
- NECL Mode (V_{EE}) ..... –4V

Input Voltage (V_{IN})
- PECL Mode ..... V_{CC}
- NECL Mode ..... V_{EE}

Output Current (I_{OUT})
- Continuous 50mA
- Surge 100mA

Lead Temperature (soldering, 20sec.) ..... 260°C

Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC})
- PECL Mode (V_{EE} =0V)…… +3.0V to +3.6V

Supply Voltage (V_{EE})
- NECL Mode (V_{CC} =0V)…… -3.0V to -3.6V

Ambient Temperature (T_A) ..... –40°C to +85°C

Junction Thermal Resistance[3]
- TQFP
- Junction-to-Ambient (θ_{JA})
  - 0lfpm ..... 80°C/W
  - 500lfpm ..... 66°C/W
- Junction-to-Case (θ_{JC}) ..... 20°C/W

PECL 10EP DC Electrical Characteristics[4](*Preliminary*)

V_{CC} = 3.3V; V_{EE} = 0V; T_A = –40°C to +85°C, unless otherwise stated.[5]

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		80	105		80	105		80	105	mA
V_{OH}	Output HIGH Voltage[6]	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage[6]	1365	1490	1615	1430	1555	1680	1470	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration)[7]	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NECL 10EP DC Electrical Characteristics[4](*Preliminary*)

V_{CC} = 0V; V_{EE} = –3.0V to –3.6V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		80	105		80	105		80	105	mA
V_{OH}	Output HIGH Voltage[6]	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage[6]	-1935	-1810	-1685	-1870	-1745	-1620	-1830	-1685	-1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration)[7]	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. θ_{JA} and θ_{JC} values are determined for a 4-layer board in still-air unless otherwise stated.
4. The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specifications limit values are applied individually under normal operating conditions and not valid simultaneously.
5. Input and output parameters vary 1:1 with V_{CC}.
6. All loading with 50Ω to V_{CC}–2.0V.
7. V_{IHCMR} (min) varies 1:1 with V_{EE}, V_{IHCMR} (max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

PECL 100EP DC Electrical Characteristics[8]

V_{CC} = 3.3V; V_{EE} = 0V; T_A = –40°C to +85°C, unless otherwise stated.[9]

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		85	120		85	120		85	120	mA
V_{OH}	Output HIGH Voltage[10]	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage[10]	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration)[11]	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NECL 100EP DC Electrical Characteristics[8]

V_{CC} = 0V; V_{EE} = –3.0V to –3.6V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		85	120		85	120		85	120	mA
V_{OH}	Output HIGH Voltage[10]	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage[10]	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration)[11]	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V_{EE} +2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

Notes:

8. The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specifications limit values are applied individually under normal operating conditions and not valid simultaneously.
9. Input and output parameters vary 1:1 with V_{CC}.
10. All loading with 50Ω to V_{CC}–2.0V.
11. V_{IHCMR} (min) varies 1:1 with V_{EE}, V_{IHCMR} (max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC Electrical Characteristics[12]

V_{CC} = 0V; V_{EE} = –3.0V to –3.6V or V_{CC} = 3.0V to 3.6V; V_{EE} = 0V; T_A = –40°C to +85°C, unless otherwise stated.[13]

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTpp}	Output Voltage Amplitude at 3GHz[14]		540	670		520	650		450	580		mV
t_{PD}	Propagation Delay to Output Differential	CLK to Q, /Q	330	430	530	350	450	550	390	490	590	ps
		MR to Q, /Q	380	530	630	400	550	650	440	590	690	
t_{RR}	Reset Recovery	MR to CLK	240	100		250	100		260	100		ps
t_S	Set-Up Time	D to CLK	80	0		80	0		80	0		ps
t_H	Hold Time	CLK to D	80	0		80	0		80	0		ps
t_{PW}	Minimum Pulse Rate	MR	400			400			400			ps
t_{SKEW}	Within-Device Skew[15]			10	40		10	40		10	40	ps
	Device-to-Device Skew[16]			35	100		35	100		35	100	
t_{JITTER}	Clock Random Jitter (RMS) at ≤3.0GHz			0.2	1		0.2	1		0.2	1	ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)	Q, /Q	100	150	250	110	160	260	130	180	280	ps
			100	150	250	110	160	260	130	180	280	

Notes:

12. The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specifications limit values are applied individually under normal operating conditions and not valid simultaneously.
13. Measured using a 750mV source, 50% duty cycle clock source, all loading with 50Ω to V_{CC}–2V.
14. V_{OL} and V_{OH} specifications not guaranteed for f_{MAX} testing
15. Skew is measured between outputs under identical transitions and conditions on any one device.
16. Device-to-device skew for identical transitions at identical V_{CC} levels.

Input Stage

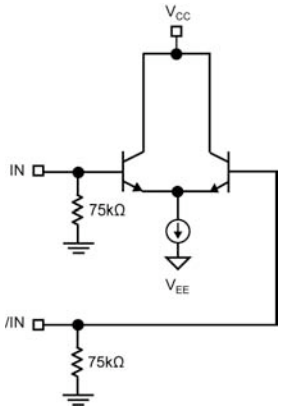
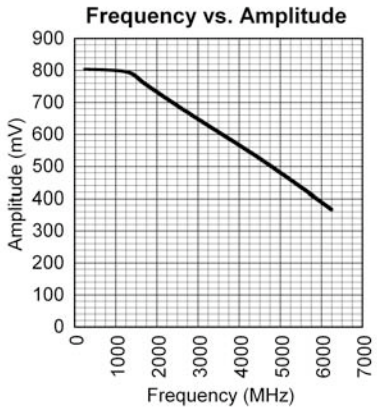
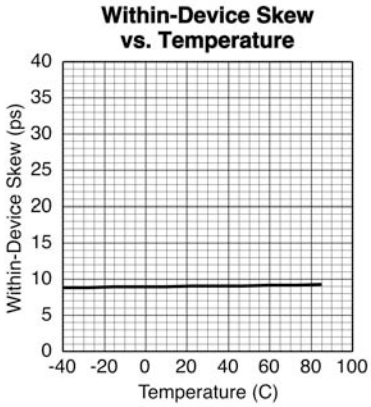


Figure 1. Simplified Differential Input Buffer

Typical Characteristics

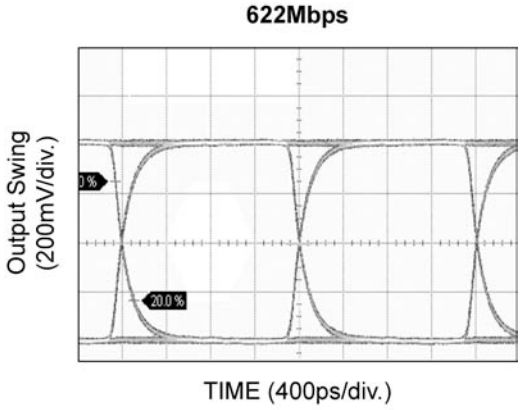
V_{CC} = 3.3V, GND = 0V, V_{IN} = 800mV, T_A = 25°C, unless otherwise stated.

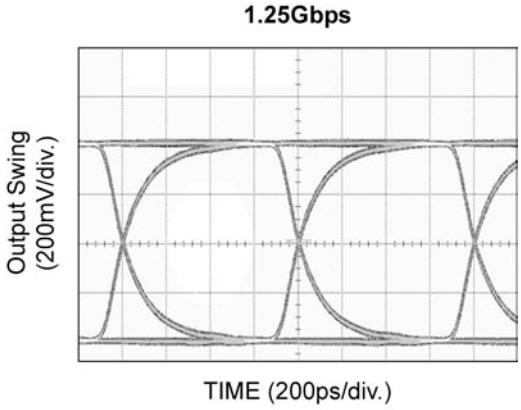


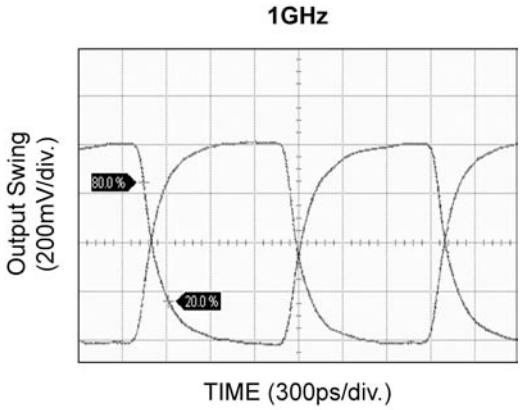


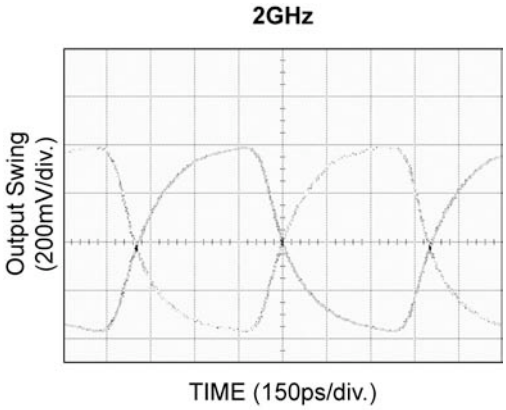
Functional Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = 800mV, T_A = 25°C, unless otherwise stated.









LVPECL Output Interface Applications

LVPECL output has very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figures 2 through 4.

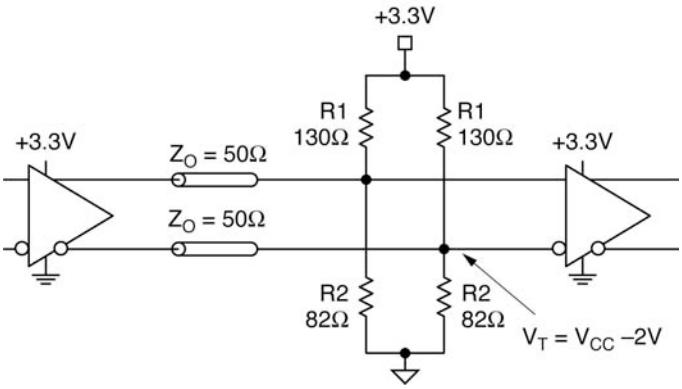


Figure 2. Parallel Termination-Thevenin Equivalent

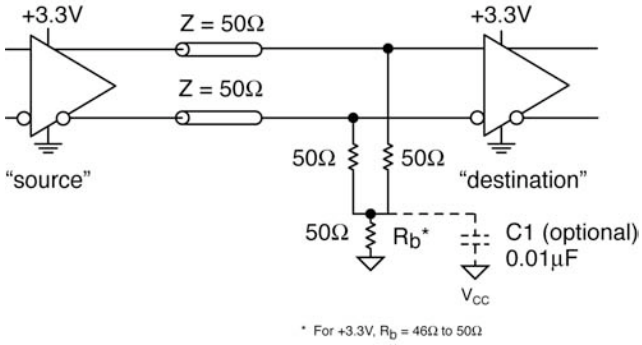


Figure 3. Three-Resistor "Y-Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_{CC}-2V.
4. C1 is an optional bypass capacitor intended to compensate for any t_r, t_f mismatches.

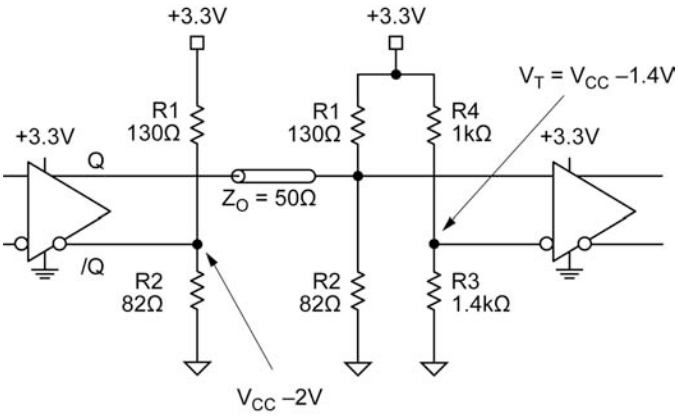


Figure 4. Terminating Unused I/O

Notes:

1. Unused output (/Q) must be terminated to balance the output.
2. Unused output pairs (Q and /Q) may be left floating.

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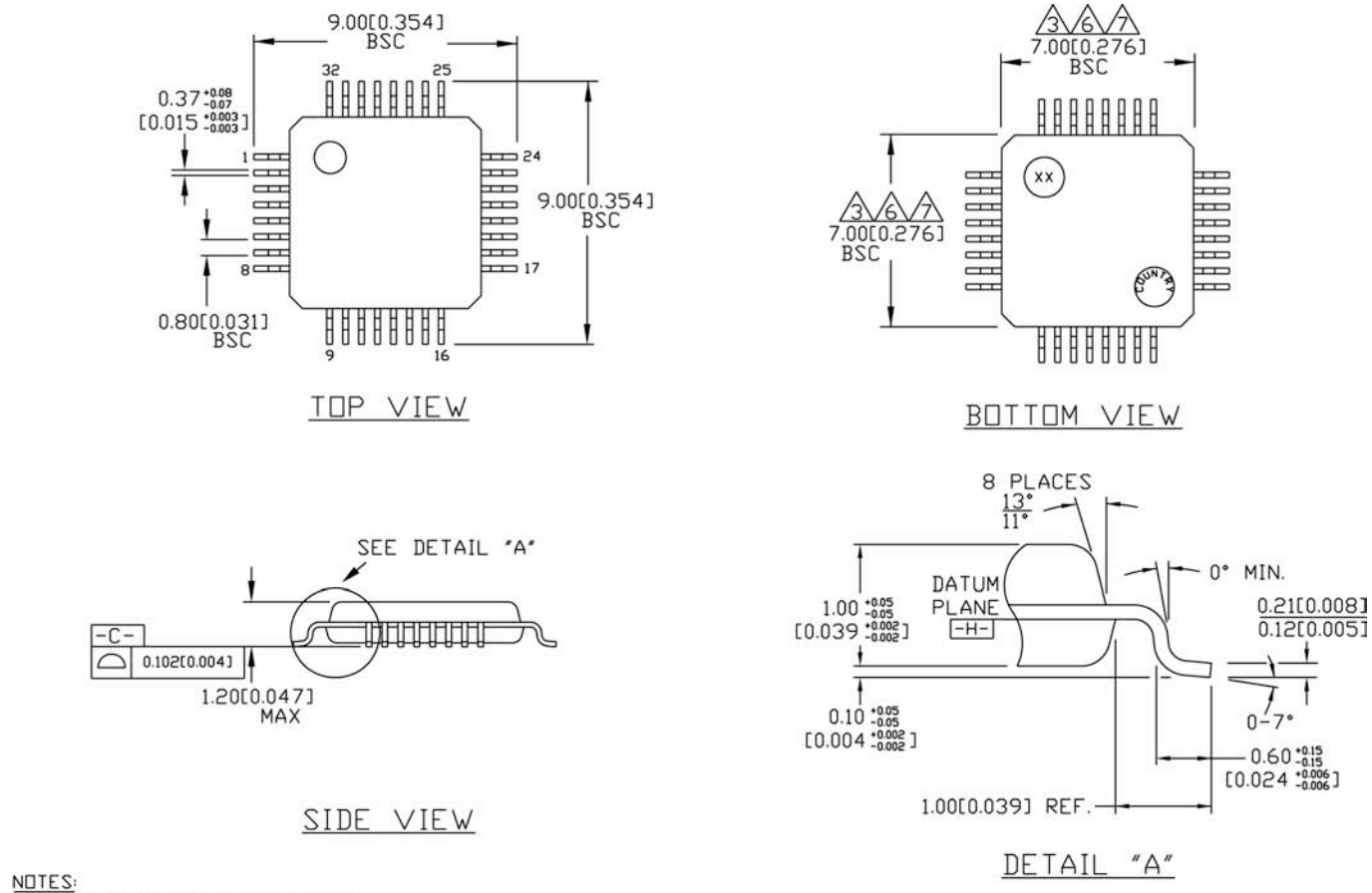
Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

32-Pin TQFP (T32-1)

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