



5V/3.3V DIFFERENTIAL DATA AND CLOCK D FLIP-FLOP

ECL Pro™
SY10EP52V

FEATURES

- Guaranteed maximum frequency >4GHz
- Guaranteed <410ps propagation delay over temperature
- 3.3V and 5V power supply options
- 75Ω internal input pulldown resistor
- Wide operating temperature range: -40°C to +85°C
- Available in 8-Pin (3mm) MSOP and SOIC package



ECL Pro™

DESCRIPTION

The SY10EP52V is a differential data, differential clock D flip-flop. The device is functionally equivalent to the EL52 device.

Data enters the master portion of the flip-flop when CLK is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK. The differential clock inputs of the EP52V allow the device to be used as a negative edge triggered flip-flop

The EP52V employs input clamping circuitry so that under open input condition (pulled down to V_{EE}) the outputs of the device will remain stable.

TRUTH TABLE

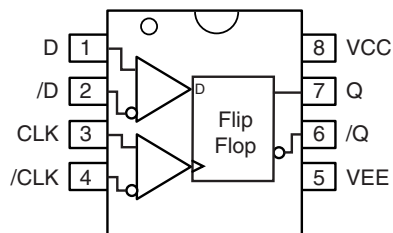
D	CLK	Q
L	Z	L
H	Z	H

Z = LOW to HIGH Transition

PIN NAMES

Pin	Function
CLK, /CLK	ECL Clock Inputs
D, /D	ECL Data Input
Q, /Q	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

PACKAGE/ORDERING INFORMATION



8-Pin SOIC and MSOP

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EP52VKC	K8-1	Commercial	HP52	Sn-Pb
SY10EP52VKCTR ⁽²⁾	K8-1	Commercial	HP52	Sn-Pb
SY10EP52VZC	Z8-1	Commercial	HEP52V	Sn-Pb
SY10EP52VZCTR ⁽²⁾	Z8-1	Commercial	HEP52V	Sn-Pb
SY10EP52VKI	K8-1	Industrial	HP52	Sn-Pb
SY10EP52VKITR ⁽²⁾	K8-1	Industrial	HP52	Sn-Pb
SY10EP52VZI	Z8-1	Industrial	HEP52V	Sn-Pb
SY10EP52VZITR ⁽²⁾	Z8-1	Industrial	HEP52V	Sn-Pb
SY10EP52VKG ⁽³⁾	K8-1	Industrial	HP52 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP52VKGTR ^(2, 3)	K8-1	Industrial	HP52 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP52VZG ⁽³⁾	Z8-1	Industrial	HEP52V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EP52VZGTR ^(2, 3)	Z8-1	Industrial	HEP52V with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V _{CC}	Power Supply Voltage (V _{EE} = 0)	+6.0 to 0	V
V _{EE}	Power Supply Voltage (V _{CC} = 0)	–6.0 to 0	V
V _{IN}	Input Voltage (V _{CC} = 0V, V _{IN} not more negative than V _{EE}) Input Voltage (V _{EE} = 0V, V _{IN} not more positive than V _{CC})	–6.0 to 0 +6.0 to 0	V V
I _{OUT}	Output Current –Continuous –Surge	50 100	mA
T _A	Operating Temperature Range	–40 to +85	°C
T _{STORE}	Storage Temperature Range	–65 to +150	°C
T _{LEAD}	Lead Temperature (soldering, 20 sec.)	+260	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) –Still Air SOIC MSOP	160 206	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case) SOIC MSOP	39 39	°C/W °C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5V PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{CC} = +5.0V ±10%, V_{EE} = 0V⁽²⁾

Symbol	Parameter	T _A = –40°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{EE}	Power Supply Current	—	—	47	—	35	47	—	—	47	mA
V _{OH}	Output HIGH Voltage ⁽³⁾	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V _{OL}	Output LOW Voltage ⁽³⁾	3050	3190	3315	3050	3255	3380	3050	3315	3440	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	3790	—	4115	3855	—	4180	3915	—	4240	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3065	—	3390	3130	—	3455	3190	—	3515	mV
V _{IHCMR}	Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Diff.)	2.0	—	V _{CC}	2.0	—	V _{CC}	2.0	—	V _{CC}	V
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I _{IL}	Input LOW Current CLK, D /CLK, /D	0.5 –150	— —	— —	0.5 –150	— —	— —	0.5 –150	— —	— —	μA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

Note 3. All loading with 50Ω to V_{CC} –2.0V.

Note 4. V_{IHCMR}(min) varies 1:1 with V_{EE}, V_{IHCMR}(max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

3.3V LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = +3.3V \pm 10\%$, $V_{EE} = 0V^{(2)}$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	—	44	—	—	45	—	—	47	mA
V_{OH}	Output HIGH Voltage ⁽³⁾	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage ⁽³⁾	1350	1490	1615	1350	1555	1680	1350	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090	—	2415	2155	—	2480	2215	—	2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365	—	1690	1430	—	1755	1490	—	1815	mV
V_{IHCMR}	Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Diff.)	2	—	V_{CC}	2	—	V_{CC}	2	—	V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current CLK,D /CLK, /D	0.5 -150	— —	— —	0.5 -150	— —	— —	0.5 -150	— —	— —	μA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC} .

Note 3. All loading with 50Ω to $V_{CC} - 2.0V$.

Note 4. $V_{IHCMR}(\min)$ varies 1:1 with V_{EE} , $V_{IHCMR}(\max)$ varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NECL/LVECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 0V$, $V_{EE} = -5.5V$ to $-3.0V^{(2)}$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current ⁽³⁾	—	—	47	—	35	47	—	—	47	mA
V_{OH}	Output HIGH Voltage ⁽⁴⁾	-1135		-0885	-1070	-0945	-0820	-1010		-0760	mV
V_{OL}	Output LOW Voltage ⁽⁴⁾	-1950		-1685	-1950	-1745	-1620	-1950		-1560	mV
V_{IH}	Input HIGH Voltage	-1210		-0885	-1145	—	-0820	-1085	—	-0760	mV
V_{IL}	Input LOW Voltage	-1935		-1610	-1870	—	-1545	-1810	—	-1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range ⁽⁵⁾	$V_{EE}+2.0$		V_{CC}	$V_{EE}+2.0$		V_{CC}	$V_{EE}+2.0$		V_{CC}	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA
I_{IL}	Input LOW Current CLK,D /CLK, /D	0.5 -150	— —	— —	0.5 -150	— —	— —	0.5 -150	— —	— —	μA

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC} .

Note 3. $V_{CC} = 0V$, $V_{EE} = V_{EE}(\min)$ to $V_{EE}(\max)$, all other pins floating.

Note 4. All loading with 50Ω to $V_{CC} - 2.0V$.

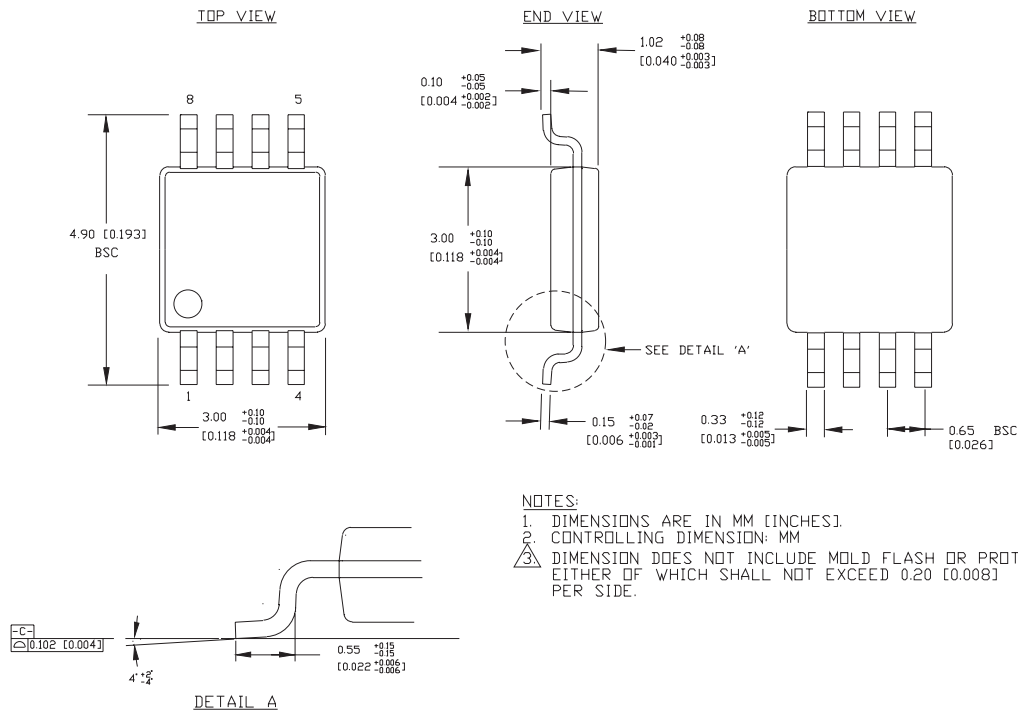
Note 5. $V_{IHCMR}(\min)$ varies 1:1 with V_{EE} , (max) varies 1:1 with V_{CC} .

AC ELECTRICAL CHARACTERISTICS⁽¹⁾NECL: $V_{CC} = 0V$, $V_{EE} = -3.3V$ to $-5.0V \pm 10\%$; PECL: $V_{EE} = 0V$, $V_{CC} = +3.3V$ to $+5.0V \pm 10\%$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency ⁽²⁾	4	—	—	4	—	—	4	—	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential CLK → Q, /Q	250	300	350	280	330	380	310	360	410	ps
t_S	Setup Time	50	—	—	50	—	—	50	—	—	ps
t_H	Hold Time	50	—	—	50	—	—	50	—	—	ps
t_{PW}	Minimum Pulse Width CLK	—	—	—	—	450	—	—	—	—	ps
t_{JITTER}	Cycle-to-Cycle Jitter (RMS)	—	—	—	—	0.2	1.0	—	—	—	ps _{RMS}
V_{DIFF}	Differential Input Voltage Range	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, /Q (20% to 80%)	70	100	170	80	120	180	90	130	200	ps

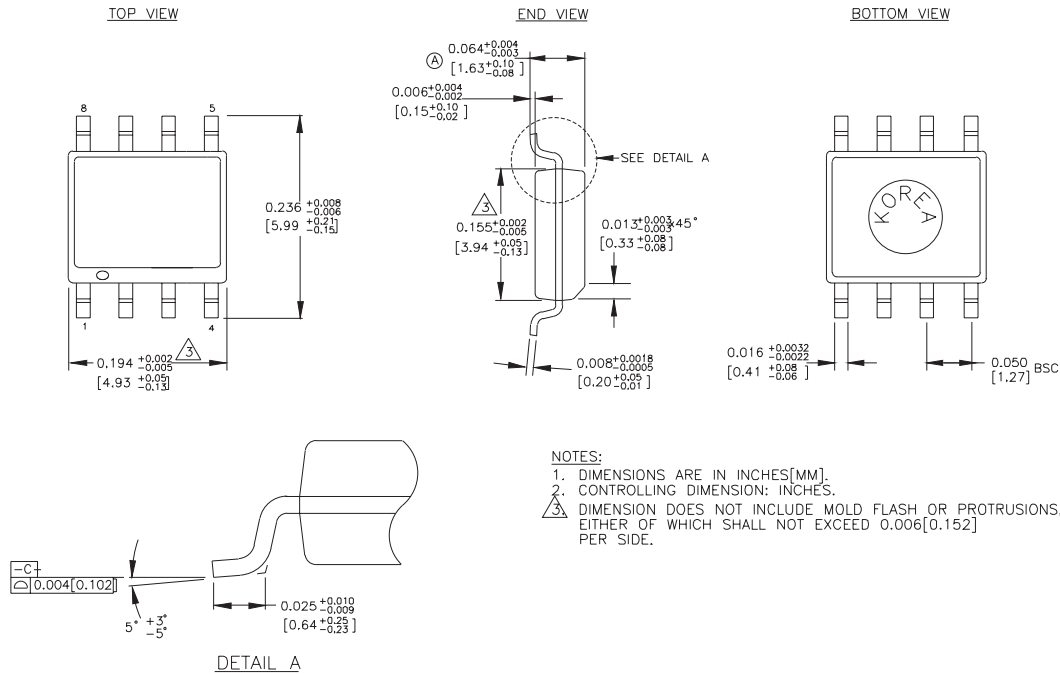
Note 1. Measured using a 750mV source, 50% duty cycle clock source. All loading with 50Ω to $V_{CC} - 2.0V$.Note 2. f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

8 LEAD MSOP (K8-1)



Rev. 01

8 LEAD PLASTIC SOIC (Z8-1)



Rev. 03

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